19-4478; Rev 0; 10/09

# Active Noise-Cancelling Solution for Stereo Headsets



## General Description

The MAX9895A is a complete audio subsystem for active noise-cancelling (ANC) stereo headsets. The device features three stages for each right and left channel. A microphone preamplifier, an analog sound processing block, and a headphone amplifier combine to create a simple and very flexible active noise-canceling system.

The MAX9895A features a feed-forward architecture, where outside microphones sense the ambient noise and on-board analog sound processing generates the compensation signal needed for noise reduction. This further supports the mechanical isolation of the headset by attenuating sound that leaks through the mechanics of the headphone.

The microphone preamplifiers feature programmable gain, allowing alignment of the microphone and driver tolerances and left-right channel matching. The headphone amplifiers are output capacitorless and can deliver 33mW into a 16Ω transducer.

The MAX9895A has three modes of operation: ANC on, PTL, and ANC off. The ANC-on mode demonstrates the noise-canceling performance of the device. PTL (push-to-listen) mode sends the microphone signals directly to the headphones to temporarily listen to the surroundings. ANC off disables noise-canceling, but allows use of the headphone amplifiers during music playback.

The MAX9895A is available in a space-saving WLP or TQFN package and is specified over the -40°C to +85°C extended temperature range.

## Applications

Noise-Cancelling Headphones/Headsets

Headsets for Mobile Communication

Mobile Phones

Portable Gaming Devices

E-Books

## Features

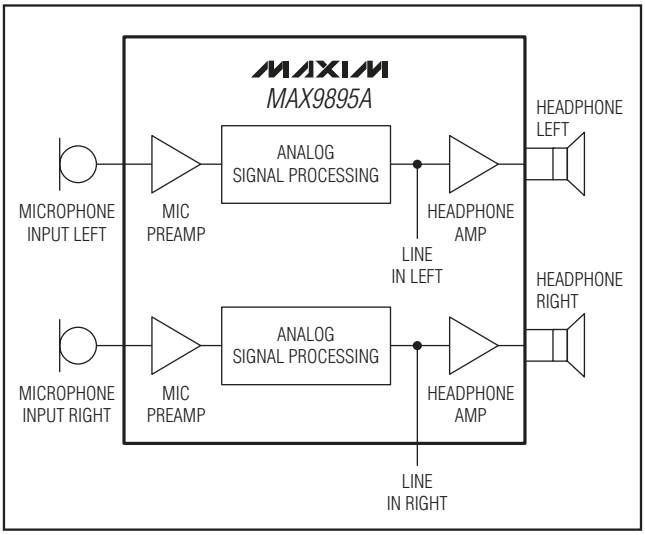
- **2.7V to 4.5V Operation**
- **Low Headphone Amplifier Noise**
- **Low-Noise Microphone Preamplifiers with 2.2V Bias**
- **Stereo 33mW into 16Ω Capacitorless Headphone Amplifiers**
- **Microphone Output Path Available for Speech Transmission**
- **Adjustable Microphone Gain by I²C Interface or External Resistors**
- **Low External Component Count**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | GAIN (V/V) |
|---|---|---|---|
| MAX9895AEWX+ | -40°C to +85°C | 36 WLP | 1 |
| MAX9895AETL+ | -40°C to +85°C | 40 TQFN-EP* | 1 |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*
**EP = Exposed pad.*

## Simplified Block Diagram




***Pin Configurations appear at end of data sheet.***

# Active Noise-Cancelling Solution for Stereo Headsets

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND .....-0.3V to +6V
PVDD to PGND .....-0.3V to +6V
PVDD to $V_{DD}$ .....-0.1V to +0.1V
CPVDD to PVDD .....Internally shorted
PGND to GND .....-0.1V to +0.1V
SDA, SCL .....-0.3V to +6V
LINEIN_ .....-0.3V to +6V
Any Other Pin .....-0.3V to ($V_{DD}$ + 0.3V)
Duration of Short Circuit Between HPOUT_ and GND .....Continuous
Duration of Short Circuit Between MICBIAS and $V_{DD}$, GND .....Continuous
Duration of Short Circuit Between $V_{MID}$ and $V_{DD}$, GND .....Continuous
Continuous Current into HPOUT_ .....200mA
Continuous Input Current (all other pins) .....±20mA
Continuous Power Dissipation ($T_A$ = +70°C)
36-Bump, 0.4mm-Pitch WLP Single-Layer Board (derate 17mW/°C above +70°C) .....1360mW
Maximum Current per Bump (10k hrs at +120°C) .....1.7A
TQFN Package (derate 22mW/°C above +70°C) .....1777mW
ESD Protection, Human Body Model .....±2kV
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = $V_{PVDD}$ = $V_{CPVDD}$ = 3.3V, $R_L$ = ∞, $C_{VDD}$ = 10µF connected between $V_{DD}$ and PGND, $C_{BIAS}$ = 1µF connected between $V_{BIAS}$ and GND, $C_{FLY}$ = 1µF connected between C1P and C1N. $C_{HOLD}$ = 1µF connected between $V_{MID}$ and PGND, $R_{PREIN\_}$ = 10kΩ, $R_{PREFB\_}$ = 50kΩ, $R_{MICBIAS}$ = 3.3kΩ, MIC signal gain in ANC mode ANC_GAIN = -11.5dB, MIC signal gain in PTL mode PTL_GAIN = -5.5dB, $V_{GAIN}$ = +1V/V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| Supply Voltage Range | $V_{DD}$<br>PVDD<br>CPVDD | Inferred by PSRR test | 2.7 | 3.3 | 4.5 | V |
| Quiescent Supply Current | $I_{DD}$ | ANC = on | | 3.4 | 4.6 | mA |
| | | ANC = off, PTL = off | | 2.5 | 3.4 | |
| | | PTL = on | | 3.4 | 4.6 | |
| Shutdown Supply Current | $I_{SHDN}$ | $I^2C$ mode, $T_A$ = +25°C | | | 12 | µA |
| Internal Reference | $V_{BIAS}$ | Voltage on $V_{BIAS}$ | 1.25 | 1.3 | 1.35 | V |
| Startup Time | $t_{ON}$ | Input from LINEIN_ | | 37 | | ms |
| | | Input from MICIN_ | | 390 | | |
| Undervoltage Lockout | UVLO | Falling threshold | 2.27 | | 2.65 | V |
| **HEADPHONE OUTPUTS** | | | | | | |
| Line Input Resistance | $R_{IN}$ | MAX9895A | 7 | 10 | 14 | kΩ |
| Output Offset Voltage | $V_{OS}$ | $T_A$ = +25°C | | 0.3 | ±3 | mV |
| Total Harmonic Distortion plus Noise | THD+N | $R_L$ = 32Ω, $P_{OUT}$ = 10mW, f = 1kHz from LINEIN_ | | 0.002 | | % |
| | | $R_L$ = 16Ω, $P_{OUT}$ = 10mW, f = 1kHz from LINEIN_ | | 0.002 | | |
| Power-Supply Rejection Ratio (Note 2) | PSRR | $V_{DD}$ = 2.5V to 4.5V, $T_A$ = +25°C | 60 | 70 | | dB |
| | | f ≤ 1kHz, $V_{IN}$ = 200m$V_{P-P}$ | | 65 | | |
| | | f = 10kHz, $V_{IN}$ = 200m$V_{P-P}$ | | 55 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = $V_{PVDD}$ = $V_{CPVDD}$ = 3.3V, $R_L$ = ∞, $C_{VDD}$ = 10µF connected between $V_{DD}$ and PGND, $C_{BIAS}$ = 1µF connected between $V_{BIAS}$ and GND, $C_{FLY}$ = 1µF connected between C1P and C1N. $C_{HOLD}$ = 1µF connected between $V_{MID}$ and PGND, $R_{PREIN\_}$ = 10kΩ, $R_{PREFB\_}$ = 50kΩ, $R_{MICBIAS}$ = 3.3kΩ, MIC signal gain in ANC mode ANC_GAIN = -11.5dB, MIC signal gain in PTL mode PTL_GAIN = -5.5dB, $V_{GAIN}$ = +1V/V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Power | $P_{OUT}$ | $R_L$ = 16Ω, THD+N = 1%, $T_A$ = +25°C (Note 3) | 20 | 38 | | mW |
| | | $R_L$ = 32Ω, THD+N = 1%, $T_A$ = +25°C | | 26 | | |
| Output Noise Voltage | $V_{ON}$ | ANC = off, PTL = off BW = 20Hz to 20kHz | | 9 | | $µV_{RMS}$ |
| | | ANC = off, PTL = off A-weighted | | 6 | | |
| | | ANC = on, A-weighted | | 6.5 | | |
| Slew Rate | SR | | | 0.2 | | V/µs |
| Maximum Capacitive Load | $C_{MAXLOAD}$ | No sustained oscillations (capacitance between HPOUT_ and $V_{MID}$) | | 100 | | pF |
| Click-and-Pop Level | KCP | Turn on; $R_L$ = 32Ω, peak voltage, A-weighted, 32 samples/sec, $T_A$ = +25°C (Note 4) | | -73 | | dBV |
| | | Turn off; $R_L$ = 32Ω, peak voltage, A-weighted, 32 samples/sec, $T_A$ = +25°C (Note 4) | | -72 | | |
| Crosstalk | | f = 1kHz, $R_L$ = 32Ω, $P_{OUT}$ = 10mW, TQFN | | 57 | | dB |
| | | WLP | | 70 | | |
| **MICROPHONE INPUTS** | | | | | | |
| Preamplifier Feedback Resistance | $R_{PREFB}$ | External | 10 | | 100 | kΩ |
| Preamplifier Input Resistance | $R_{PREIN}$ | External | 1 | | 10 | kΩ |
| Input Bias Current | $I_{BIAS}$ | Measured at MICIN, $T_A$ = +25°C | | 1 | 10 | nA |
| Microphone Input Noise Voltage | $e_N$ | BW = 20Hz to 20kHz measured at MICOUT_ | | 6 | | µV |
| Minimum ANC Gain | ANCG_MIN | MICOUT_ to HPOUT_, measured at DC | -18.0 | -17.5 | -17.0 | dB |
| Maximum ANC Gain | ANCG_MAX | | -6.0 | -5.5 | -5.0 | dB |
| Minimum PTL Gain | PTLG_MIN | | -12.0 | -11.5 | -11.0 | dB |
| Maximum PTL Gain | PTLG_MAX | | 0 | 0.5 | 1 | dB |
| ANC/PTL Gain Stepsize | AG_STEP | MICOUT_ to HPOUT_, measured at DC | | 0.5 | | dB |
| OPA Offset | | Measured at SPR1 and SPR2 with respect to $V_{BIAS}$ | -30 | | +30 | mV |
| Maximum Capacitive Load | $C_{MAXLOAD}$ | Allowed capacitance to GND on MICOUT_ and all signal processing filter I/O except SPC3 | | 15 | | pF |
| Dynamic Range | MICDYN | Swing of all internal and external nodes of preamplifier, signal processing, and filter with respect to $V_{BIAS}$ | | ±1 | | V |

# Active Noise-Cancelling Solution for Stereo Headsets

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = $V_{PVDD}$ = $V_{CPVDD}$ = 3.3V, $R_L$ = ∞, $C_{VDD}$ = 10µF connected between $V_{DD}$ and PGND, $C_{BIAS}$ = 1µF connected between $V_{BIAS}$ and GND, $C_{FLY}$ = 1µF connected between C1P and C1N. $C_{HOLD}$ = 1µF connected between $V_{MID}$ and PGND, $R_{PREIN\_}$ = 10kΩ, $R_{PREFB\_}$ = 50kΩ, $R_{MICBIAS}$ = 3.3kΩ, MIC signal gain in ANC mode ANC_GAIN = -11.5dB, MIC signal gain in PTL mode PTL_GAIN = -5.5dB, $V_{GAIN}$ = +1V/V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Maximum Output Current | $I_{OUT}$ | Current capability of preamplifier, signal processing, and filter output | | ±500 | | µA |
| PTL Attenuation | | Attenuation from LINEIN_ to HPOUT_ in PTL mode | | 40 | | dB |
| **MICROPHONE BIAS (MICBIAS Pin)** | | | | | | |
| MIC Bias Voltage | $V_{MICBIAS}$ | $V_{DD}$ = 3.3V; 100µA < $I_{MICBIAS}$ < 1mA | 2.1 | 2.2 | 2.3 | V |
| MIC Bias Current Limit | $I_{MICLM}$ | | | 35 | | mA |
| Maximum Capacitive Load | $C_{MAXLOAD}$ | | | 100 | | pF |
| MICBIAS PSRR | MB_PSRR | $V_{DD}$ from 2.7V to 4.5V | 55 | 62 | | dB |
| | | f = 20kHz | | 60 | | |
| MICBIAS Noise | MB_N | | | 6 | | µV |
| **CHARGE PUMP** | | | | | | |
| Charge-Pump Frequency | $f_{OSC}$ | | 225 | 250 | 275 | kHz |
| $V_{MID}$ Output Resistance | $R_{VMID}$ | | | 4 | | Ω |
| **DIGITAL INPUT SDA (SCL Tied to GND: I²C Interface Disabled)** | | | | | | |
| Input Leakage | $I_L$ | $V_{SDA}$ = 0V to 3.3V<br>$T_A$ = +25°C | | | ±16 | µA |
| Input Voltage High | $V_{IH}$ | | 1.8 | | | V |
| Input Voltage Low | $V_{IL}$ | | | | 0.8 | V |
| **SCL/SDA (I²C Interface Enabled)** | | | | | | |
| Input Voltage High | $V_{IH}$ | 1.8V CMOS compatibility | 1.4 | | | V |
| Input Voltage Low | $V_{IL}$ | 1.8V CMOS compatibility | | | 0.4 | V |
| Input Hysteresis | $V_{IHIST}$ | | | 0.2 | | V |
| Input High Leakage Current | $I_{IH}$ | $V_{IN}$ = 3V; $T_A$ = +25°C | | | ±1 | µA |
| Input Low Leakage Current | $I_{IL}$ | $V_{IN}$ = 0; $T_A$ = +25°C | | | ±1 | µA |
| Input Capacitance | $C_{IN}$ | | | 10 | | pF |
| Output Voltage Low | $V_{OL}$ | $I_{OL}$ = 3mA; $T_A$ = +25°C | | | 0.4 | V |
| **I²C INTERFACE** | | | | | | |
| Serial-Clock Frequency | $f_{SCL}$ | | | | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | µs |
| Hold Time (REPEATED) START Condition | $t_{HD:STA}$ | | 0.6 | | | µs |
| Setup Time for a REPEATED START Condition | $t_{SU:STA}$ | | 0.6 | | | µs |

## ELECTRICAL CHARACTERISTICS (continued)

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCL Pulse-Width Low | $t_{LOW}$ | | 1.3 | | | µs |
| SCL Pulse-Width High | $t_{HIGH}$ | | 0.6 | | | µs |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | | 900 | ns |
| SDA and SCL Receiving Rise Time | $t_R$ | (Note 5) | 20 + 0.1$C_B$ | | 300 | ns |
| SDA and SCL Receiving Fall Time | $t_F$ | (Note 5) | 20 + 0.1$C_B$ | | 300 | ns |
| SDA Transmitting Fall Time | $t_F$ | (Note 5) | 20 + 0.1$C_B$ | | 250 | ns |
| Setup Time for STOP Condition | $t_{SU,STO}$ | | 0.6 | | | µs |
| Bus Capacitance | $C_B$ | | | | 400 | pF |
| Pulse Width of Suppressed Spike | $t_{SP}$ | | 0 | | 50 | ns |

**Note 1:** All devices are 100% production tested at $T_A$ = +25°C. Specifications over temperature limits are guaranteed by design.

**Note 2:** PSRR at any frequency is limited by resistor matching (common-mode sense architecture used to reject the modulation on VMID).

**Note 3:** Output power is guaranteed by measuring the RDSON of all power MOSFETs (headphone driver and charge pump).

**Note 4:** Line inputs AC-coupled to GND.

**Note 5:** $C_B$ is in pF.

# Active Noise-Cancelling Solution for Stereo Headsets

## Typical Operating Characteristics

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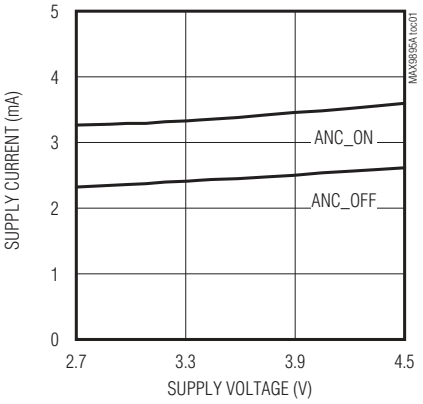
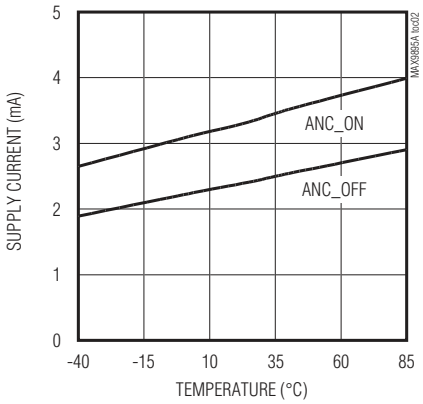
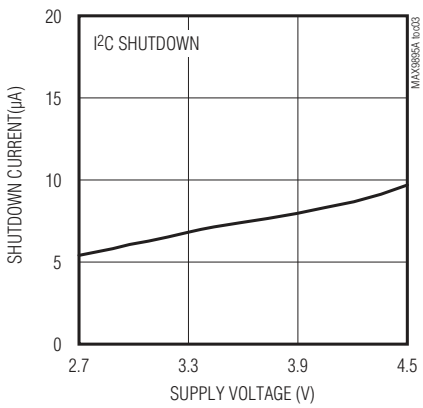
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



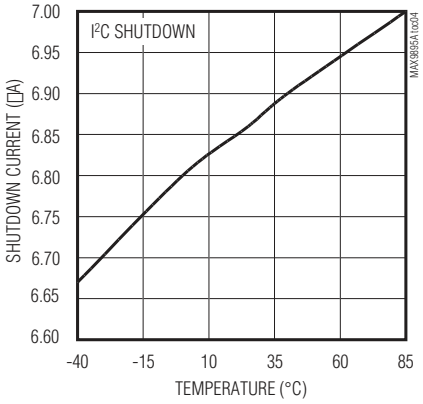

**SUPPLY CURRENT vs. TEMPERATURE**



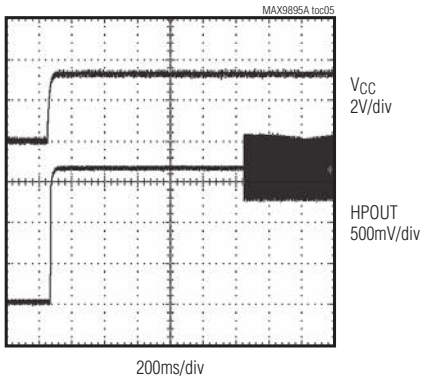

**SHUTDOWN CURRENT vs. SUPPLY VOLTAGE**



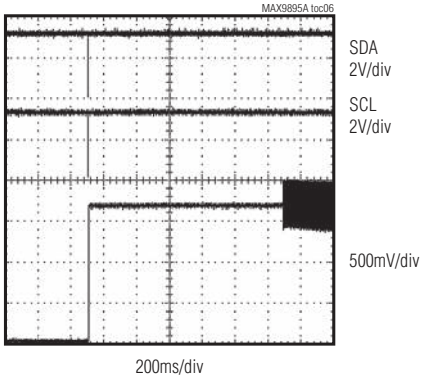

**SHUTDOWN CURRENT vs. TEMPERATURE**



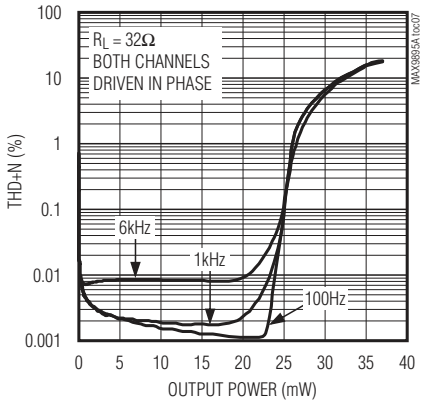

**HARDWARE TURN-ON**



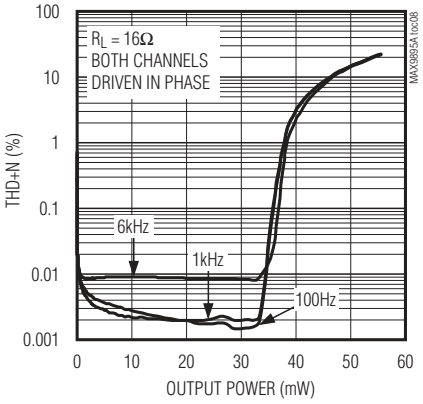

**SOFTWARE TURN-ON**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER**



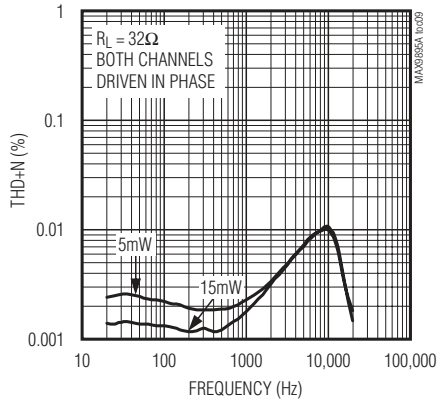

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER**



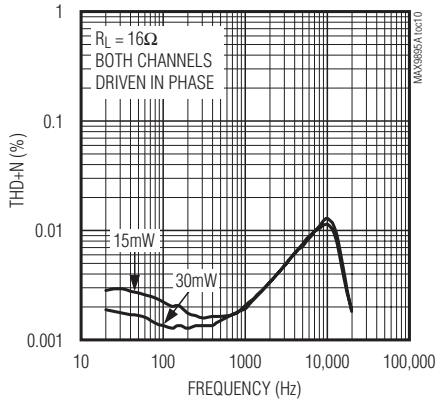
## Typical Operating Characteristics (continued)

($V_{DD}$ = $V_{PVDD}$ = $V_{CPVDD}$ = 3.3V, $R_L$ = ∞, $C_{VDD}$ = 10µF connected between $V_{DD}$ and PGND, $C_{BIAS}$ = 1µF connected between $V_{BIAS}$ and GND, $C_{FLY}$ = 1µF connected between C1P and C1N. $C_{HOLD}$ = 1µF connected between $V_{MID}$ and GND, $R_{PREIN\_}$ = 10kΩ, $R_{PREFB\_}$ = 10kΩ, $R_{MICBIAS}$ = 3.3kΩ, MIC signal gain in ANC mode ANC_GAIN = -11.5dB, MIC signal gain in PTL mode PTL_GAIN = -5.5dB, both outputs driven in phase, GAIN = +1V/V (MAX9895AA)).

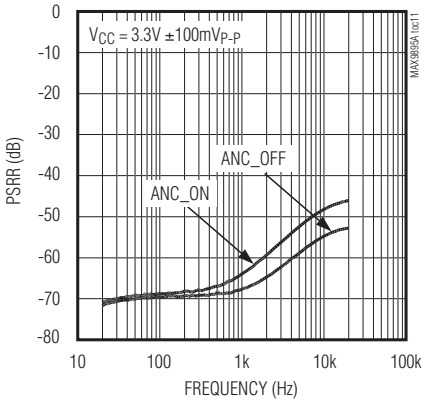
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



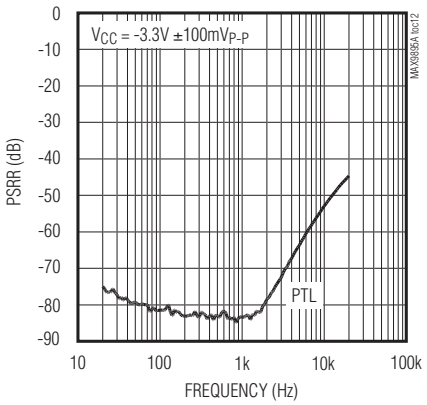

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



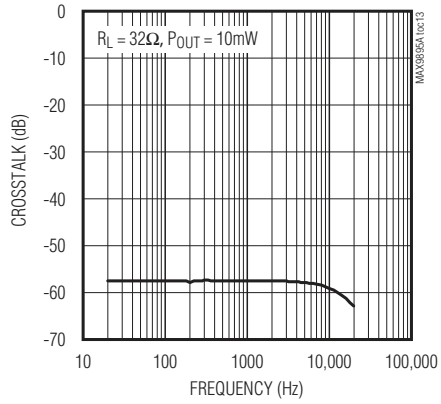

**POWER-SUPPLY REJECTION RATIO**



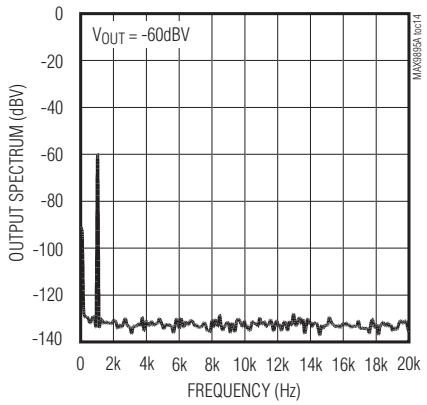

**POWER-SUPPLY REJECTION RATIO**




**CROSSTALK vs. FREQUENCY**




**OUTPUT SPECTRUM vs. FREQUENCY**



# Active Noise-Cancelling Solution for Stereo Headsets

## Typical Operating Characteristics (continued)

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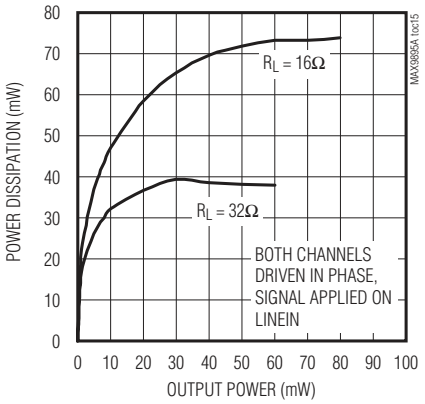
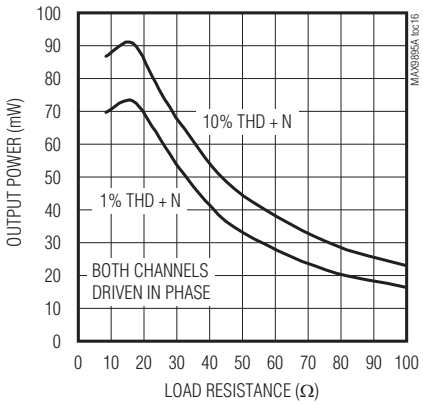
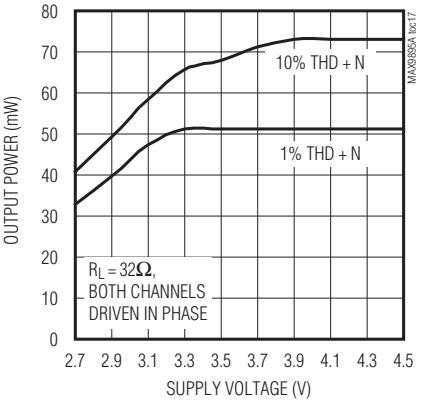
**POWER DISSIPATION vs. OUTPUT POWER**



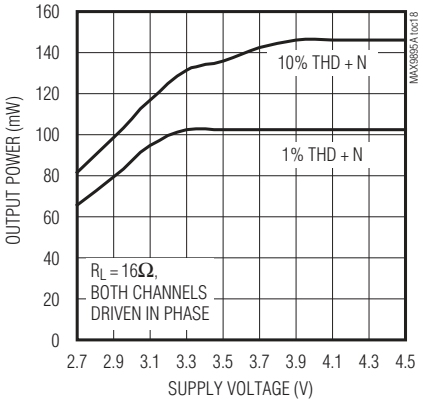

**OUTPUT POWER vs. LOAD RESISTANCE**



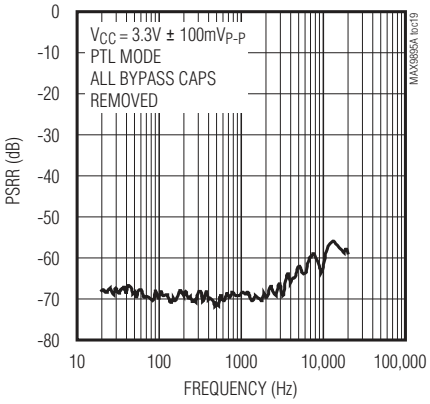

**TOTAL OUTPUT POWER vs. SUPPLY VOLTAGE**



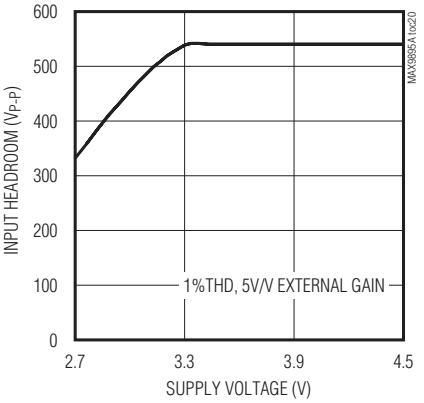

**OUTPUT POWER vs. SUPPLY VOLTAGE**




**MICBIAS POWER-SUPPLY REJECTION RATIO**




**MICIN INPUT HEADROOM vs. SUPPLY VOLTAGE**



## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| TQFN | WLP | | |
| 1 | A6 | SPR1_L | Left-Channel Signal Processing |
| 2 | C5 | MICOUT_L | Left-Channel Microphone Preamplifier Output. Apply feedback resistor to set input gain. See the *Microphone Output* section for more details. |
| 3 | B6 | MICIN_L | Left-Channel Microphone Input |
| 4 | C6 | MICBIAS | Microphone Supply Voltage. Use separate left/right MICBIAS resistors. |
| 5 | C4 | LINEIN_L | Left-Channel Audio Line Input |
| 6 | D4 | LINEIN_R | Right-Channel Audio Line Input |
| 7, 8 | D6 | GND | Signal Ground (Reference for $V_{BIAS}$, MICBIAS, and LINEIN) |
| 9 | E6 | MICIN_R | Right-Channel Microphone Input |
| 10 | D5 | MICOUT_R | Right-Channel Microphone Preamplifier Output. Apply feedback resistor to set input gain. |
| 11 | F6 | SPR1_R | Right-Channel Signal Processing |
| 12 | E5 | SPC1_R | Right-Channel Signal Processing |
| 13 | F5 | SPC2_R | Right-Channel Signal Processing |
| 14 | E4 | SPC3_R | Right-Channel Signal Processing |
| 15 | F4 | SPC4_R | Right-Channel Signal Processing |
| 16 | E3 | SPR2_R | Right-Channel Signal Processing |
| 17 | F3 | $V_{BIAS}$ | Internal Reference. Bypass $V_{BIAS}$ to GND with a 1µF capacitor. Used for MICIN and LINEIN. |
| 18 | E2 | SPFC2_R | Right-Channel Signal Processing |
| 19 | F2 | SPFC1_R | Right-Channel Signal Processing |
| 20 | D2 | SPFO_R | Right-Channel Signal Processing |
| 21 | F1 | HPOUT_R | Right-Channel Headphone Output |
| 22 | E1 | $V_{DD}$ | Positive Supply Voltage |
| 23 | | PVDD | |
| 24 | | CPVDD | |
| 25 | D1 | C1P | Charge-Pump Flying Capacitor Positive |
| 26 | C1 | C1N | Charge-Pump Flying Capacitor Negative |
| 27 | B1 | $V_{MID}$ | Charge-Pump Output Voltage. Connect to common return of headphone. Bypass $V_{MID}$ with a 1µF capacitor to PGND. |
| 28 | — | N.C. | No Connection |
| 29 | A1 | PGND | Power Ground |
| 30 | D3 | SDA/NC-MODE | I²C Interface Data Line. Also used as MODE select in hardware mode (SCL = GND). See Table 1. |
| 31 | C3 | SCL | I²C Interface Clock Line. Connect to GND for hardware mode. |
| 32 | A2 | HPOUT_L | Left-Channel Headphone Output |

# Active Noise-Cancelling Solution for Stereo Headsets

## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| TQFN | WLP | | |
| 33 | C2 | SPFO_L | Left-Channel Signal Processing |
| 34 | B2 | SPFC1_L | Left-Channel Signal Processing |
| 35 | A3 | SPFC2_L | Left-Channel Signal Processing |
| 36 | B3 | SPR2_L | Left-Channel Signal Processing |
| 37 | A4 | SPC4_L | Left-Channel Signal Processing |
| 38 | B4 | SPC3_L | Left-Channel Signal Processing |
| 39 | A5 | SPC2_L | Left-Channel Signal Processing |
| 40 | B5 | SPC1_L | Left-Channel Signal Processing |
| — | — | EP | Exposed Pad. Must be connected to PGND. |

## Detailed Description

The MAX9895A is a complete audio subsystem for active noise-cancelling stereo headsets. The device features a microphone preamplifier, an analog sound processing block, and a headphone amplifier combining to create a simple and very flexible active noise-canceling system. The MAX9895A uses feed-forward architecture, creating a headphone signal that has the same amplitude, but opposite phase as outside noise that leaks through the mechanical isolation of the earphones. These two signals cancel each other and provide noise suppression at the ear. The device consists of an ultra-low noise microphone preamplifier to set input impedance and gain, followed by an analog signal processing block, and a capacitorless headphone amplifier. The headphone amplifier does not require the large output-coupling capacitors used by conventional single-supply headphone amplifiers, and can output 33mW into a 16Ω headphone. The product also features undervoltage lockout and comprehensive click-and-pop suppression circuitry. See the *Functional Diagram/Typical Applications Circuit* for further details.

### Modes of Operation

The MAX9895A features three modes of operation; active noise canceling (ANC) on or off, and push-to-listen (PTL). The ANC-on mode provides full noise canceling and provides line-input mixing to the headphones. This allows music to be played while noise canceling is operational. The ANC-off mode disables the microphone preamplifiers and noise processing blocks, but allows the line inputs to operate normally. This gives flexibility to the design such that music can still be played through the headphones while noise canceling is inactive.

The PTL mode connects the microphone preamplifier directly to the headphone amplifier, bypassing the noise cancellation, and attenuates the line-input signal. PTL mode gives the user the option of listening to the surroundings without removing the headphones. See Table 1 for hardware mode settings.

### Microphone Preamplifier

The MAX9895A features an ultra-low noise microphone input preamplifier. Using an inverting op amp design with external input and feedback resistors allows flexibility in setting input impedance and gain. The microphone gain can be adjusted in two ways: adjust the feedback resistor in the preamplifier stage by use of a potentiometer or setting I²C registers using a microcontroller to adjust the gain after the analog processing stage.

#### Microphone Bias Supply

The MAX9895A provides a low-noise voltage bias designed for biasing electret condenser microphones (ECM). The bias output is regulated to 2.5V.

### Table 1. Mode Selection (in Hardware Mode)

| SDA LEVEL | CONFIGURATION |
|---|---|
| GND | (PTL Mode) LINEIN_ is attenuated, MICOUT_ signal is passed directly to the headphone driver without filtering and phase reversal. |
| Hi-Z | ANC on |
| $V_{DD}$ | ANC off (only HP amps are active) |

### Microphone Output

The outputs of the microphone preamplifiers are provided to allow for external adjustment of the gain of the preamplifier and to provide a path for voice transmission (headset) applications.

### Programmable Gain

The second gain stage can be programmed in 0.5dB steps to compensate for microphone and headphone sensitivity. This requires a microcontroller connected to the I²C bus, which operates in slave mode. An alternate solution for gain setting is to add a trim-pot to the feedback resistor of the microphone preamplifier. See the *Typical Application Circuit*.

### Analog Signal Processing

This block creates the noise cancellation signal. The signal processing block uses the output of the microphone preamp and external components to create a headphone signal that has the same amplitude, but opposite phase as outside noise that leaks through the mechanical isolation of the earphones, so both waves cancel each other. **Note:** The choice of external components depends on the headset characteristics. Please contact your local Maxim sales office for more information on determining the proper component values for the *Analog Signal Processing* section.

### Headphone Amplifier

The stereo headphone amplifier is capable of delivering 33mW into 16Ω loads and has a gain (line in to headphone out) of 1V/V for the MAX9895AA. The input to the headphone amplifier is a linear sum of three signals: line in (external input), mic gain (output of analog signal processing block) and PTL gain (ANC bypass).

Unlike conventional single-supply, single-ended amplifiers, the MAX9895A headphone amplifier does not need large DC-blocking caps, as the outputs are referred to $V_{CC}/2$, which is the bias output voltage of the amplifier. Conventional single-supply headphone amplifiers require large coupling capacitors to block the output DC bias from the headphone. The MAX9895A architecture uses a high-efficiency charge pump to create an internal midbias supply voltage ($V_{MID}$). This keeps supply current low and allows the amplifier outputs to be connected directly to the headphones without the need for these large coupling capacitors.

## Serial Interface

The MAX9895A features an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9895A and the master at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The MAX9895A is a receive-only slave device relying on the master to generate the SCL signal. The MAX9895A cannot write to the SDA bus except to acknowledge the receipt of data from the master. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. If the serial interface is not used, the SCL pin must be tied to GND to disable this feature and allow the device to be used in hardware mode (no microcontroller).

A master device communicates to the MAX9895A by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) con-

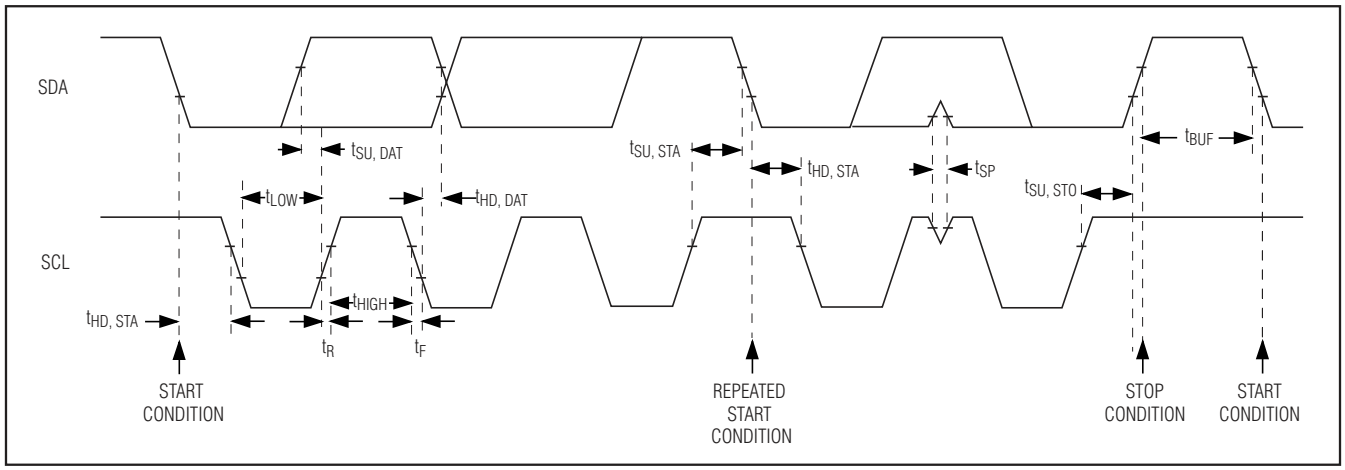



*Figure 1. 2-Wire Serial-Interface Timing Diagram*

# Active Noise-Cancelling Solution for Stereo Headsets

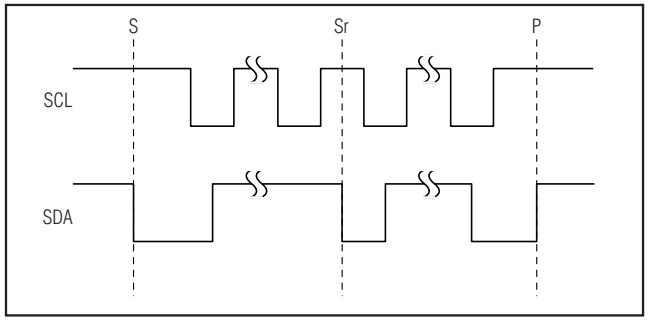



*Figure 2. START, STOP, and REPEATED START Conditions*

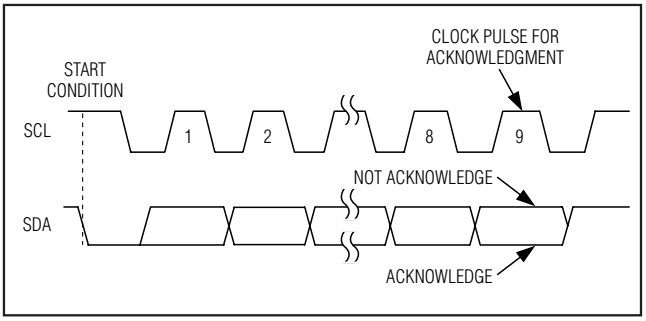



*Figure 3. Acknowledge*

dition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9895A SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The MAX9895A SCL line operates as an input only. A pullup resistor, greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9895A from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

### Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

## START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master device initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP (P) condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of transmission to the MAX9895A. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

## Early STOP Conditions

The MAX9895A recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

## Slave Address

The MAX9895A is available with 0x40 preset slave addresses. The address is defined as the seven most significant bits (MSBs) followed by the read/write (R/W) bit. The address is the first byte of information sent to the MAX9895A after the START condition. The MAX9895A is a slave device only capable of being written to. The sent R/W bit must always be a zero when configuring the MAX9895A.

The MAX9895A acknowledges the receipt of its address even if R/W is set to 1. However, the MAX9895A does not drive SDA. Addressing the MAX9895A with R/W set to 1 causes the master to receive all 1s regardless of the contents of the command register.

## Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9895A uses to handshake receipt of each byte of data (see Figure 3). The MAX9895A pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

## Write Data Format

A write to the MAX9895A includes transmission of a START (S) condition, the slave address with the R/W bit reset to 0, one byte of data to configure the command register, and a STOP (P) condition. Figure 4 illustrates the proper format for one frame.

The MAX9895A only accepts write data, but it acknowledges the receipt of its address byte with the R/W bit set high. The MAX9895A does not write to the SDA bus

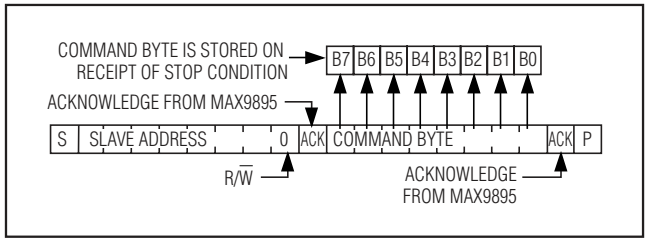



*Figure 4. Write Data Format Example*

in the event that the R/W bit is set high. Subsequently, the master reads all 1s from the MAX9895A. Always reset the R/W bit to 0 to avoid this situation.

### I²C-Enabled Software Mode

The MAX9895A can operate with or without an external microcontroller (µC). When a µC is present, commands are sent through the I²C protocol (SCL, SDA).

### I²C-Disabled Hardware Mode

By tying SCL to ground, the I²C interface is disabled and the device operates in hardware mode. In this case, the SDA pin operates as a MODE select. Table 1 shows different configurations with the SDA level.

## Application Information

### Input-Coupling Capacitor

The input capacitor ($C_{IN}$), in conjunction with the input resistor ($R_{IN}$), forms a highpass filter that removes the DC bias from an incoming signal (see the *Functional Diagram/Typical Applications Circuit*). The AC-coupling capacitor allows the device to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose the CIN so that $f_{-3dB}$ is well below the lowest frequency of interest. Setting $f_{-3dB}$ too high affects the device's low-frequency response. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies.

Apply same method for microphone input-coupling capacitor ($C_{PREIN\_}$). The $R_{IN}$ for microphone input is $R_{PREIN\_}$.

### Setting the Gains

The gains of the microphone input preamplifiers are set through the feedback using the following equation:

$$A_V\ (V/V) = -(R_F/R_{IN})$$

In stand-alone control mode, the internal gain stage for MIC GAIN is fixed at 11.5dB and the PTL GAIN stage is fixed at -5.5dB. In software control mode (I²C mode), the internal gain stage stages, MIC GAIN and PTL GAIN, are programmable through the I²C registers. See the *Serial Interface* section for more information.

The LINE IN and HEADPHONE AMP stages each have fixed voltage gain of 0dB.

### Charge-Pump Capacitor Selection

Use ceramic capacitors with a low ESR for optimum performance. For optimal performance over the extended temperature range, select capacitors with an X7R dielectric. Table 2 lists suggested manufacturers.

### Layout and Grounding

Proper layout and grounding are essential for optimum performance. Connect PGND and GND together at a single point on the PCB. Place the power-supply bypass capacitor and the charge-pump hold capacitor as close as possible to the MAX9895A. Route PGND and all traces that carry switching transients away from GND and the audio signal path. The thin QFN package features an exposed pad that improves thermal efficiency. Ensure that the exposed pad is electrically connected to PGND and is isolated from $V_{DD}$, PVDD, and CPVDD.

**Table 2. Suggest Capacitor Manufacturers**

| SUPPLIER | PHONE | FAX | WEBSITE |
|---|---|---|---|
| Taiyo Yuden | 800-348-2496 | 847-925-0899 | www.t-yuden.com |
| TDK | 847-803-6100 | 847-390-4405 | www.component.tdk.com |
| Murata | 770-436-1300 | 770-436-3030 | www.murata.com |

# Active Noise-Cancelling Solution for Stereo Headsets

## Table 3. I²C Register Table

| ADDRESS | TYPE | POR | NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | R/W | 0x0B | ANC_GAIN_LEFT | X | X | X | ANC GAIN setting for LEFT CHANNEL | | | | |
| 0x01 | R/W | 0x0B | ANC_GAIN_RIGHT | X | X | X | ANC GAIN setting for RIGHT CHANNEL | | | | |
| 0x02 | R/W | 0x0B | PTL_GAIN_LEFT | X | X | X | PTL GAIN setting for LEFT CHANNEL | | | | |
| 0x03 | R/W | 0x0B | PTL_GAIN_RIGHT | X | X | X | PTL GAIN setting for RIGHT CHANNEL | | | | |
| 0x04 | R/W | 0x00 | MODE | X | | | | 0 | PTL | $\overline{ANC}$ | $\overline{SHDN}$ |

## Table 4. Gain Setting Register 0x00, 0x01, 0x02, 0x03

| HEX | 0x00, 0x01 ANC GAIN [dB] | HEX | 0x00, 0x01 ANC GAIN [dB] | HEX | 0x00, 0x01 ANC GAIN [dB] |
|---|---|---|---|---|---|
| 0x00 | -6.0 | 0x08 | -10.0 | 0x10 | -14.0 |
| 0x01 | -6.5 | 0x09 | -10.5 | 0x11 | -14.5 |
| 0x02 | -7.0 | 0x0A | -11.0 | 0x12 | -15.0 |
| 0x03 | -7.5 | 0x0B (POR) | -11.5 | 0x13 | -15.5 |
| 0x04 | -8.0 | 0x0C | -12.0 | 0x14 | -16.0 |
| 0x05 | -8.5 | 0x0D | -12.5 | 0x15 | -16.5 |
| 0x06 | -9.0 | 0x0E | -13.0 | 0x16 | -17.0 |
| 0x07 | -9.5 | 0x0F | -13.5 | 0x17 | -17.5 |
| **HEX** | **0x02, 0x03 PTL GAIN [dB]** | **HEX** | **0x02, 0x03 PTL GAIN [dB]** | **HEX** | **0x02, 0x03 PTL GAIN [dB]** |
| 0x00 | -0.0 | 0x08 | -4.0 | 0x10 | -8.0 |
| 0x01 | -0.5 | 0x09 | -4.5 | 0x11 | -8.5 |
| 0x02 | -1.0 | 0x0A | -5.0 | 0x12 | -9.0 |
| 0x03 | -1.5 | 0x0B (POR) | -5.5 | 0x13 | -9.5 |
| 0x04 | -2.0 | 0x0C | -6.0 | 0x14 | -10.0 |
| 0x05 | -2.5 | 0x0D | -6.5 | 0x15 | -10.5 |
| 0x06 | -3.0 | 0x0E | -7.0 | 0x16 | -11.0 |
| 0x07 | -3.5 | 0x0F | -7.5 | 0x17 | -11.5 |

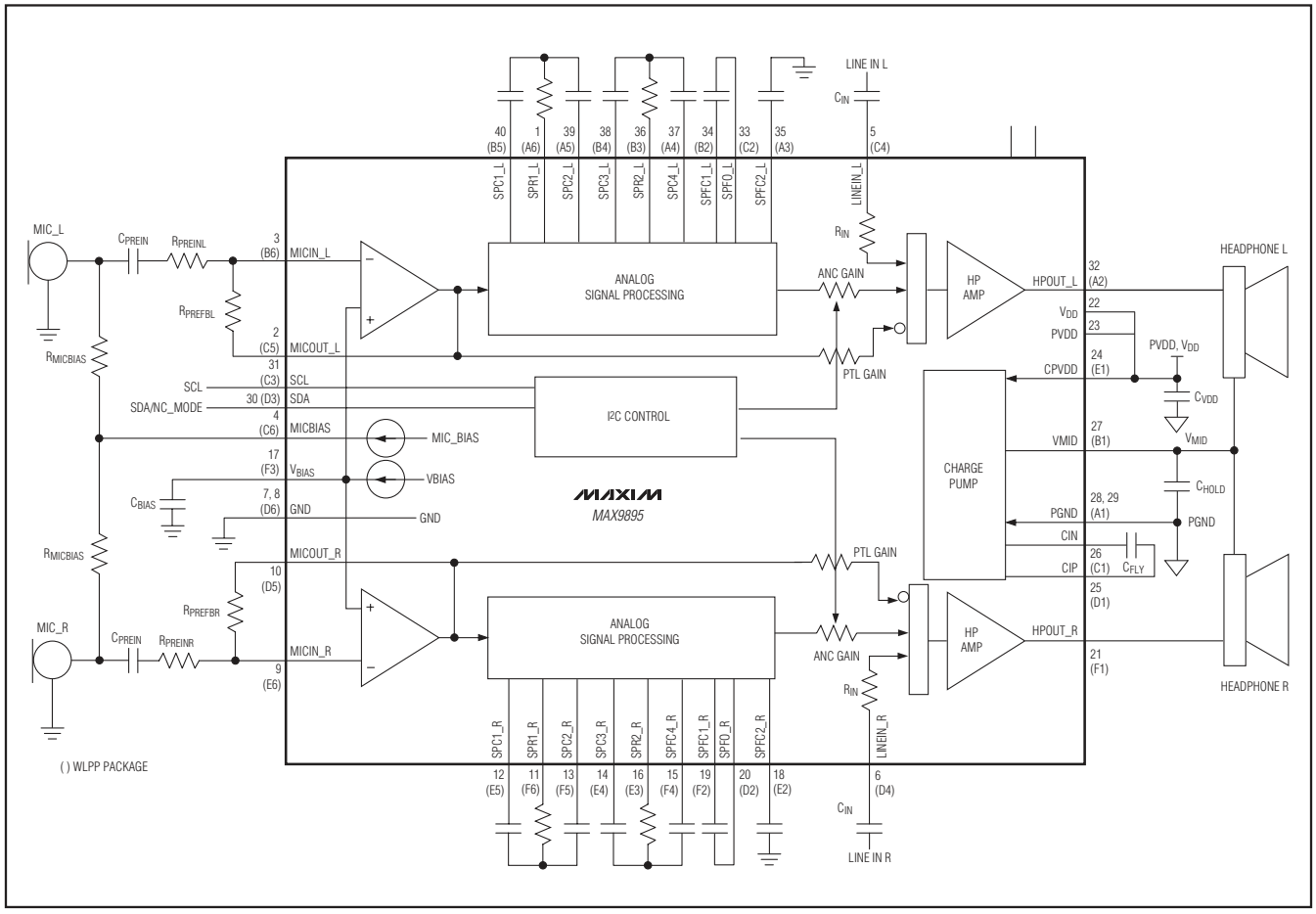
## Table 5. Mode Register 0x04

| BIT | NAME | POR | FUNCTION |
|---|---|---|---|
| 0 | $\overline{SHDN}$ | 0 | 0: Shut down<br>1: Play |
| 1 | ANC | 0 | 0: Noise cancelling on<br>1: Noise cancelling off (microphone muted) |
| 2 | PTL | 0 | 0: LINEIN routed to HPOUT<br>1: LINEIN attenuated; MICOUT routed to HPOUT |

## Table 6. Source Select

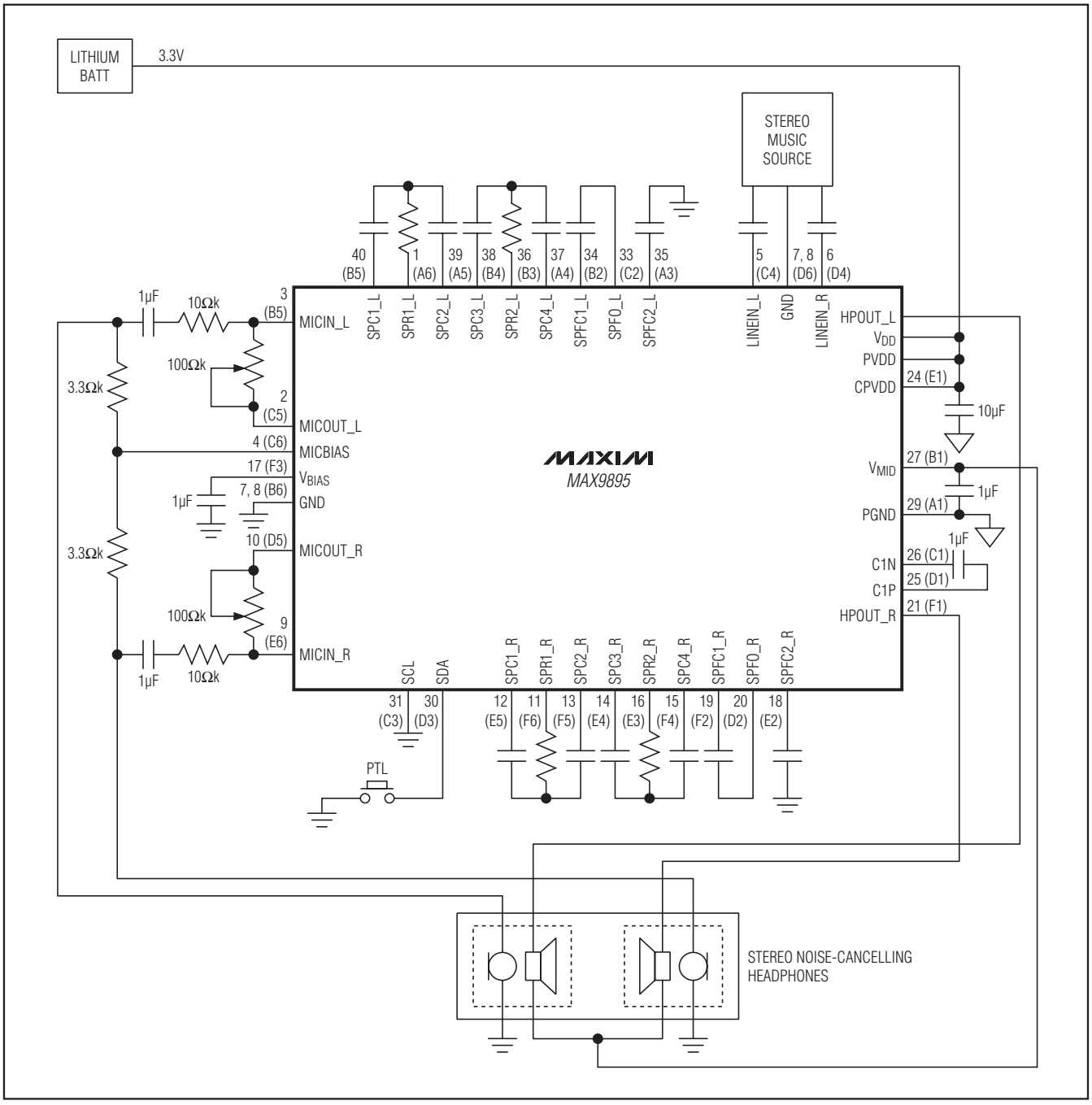
| INPUT | MODE | | |
|---|---|---|---|
| | ANC ON | ANC OFF | PTL |
| Microphone In | NC mode, inverting, gain defined by I²C REG 01 and 02 | Muted | Noninverting, gain defined by I²C REG 03 and 04 |
| Line In | Noninverting, 0db | Noninverting, 0dB | Attenuated |

## Functional Diagram/Typical Applications Circuit



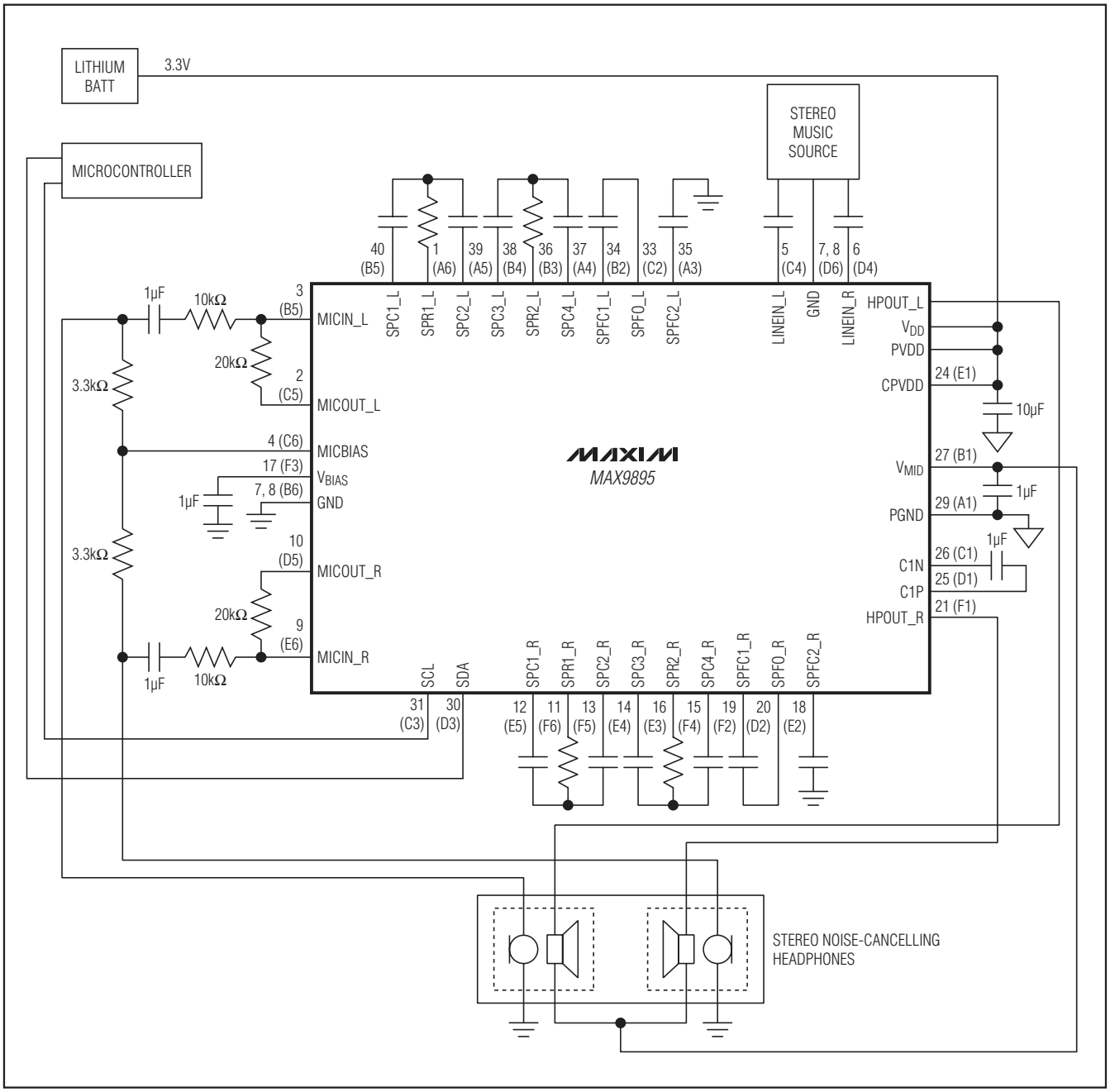
# Active Noise-Cancelling Solution for Stereo Headsets

## Typical Applications Circuit (Hardware Mode)



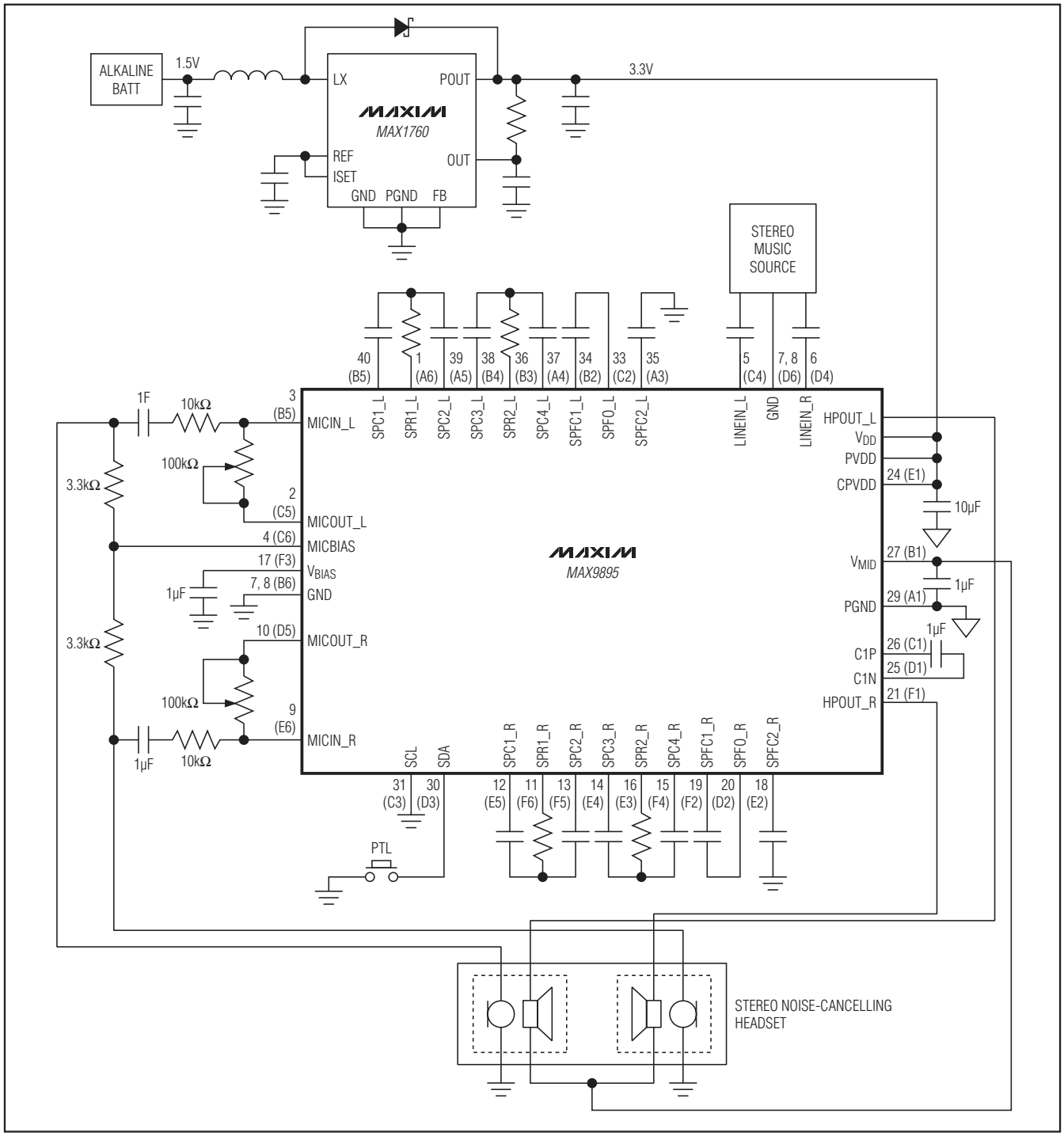
# Active Noise-Cancelling Solution for Stereo Headsets

## Typical Applications Circuit (Software Mode)



# Active Noise-Cancelling Solution for Stereo Headsets

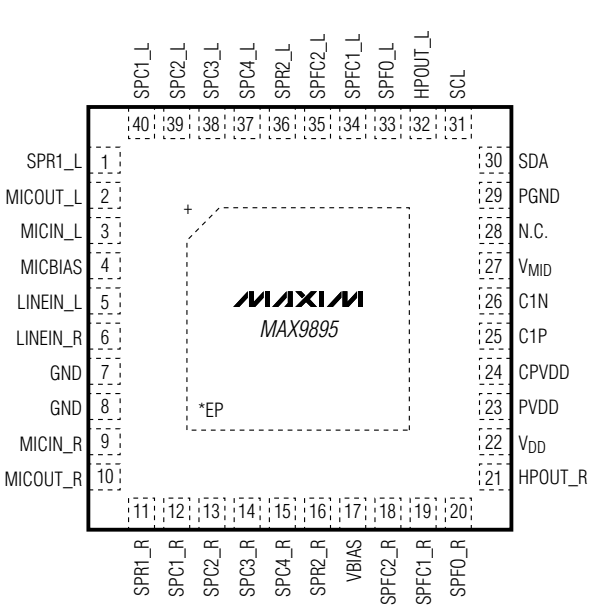
## Typical Applications Circuit (AAA Battery, Hardware Mode)



# Active Noise-Cancelling Solution for Stereo Headsets

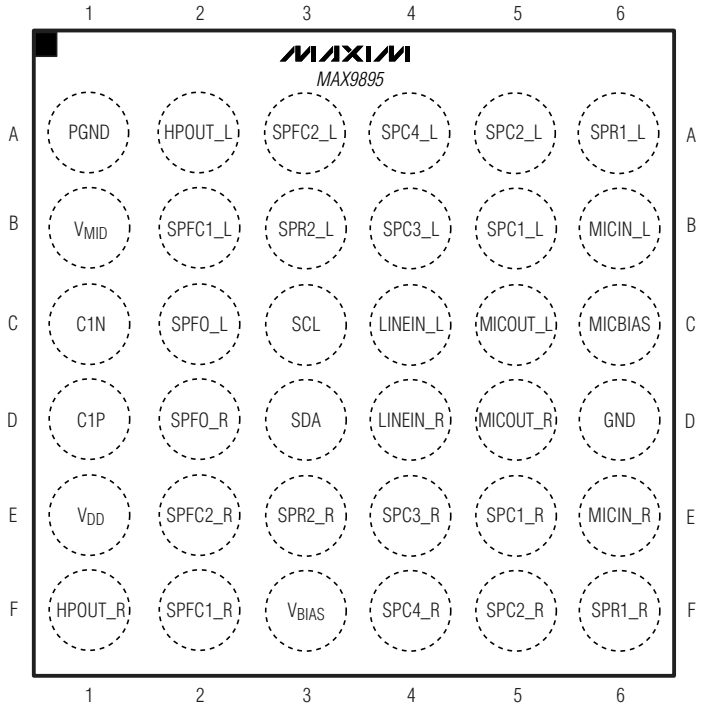
## Pin Configurations

TOP VIEW




**TQFN-EP**
**5mm x 5mm**

TOP VIEW
(BUMPS ON BOTTOM)




**WLP (0.4mm pitch)**
**2.54mm x 2.54mm**

*EP = EXPOSED PAD; CONNECT TO PGND.

## Chip Information

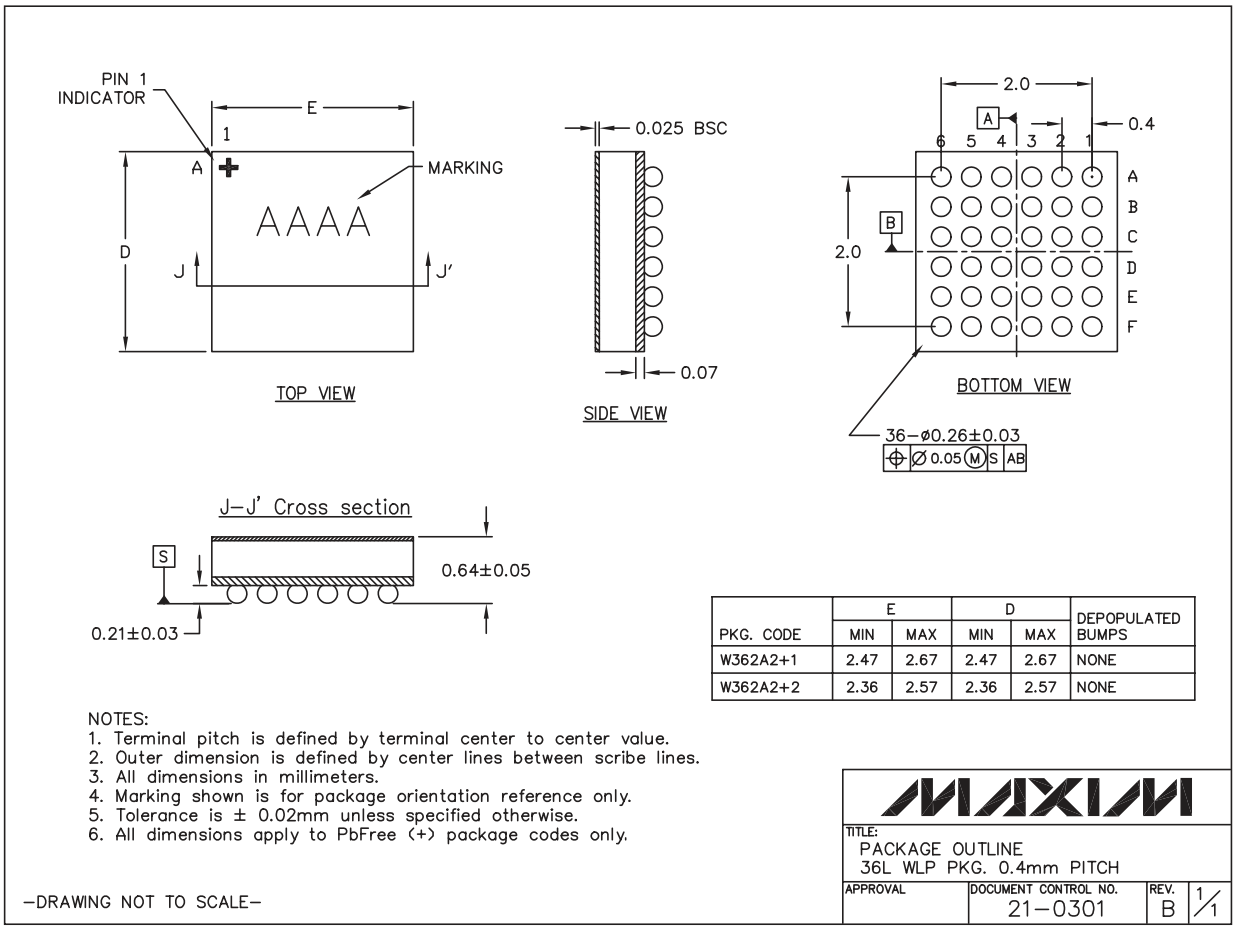
PROCESS: BiCMOS

# Active Noise-Cancelling Solution for Stereo Headsets

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 36 WLP | W362A2+2 | 21-0301 |
| 40 TQFN | T4055+1 | 21-0140 |




| PKG. CODE | E MIN | E MAX | D MIN | D MAX | DEPOPULATED BUMPS |
|---|---|---|---|---|---|
| W362A2+1 | 2.47 | 2.67 | 2.47 | 2.67 | NONE |
| W362A2+2 | 2.36 | 2.57 | 2.36 | 2.57 | NONE |

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.

-DRAWING NOT TO SCALE-

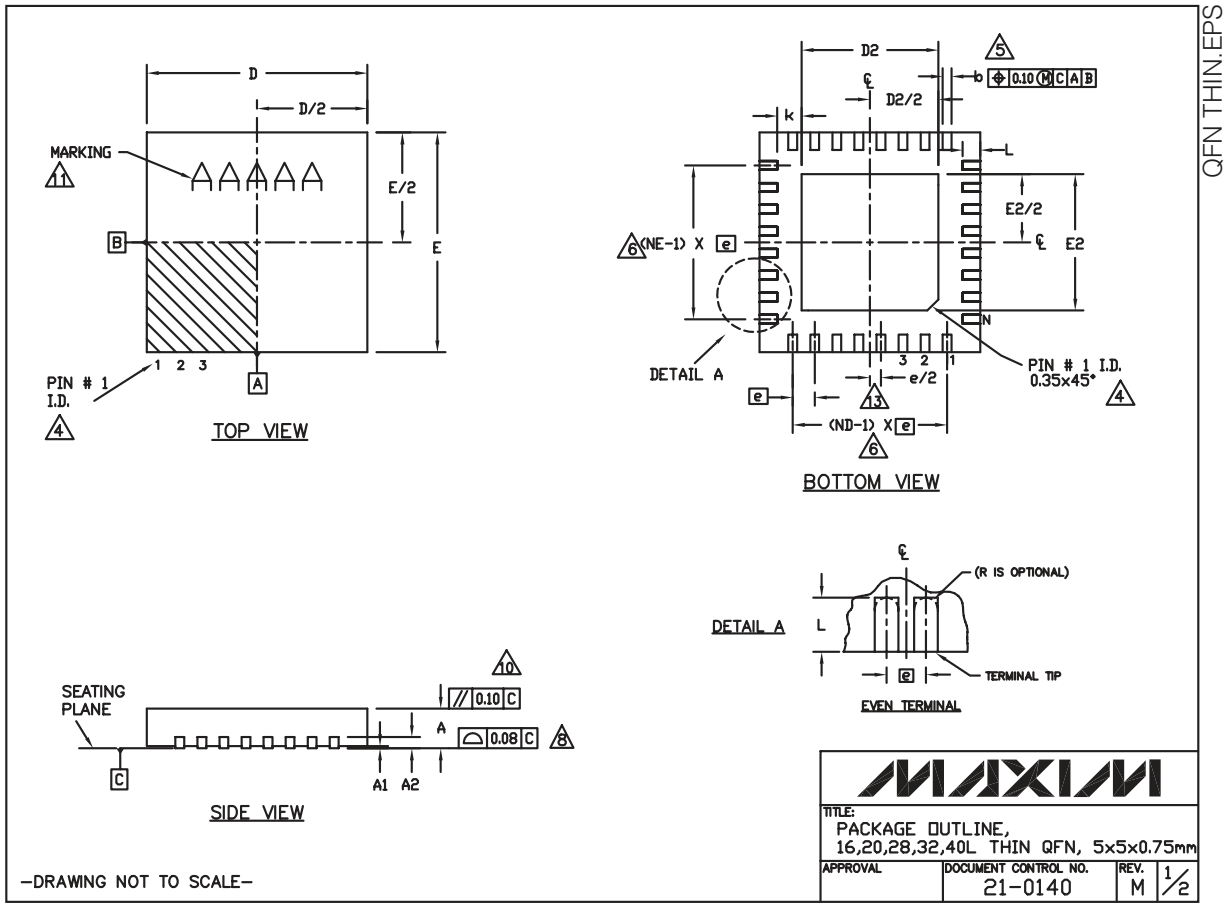
MAXIM

TITLE:
PACKAGE OUTLINE
36L WLP PKG. 0.4mm PITCH

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0301 | B | 1/1 |

## Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



# Active Noise-Cancelling Solution for Stereo Headsets

## Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

**COMMON DIMENSIONS**

| PKG. | 16L 5x5 | | | 20L 5x5 | | | 28L 5x5 | | | 32L 5x5 | | | 40L 5x5 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 |
| N | 16 | | | 20 | | | 28 | | | 32 | | | 40 | | |
| ND | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | |
| NE | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | |
| JEDEC | WHHB | | | WHHC | | | WHHD-1 | | | WHHD-2 | | | ----- | | |

**EXPOSED PAD VARIATIONS**

| PKG. CODES | D2 | | | E2 | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1655-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-4 | 2.19 | 2.29 | 2.39 | 2.19 | 2.29 | 2.39 |
| T165N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2055MN-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-3 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-4 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-6 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-7 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-8 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855N-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T3255-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255M-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-5 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T4055-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055-2 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055N-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055MN-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0140 | M | 2/2 |