

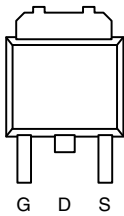
P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 40	0.005 at $V_{GS} = - 10$ V	- 110	185 nC

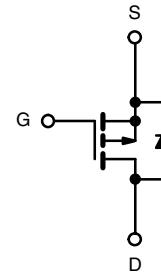
FEATURES

- TrenchFET[®] Power MOSFET


**RoHS
COMPLIANT**
TO-263


Top View

Drain Connected to Tab



P-Channel MOSFET

Ordering Information: SUM110P04-05-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	- 40	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 175$ °C)	$T_C = 25$ °C	- 110 ^a	A	
	$T_C = 70$ °C	- 110 ^a		
	$T_A = 25$ °C	39 ^{b, c}		
	$T_A = 70$ °C	33 ^{b, c}		
Pulsed Drain Current	I_{DM}	240		
Continuous Source-Drain Diode Current	$T_C = 25$ °C	110		
	$T_A = 25$ °C	10 ^{b, c}		
Avalanche Current	$L = 0.1$ mH	I_{AS}	75	
Single-Pulse Avalanche Energy		E_{AS}	281	mJ
Maximum Power Dissipation	$T_C = 25$ °C	P_D	375	W
	$T_C = 70$ °C		262	
	$T_A = 25$ °C		15 ^{b, c}	
	$T_A = 70$ °C		10.5 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	8	10	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	0.33	0.4	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

 c. $t = 10$ s.

d. Maximum under Steady State conditions is 40 °C/W.

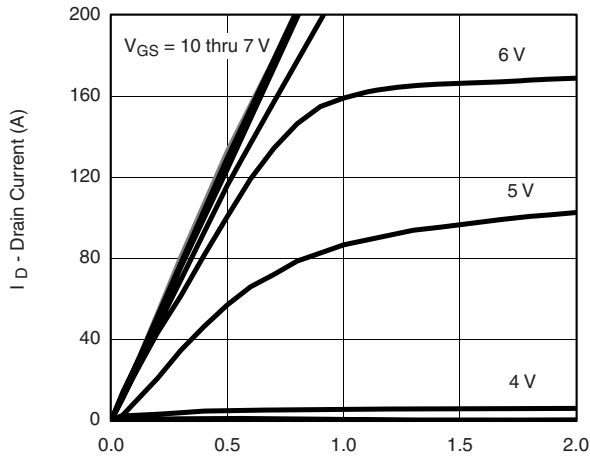


SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-40		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-2	-3	-4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$	-120			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -20\text{ A}$		0.0041	0.005	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -20\text{ A}$		75		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		11300		pF
Output Capacitance	C_{oss}			1510		
Reverse Transfer Capacitance	C_{rss}			1000		
Total Gate Charge	Q_g	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -110\text{ A}$		185	280	nC
Gate-Source Charge	Q_{gs}			48		
Gate-Drain Charge	Q_{gd}			42		
Gate Resistance	R_g	$f = 1\text{ MHz}$		4.0		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 0.18\text{ }\Omega$ $I_D \cong -110\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		25	40	ns
Rise Time	t_r			290	440	
Turn-Off Delay Time	$t_{d(off)}$			110	165	
Fall Time	t_f			35	55	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-110	A
Pulse Diode Forward Current ^a	I_{SM}				-240	
Body Diode Voltage	V_{SD}	$I_S = -20\text{ A}$		-0.8	-1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		70	105	ns
Body Diode Reverse Recovery Charge	Q_{rr}			130	200	nC
Reverse Recovery Fall Time	t_a			37		ns
Reverse Recovery Rise Time	t_b			33		

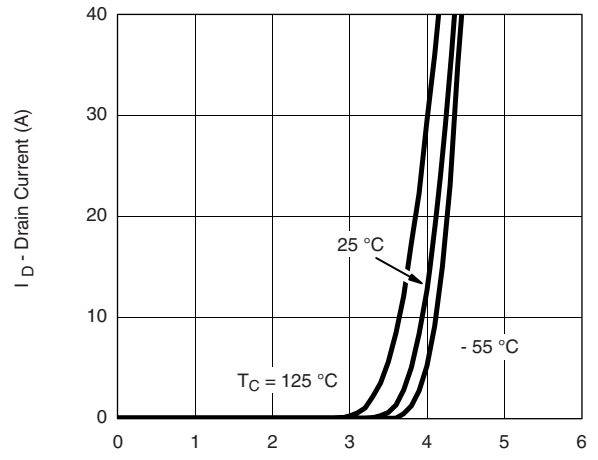
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

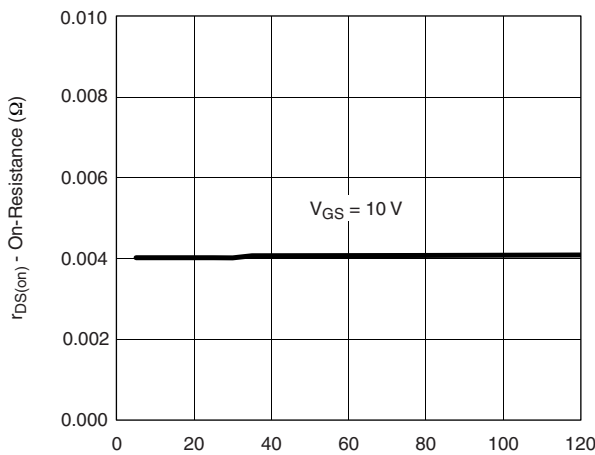
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


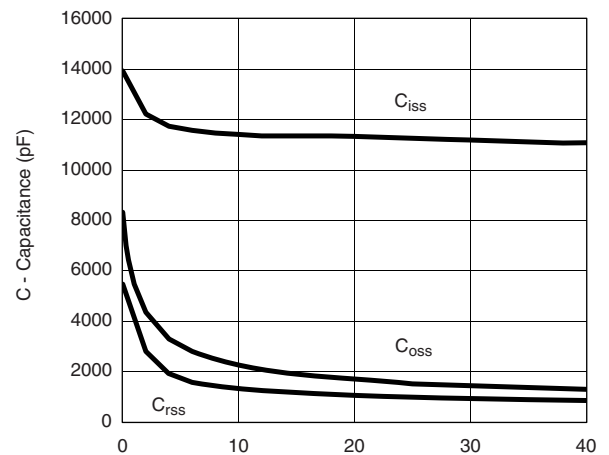
V_{GS} - Drain-to-Source Voltage (V)
Output Characteristics



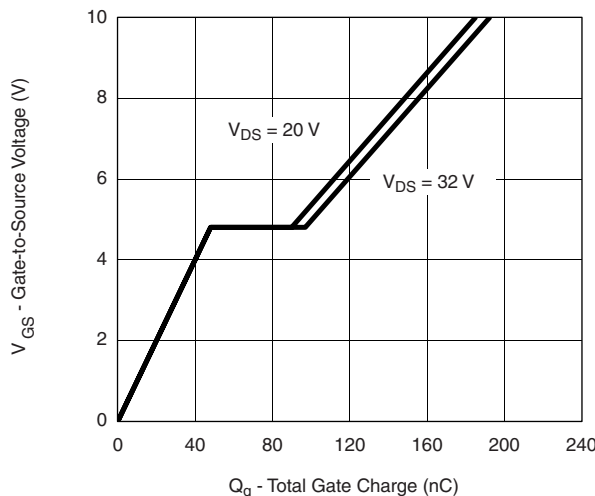
$T_C = 125^\circ\text{C}$
 25°C
 -55°C
 V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



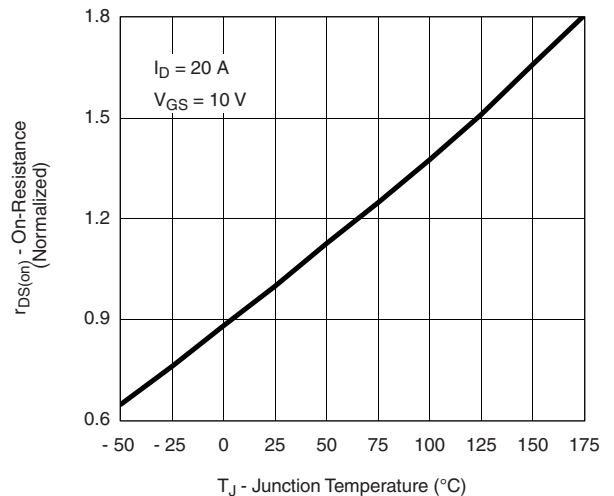
$r_{DS(on)}$ - On-Resistance (Ω)
 $V_{GS} = 10\text{ V}$
 I_D - Drain Current (A)
On-Resistance vs. Drain Current



C_{iss}
 C_{oss}
 C_{rss}
 V_{DS} - Drain-to-Source Voltage (V)
Capacitance

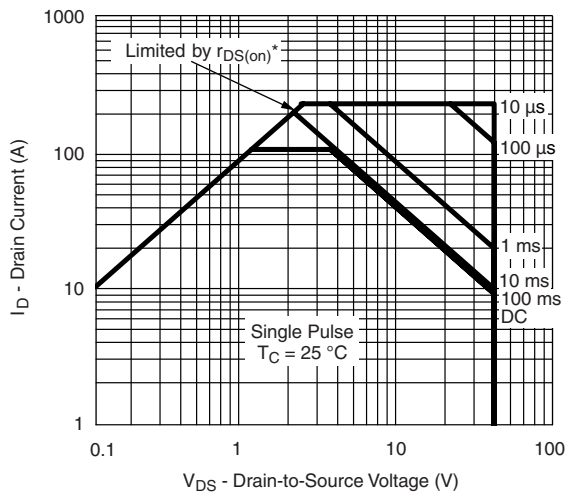
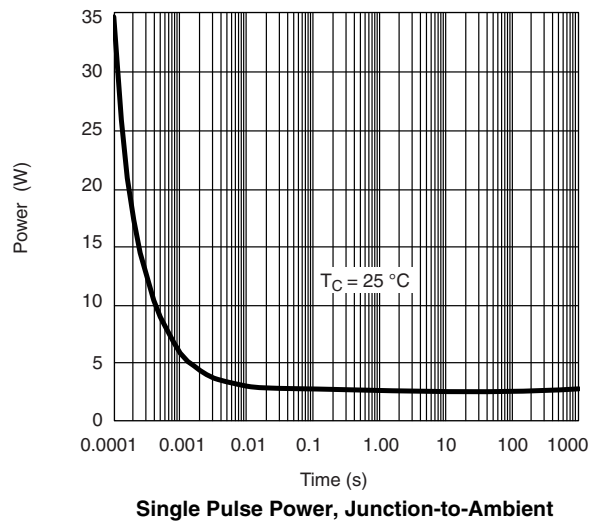
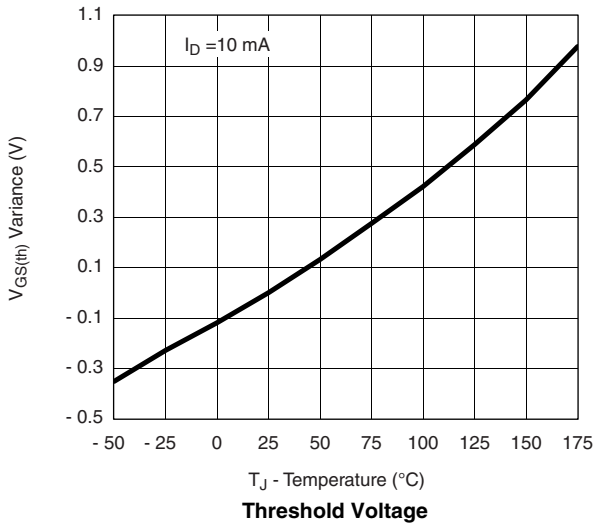
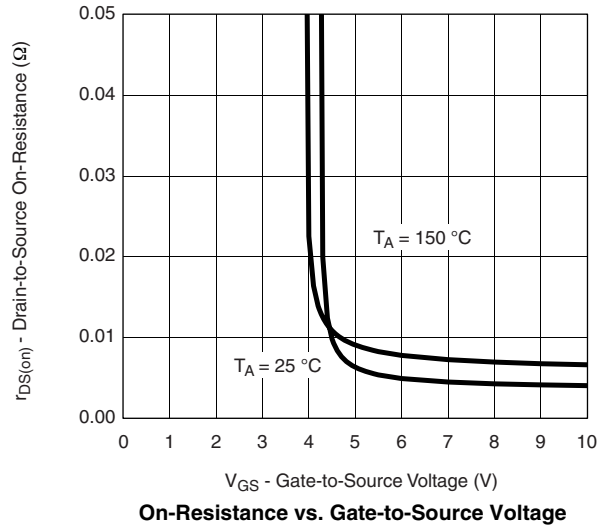
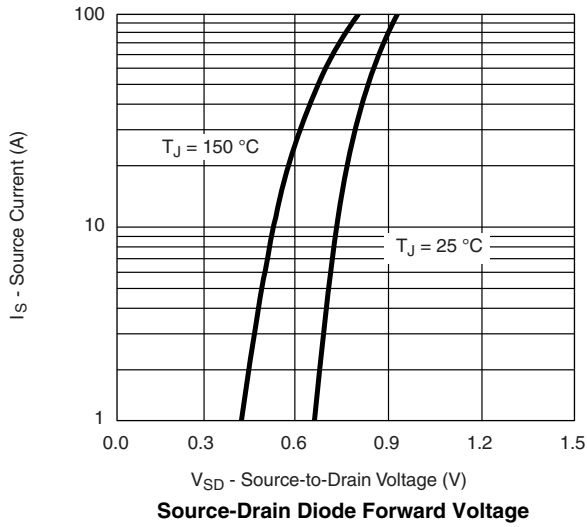


V_{GS} - Gate-to-Source Voltage (V)
 Q_g - Total Gate Charge (nC)
Gate Charge



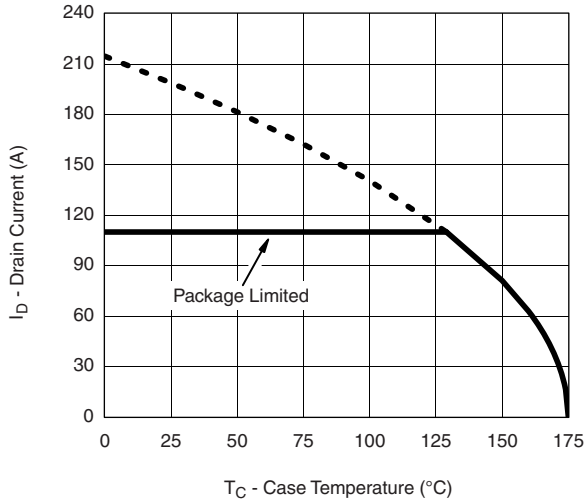
$r_{DS(on)}$ - On-Resistance (Normalized)
 T_J - Junction Temperature ($^\circ\text{C}$)
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

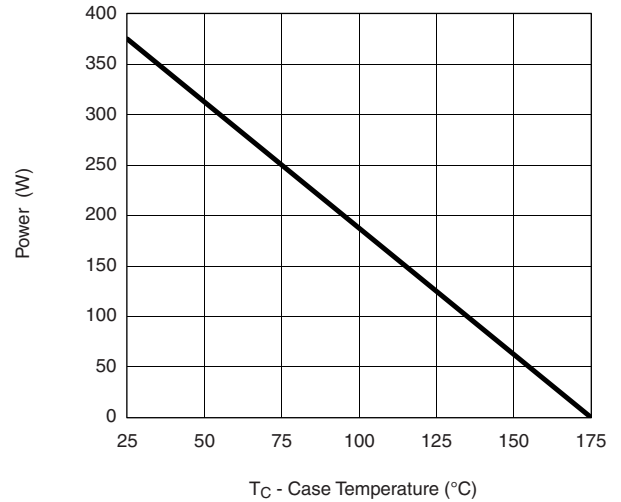


* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

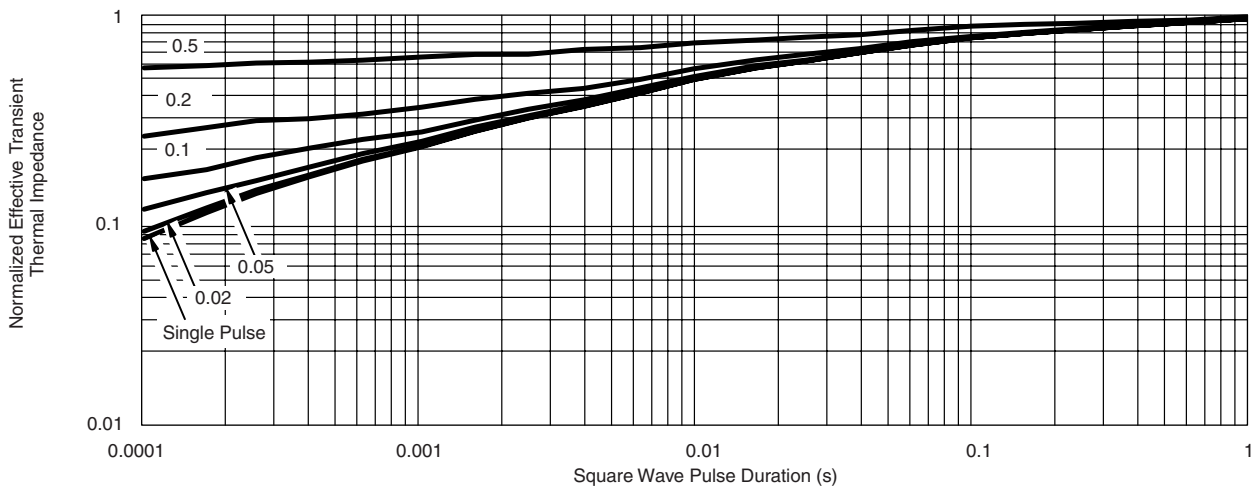
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Max. Avalanche and Drain Current vs. Case Temperature*



Power Derating, Junction-to-Case

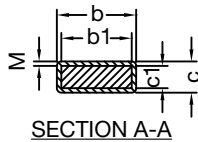
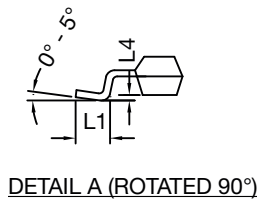
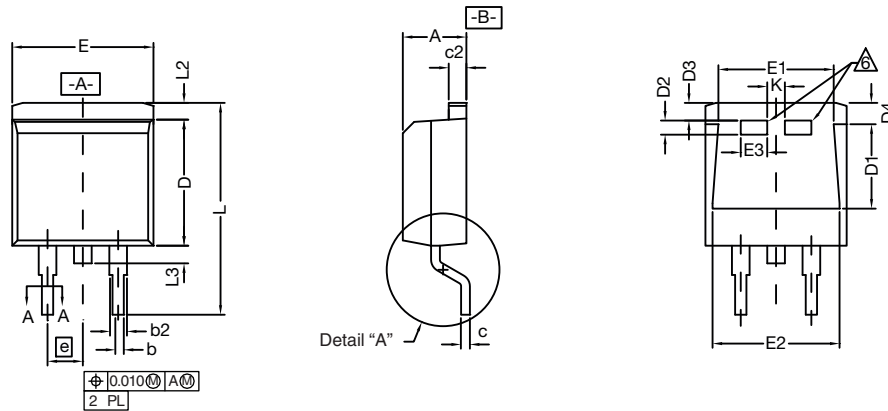


Normalized Thermal Transient Impedance, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)} = 175\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper power dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TO-263 (D²PAK): 3-LEAD



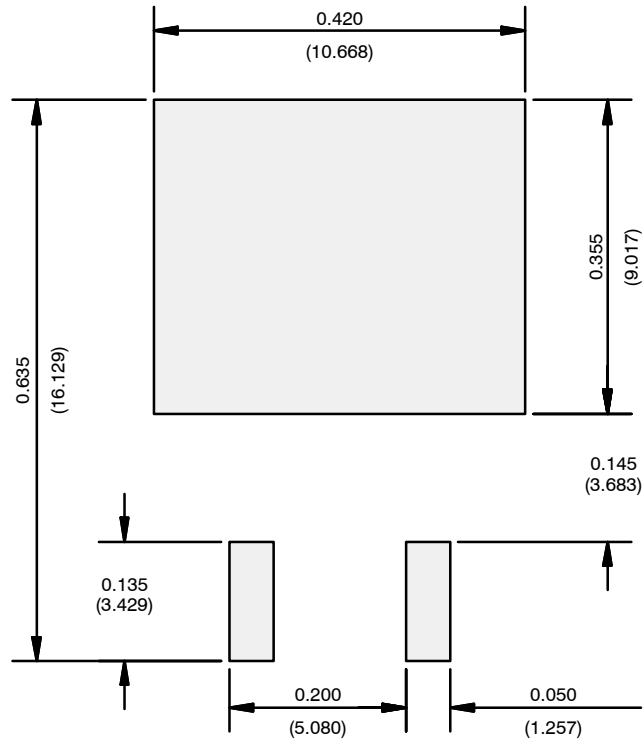
DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	

ECN: T13-0707-Rev. K, 30-Sep-13
DWG: 5843

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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