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1. GENERAL DESCRIPTION

The Winbond 128Mb Low Power SDRAM is a low power synchronous memory containing 134,217,728 memory cells fabricated with Winbond high performance process technology.

It is designed to consume less power than the ordinary SDRAM with low power features essential for applications which use batteries. It is available in two organizations: 1,048,576 words × 4 banks × 32 bits or 2,097,152 words × 4 banks × 16 bits. The device operates in a fully synchronous mode, and the output data are synchronized to positive edges of the system clock and is capable of delivering data at clock rate up to 166MHz. The device supports special low power functions such as Partial Array Self Refresh (PASR) and Automatic Temperature Compensated Self Refresh (ATCSR).

The Low Power SDRAM is suitable for 2.5G / 3G cellular phone, PDA, digital still camera, mobile game consoles and other handheld applications where large memory density and low power consumption are required. The device operates from 1.8V power supply, and supports the 1.8V LVCMOS bus interface.

2. FEATURES

- Power supply V_{DD} = 1.7V~1.95V
- V_{DDQ} = 1.7V~1.95V
- Frequency : 166MHz (-6) ,133MHz(-75)
- Programmable Partial Array Self Refresh
- Power Down Mode
- Deep Power Down Mode (DPD)
- Programmable output buffer driver strength
- Automatic Temperature Compensated Self Refresh

- $\overline{CAS}$ Latency: 2 and 3
- Burst Length: 1, 2, 4, 8, and full page
- Refresh: 4K refresh cycle / 64ms
- Interface: LVCMOS
- Support package :

  54 balls VFBGA (x16)
  90 balls VFBGA (x32)
- Operating Temperature Range

  Extended (-25°C ~ +85°C)

  Industrial (-40°C ~ +85°C)

3. PIN CONFIGURATION

3.1 Ball Assignment: LPSDR X 16

54Ball FBGA									
	1	2	3	4	5	6	7	8	9
A	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ				VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ				VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ				VSSQ	DQ6	DQ5
E	DQ8	NC	VSS				VDD	LDQM	DQ7
F	UDQM	CLK	CKE				$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	NC	A11	A9				BA0	BA1	$\overline{CS}$
H	A8	A7	A6				A0	A1	A10
J	VSS	A5	A4				A3	A2	VDD

(Top View)

3.2 Ball Assignment: LPSDR X 32

90Ball FBGA									
	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	VSS				VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ				VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25				DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30				DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC				NC	DQ16	VSSQ
F	VSS	DQM3	A3				A2	DQM2	VDD
G	A4	A5	A6				A10	A0	A1
H	A7	A8	NC				NC	BA1	A11
J	CLK	CKE	A9				BA0	$\overline{CS}$	$\overline{RAS}$
K	DQM1	NC	NC				$\overline{CAS}$	$\overline{WE}$	DQM0
L	VDDQ	DQ8	VSS				VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9				DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14				DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ				VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS				VDD	DQ0	DQ2

(Top View)

4. PIN DESCRIPTION

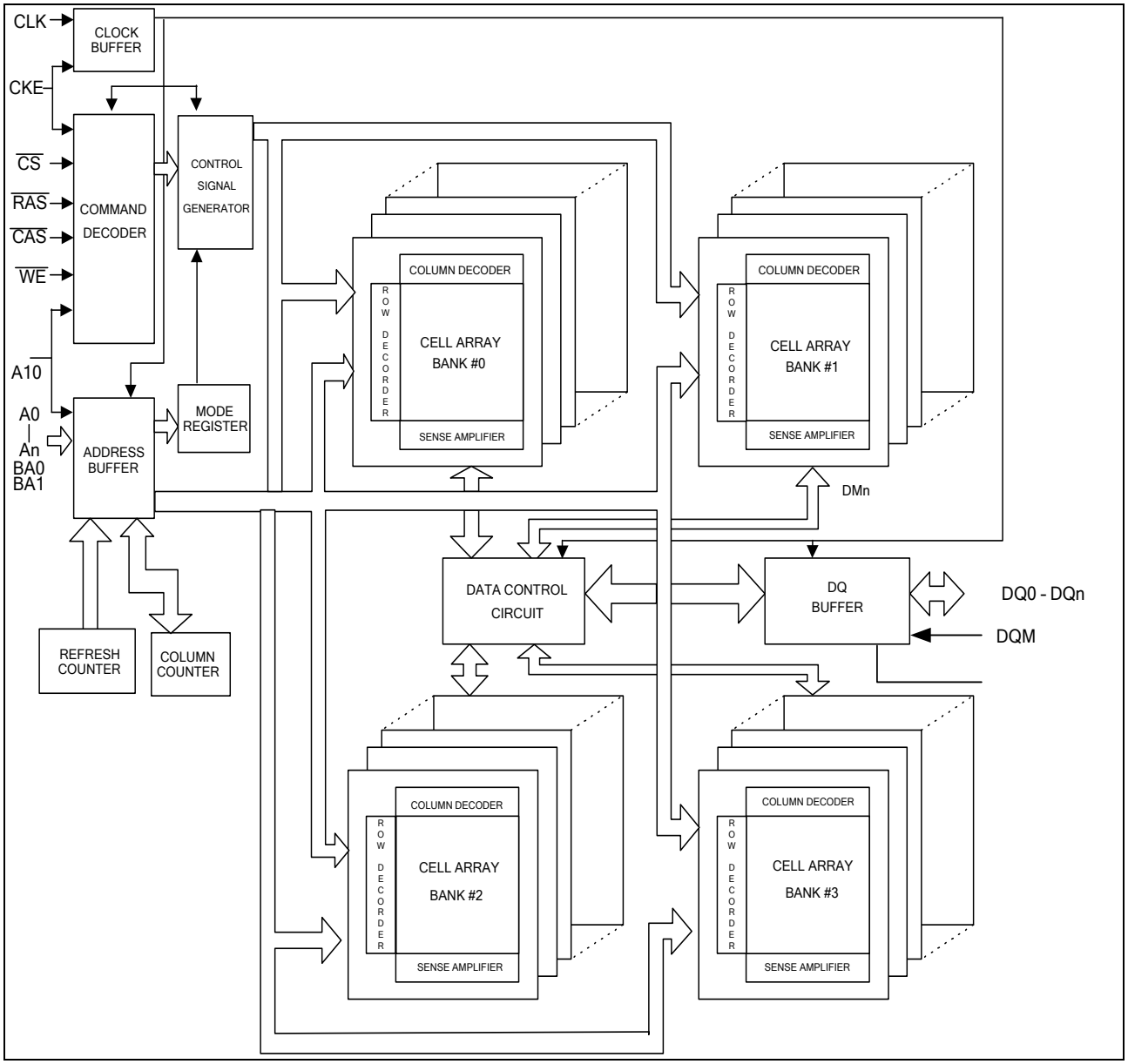
4.1 Signal Description

BALL NAME	FUNCTION	DESCRIPTION
A [n : 0]	Address	Multiplexed pins for row and column address. A10 is Auto Precharge Select
BA0, BA1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during address latch time.
DQ0~DQ15 (×16) DQ0~DQ31 (×32)	Data Input/ Output	Multiplexed pins for data output and input.
$\overline{CS}$	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
$\overline{RAS}$	Row Address Strobe	Command input. When sampled at the rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed.
$\overline{CAS}$	Column Address Strobe	Referred to $\overline{RAS}$
$\overline{WE}$	Write Enable	Referred to $\overline{WE}$
UDQM / LDQM(x16) DQM0 ~ DQM3 (x32)	I/O Mask	The output buffer is placed at Hi-Z (with latency of 2 in CL=2, 3;) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency
CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode or Self Refresh mode is entered.
VDD	Power	Power supply for input buffers and logic circuit inside DRAM.
VSS	Ground	Ground for input buffers and logic circuit inside DRAM.
VDDQ	Power for I/O Buffer	Power supply separated from VDD, used for output buffers to improve noise.
VSSQ	Ground for I/O Buffer	Separated ground from VSS, used for output buffers to improve noise.
NC	No Connection	No connection

4.2 Addressing Table

ITEM		128 Mb
Number of banks		4
Bank address pins		BA0,BA1
Auto precharge pin		A10/AP
X16	Row addresses	A0-A11
	Column addresses	A0-A8
	Refresh count	4K
x32	Row addresses	A0-A11
	Column addresses	A0-A7
	Refresh count	4K

5. BLOCK DIAGRAM



6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUES		UNITS
		MIN	MAX	
Voltage on VDD relative to VSS	VDD	−0.3	2.7	V
Voltage on VDDQ relative to VSS	VDDQ	−0.3	2.7	V
Voltage on any pin relative to VSS	VIN, VOUT	−0.3	2.7	V
Operating Temperature	Tc	-25 -40	85 85	°C
Storage Temperature	TSTG	−55	150	°C
Short Circuit Output Current	IOUT		±50	mA
Power Dissipation	PD		1.0	W

6.2 Operating Conditions

(Notes : 1)

PARAMETER	SYMBOL	MIN.	TYP.	MA X.	UNIT
Supply Voltage	VDD	1.7	1.8	1.95	V
Supply Voltage (for I/O Buffer)	VDDQ	1.7	1.8	1.95	V
Input High level Voltage	VIH	0.8*VDDQ	-	VDDQ + 0.3	V
Input Low level Voltage	VIL	-0.3	-	+0.3	V
LVCOMS Output "H" Level Voltage (IOUT = -0.1 mA)	VOH	0.9*VDDQ	-	-	V
LVCMOS Output "L" Level Voltage (IOUT = +0.1 mA)	VOL	-	-	0.2	V
Input Leakage Current (0V ≤ VIN ≤ VDD, all other pins not under test = 0V)	II(L)	-1	-	1	μA
Output Leakage Current (Output disable , 0V ≤ VOUT ≤ VDDQ)	IO(L)	-5	-	5	μA

Note: V_{IH}(max) = V_{DD}/ V_{DDQ}+1.2V for pulse width ≤ 5 ns , V_{IL}(min) = V_{SS}/ V_{SSQ}-1.2V for pulse width ≤ 5 ns

6.3 Capacitance

(V_{DD} = 1.7V~1.9V, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance : All other input-only	CI	1.5	3.0	pf
Input Capacitance (CLK)	CCLK	1.5	3.5	pf
Input/Output capacitance	CIO	3.0	5.0	pf

Note: These parameters are periodically sampled and not 100% tested.

6.4 DC Characteristics

(X16)

PARAMETER / CONDITION	SYM.		-6 MAX.	-75 MAX.	UNIT	NOTES
Operating current: Active mode, 1 bank, BL = 1, tRC = tRC (min), Iout=0mA, Active Precharge command cycling without burst operation.	IDD1		38	35	mA	2, 3, 4
Standby current: Power-down mode, All banks idle, CKE = LOW.	Idd2P	Low power	0.23	0.23	mA	5
		Normal power	0.28	0.28		
Standby current: Nonpower-down mode, All banks idle, CKE = HIGH.	Idd2N		10	10	mA	
Standby current: Active mode; CKE = LOW, CS# = HIGH, All banks active, No accesses in progress.	Idd3P		3	3	mA	3, 4, 6
Standby current: Active mode, CKE = HIGH, CS# = HIGH, All banks active after tRCD met, No accesses in progress.	Idd3N		20	15	mA	3, 4, 6
Operating current: Burst mode, All banks active, Iout=0mA, READ/WRITE command cycling,	Idd4		75	70	mA	2, 3, 4
Auto refresh current: tRFC=tRFC (MIN), Auto refresh command cycling	Idd5		50	50	mA	2, 3, 4, 6
Deep Power Down Mode	Izz		10	10	µA	5,8

(X32)

PARAMETER / CONDITION	SYM.		-6 MAX.	-75 MAX.	UNIT	NOTES
Operating current: Active mode, 1 bank, BL = 1, tRC = tRC (min), Iout=0mA, Active Precharge command cycling without burst operation.	IDD1		38	35	mA	2, 3, 4
Standby current: Power-down mode, All banks idle, CKE = LOW.	Idd2P	Low power	0.23	0.23	mA	5
		Normal power	0.28	0.28		
Standby current: Nonpower-down mode, All banks idle, CKE = HIGH.	Idd2N		10	10	mA	
Standby current: Active mode; CKE = LOW, CS# = HIGH, All banks active, No accesses in progress.	Idd3P		3	3	mA	3, 4, 6
Standby current: Active mode, CKE = HIGH, CS# = HIGH, All banks active after tRCD met, No accesses in progress.	Idd3N		20	15	mA	3, 4, 6
Operating current: Burst mode, All banks active, Iout=0mA, READ/WRITE command cycling,	Idd4		75	70	mA	2, 3, 4
Operating current: Active mode, 1 bank, BL = 1, tRC = tRC (min), Iout=0mA, Active Precharge command cycling without burst operation.	Idd5		50	50	mA	2, 3, 4, 6
Standby current: Power-down mode, All banks idle, CKE = LOW.	Izz		10	10	µA	5,8

Notes:

1. A full initialization sequence is required before proper device operation is ensured.
2. Idd is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
3. The Idd current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every 2 clocks.
5. Measurement is taken 500ms after entering into this operating mode to provide tester measuring unit settling time.
6. Other input signals can transition only one time for every 2 clocks and are otherwise at valid Vih or Vil levels.
7. CKE is HIGH during the REFRESH command period tRFC (MIN) else CKE is LOW. The Idd7 limit is a nominal value and does not result in a fail value.
8. Typical values at 25°C (not a maximum value).

6.5 Automatic Temperature Compensated Self Refresh Current Feature

IDD6	Low Power		Normal Power		Units
TCSR Range	45℃	85℃	45℃	85℃	uA
Full Array	180	230	220	280	
1/2 Array	160	200	190	250	
1/4 Array	150	180	170	230	

Note:

1. A full initialization sequence is required before proper device operation is ensured.
2. Measurement is taken 500ms after entering into this operating mode to provide tester measuring unit settling time.
3. Enables on-die refresh and address counters.
4. Values for Idd6 85°C full array and partial array are guaranteed for the entire temperature range.
5. IDD6 is typical value.

6.6 AC Characteristics And AC Operating Conditions

6.6.1 AC Characteristics

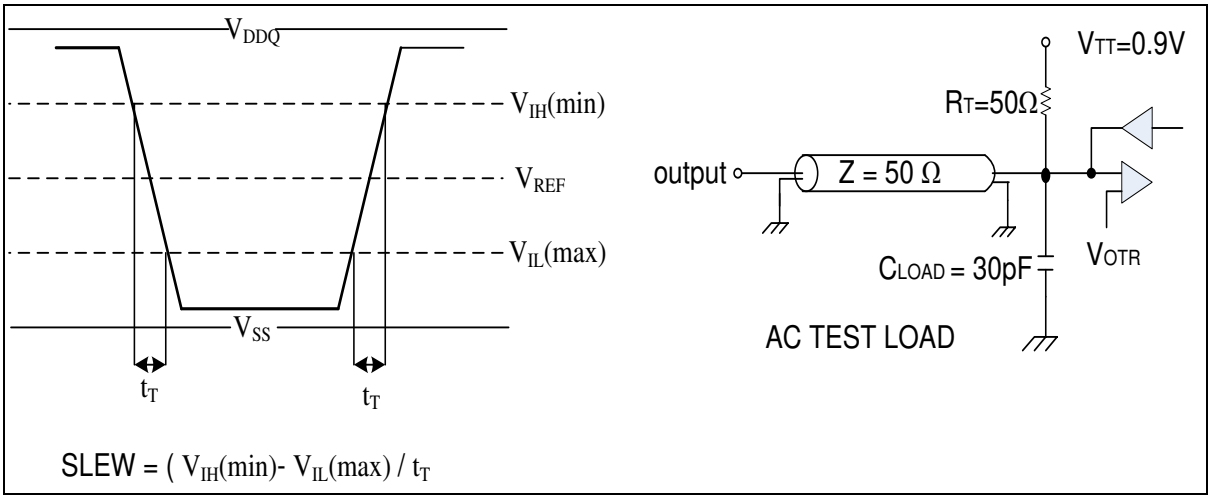
*CL= $\overline{CAS}$ Latency; (Notes: 5,6,7)

PARAMETER		SYM	-6		-75		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Ref/Active to Ref/Active Command Period		tRC	60		72.5	-	ns	8
Active to precharge Command Period		tRAS	42	100000	50	100000	ns	8
Active to Read/Write Command Delay Time		tRCD	18		18	-	ns	8
Read/Write(a) to Read/Write(b)Command Period		tCCD	1		1	-	CLK	8
Precharge to Active Command Period		tRP	18		18	-	ns	8
Active(a) to Active(b) Command Period		tRRD	12		15	-	ns	8
Write Recovery Time		tWR	15		15	-	ns	
Write-Recovery Time (Last data to Read)		tLDR	1		1		CLK	
CLK Cycle Time	CL * = 3	tCK	6	1000	7.5	1000	ns	
	CL * = 2		12	1000	12	1000	ns	
CLK High Level width		tCH	2		2.5	-	ns	
CLK Low Level width		tCL	2		2.5	-	ns	
Access Time from CLK	CL * = 3	tAC		5.4	-	5.4	ns	
	CL * = 2			6	-	8	ns	
Output Data Hold Time		tOH	2.5		2.5	-	ns	
Output Data High Impedance Time	CL * = 3	tHZ		5.4	-	5.4	ns	7
	CL * = 2			6	-	6	ns	7
Output Data Low Impedance Time		tLZ	1		1	-	ns	
Power Down Mode Entry Time		tSB	0	6	0	7.5	ns	
Transition Time of CLK (Rise and Fall)		tT	0.3	1	0.3	1.2	ns	
Data-in Set-up Time		tDS	1.5		1.5	-	ns	
Data-in Hold Time		tDH	1		1	-	ns	
Address Set-up Time		tAS	1.5		1.5	-	ns	
Address Hold Time		tAH	1		1	-	ns	
CKE Set-up Time		tCKS	1.5		1.5	-	ns	
CKE Hold Time		tCKH	1		1	-	ns	
Command Set-up Time		tCMS	1.5		1.5	-	ns	

PARAMETER		SYM	-6		-75		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Command Hold Time		tCMH	1		1	-	ns	
Refresh Time		tREF		64		64	ms	
Mode register Set Cycle Time		tRSC	12		15	-	ns	8
Ref to Ref/Active Command period		tRFC	72		72	-	ns	
Self Refresh exit to next valid command delay		tXSR	115		115	-	ns	

6.6.2 AC Test Condition

SYMBOL	PARAMETER	VALUE	UNIT
VIH(min)	Input High Voltage Level (AC)	0.8 x VDDQ	V
VIL(max)	Input Low Voltage Level (AC)	0.2 x VDDQ	V
VREF	Input Signal Reference Level	0.5 x VDDQ	V
VOTR	Output Signal Reference Level	0.5 x VDDQ	V
SLEW	Input Signal Slew Rate	1	V/ns



Transition times are measured between VIH and VIL.

Note :
1. Conditions outside the limits listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may affect deice reliability.
2. All voltages are referenced to VSS and VSSQ.
3. These parameters depend on the cycle rate. These values are measured at a cycle rate with the minimum values of tCK and tRC . Input signals transition once per tCK period.
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. Power-up sequence is described in Note 9.
6. AC TEST CONDITIONS : (refer to 6.6.2)
7. tHZ defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
8. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows: The number of clock cycles = specified value of timing / clock period (count fractions as a whole number)
9. Power up Sequence : The SDRAM should be powered up by the following sequence of operations.
   a. Power must be applied to VDD before or at the seme time as VDDQ while all input signals are held in the “NOP” state. The CLK signal will be applied at power up with power.
   b. After power-up a pause of at least 200 uA is required. It is required that DQM and CKE signals must be held “High” (VDD levels) to ensure that the DQ output is in High-impedance state.
   c. All banks must be precharged.
   d. The Mode Register Set command must be issued to initialize the Mode Register.
   e. The Extended Mode Register Set command must be issued to initialize the Extended Mode Register.
   f. Issue two or more Auto Refresh dummy cycles to stabilize the internal circuitry of the device.

The Mode Register Set command can be invoked either before or after the Auto Refresh dummy cycles.

6.6.3 AC Latency Characteristics

CKE to clock disable (CKE Latency)		1	Cycle
DQM to output in High-Z (Read DQM Latency)		2	
DQM to input data delay (Write DQM Latency)		0	
Write command to input data (Write Data Latency)		0	
$\overline{CS}$ to Command input ($\overline{CS}$ Latency)		0	
Precharge to DQ Hi-Z Lead time	CL = 2	2	
	CL = 3	3	
Precharge to Last Valid data out	CL = 2	1	
	CL = 3	2	
Burst Stop Command to DQ Hi-Z Lead time	CL = 2	2	
	CL = 3	3	
Burst Stop Command to Last Valid data out	CL = 2	1	
	CL = 3	2	
Read with Auto Precharge Command to Active/Ref Command	CL = 2	BL+ tRP	Cycle + ns
	CL = 3	BL+ tRP	
Write with Auto Precharge Command to Active/Ref Command	CL = 2	BL+1 + tRP	
	CL = 3	BL+1 + tRP	

7. FUNCTION DESCRIPTION

7.1 Command Function

7.1.1Table 1. Truth Table

(Note (1) and (2))

Symbol	Command	Device State	CKEn-1	CKEn	DQM(5)	BS0, BS1	A10	An~A0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
ACT	Bank Activate	Idle (3)	H	X	X	V	V	V	L	L	H	H
PRE	Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
PREA	Precharge All	Any	H	X	X	X	H	X	L	L	H	L
WRIT	Write	Active (3)	H	X	X	V	L	V	L	H	L	L
WRITA	Write with Auto Precharge	Active (3)	H	X	X	V	H	V	L	H	L	L
READ	Read	Active (3)	H	X	X	V	L	V	L	H	L	H
READA	Read with Auto Precharge	Active (3)	H	X	X	V	H	V	L	H	L	H
MRS	Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
EMRS	Extended Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
NOP	No-Operation	Any	H	X	X	X	X	X	L	H	H	H
BST	Burst stop	Active (4)	H	X	X	X	X	X	L	H	H	L
DSL	Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AREF	Auto-Refresh	Idle	H	H	X	X	X	X	L	L	L	H
SELF	Self-Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SELEX	Self-Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
									L	H	H	H
CSE	Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
PD	Power Down Mode Entry	Idle/Active (6)	H	L	X	X	X	X	H	X	X	X
									L	H	H	H
CSEX	Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
PDEX	Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
DE	Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
DD	Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X
DPD	Deep Power Down Mode Entry	Idle	H	L	X	X	X	X	L	H	H	L
DPDE	Deep Power Down Mode Exit	Idle (DPD)	L	H	X	X	X	X	X	X	X	X

Note

1. V = Valid, × = Don't Care, L = Low level, H = High level
2. CKEn signal is input level when commands are issued.
   CKEn-1 signal is input level one clock cycle before the commands are issued.
3. These are state designated by the BS0, BS1 signals.
4. Device state is Full Page Burst operation.
5. x32: DQM0-3, x16 : LDQM / UDQM
6. Power Down Mode cannot entry in the burst cycle.

When this command assert in the burst cycle, device state is clock suspend mode.

7.1.2 Functional Truth Table

(See Note 1 at the end of this Table)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Idle	H	X	X	X	X	DSL	Nop	
	L	H	H	X	X	NOP/BST	Nop	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	Row activating	
	L	L	H	L	BS, A10	PRE/PREA	Nop	
	L	L	L	H	X	AREF/SELF	Refresh or Self refresh	2
	L	L	L	L	Op-Code	MRS/EMRS	Mode register accessing	2
Row active	H	X	X	X	X	DSL	Nop	
	L	H	H	X	X	NOP/BST	Nop	
	L	H	L	H	BS, CA, A10	READ/READA	Begin read: Determine AP	4
	L	H	L	L	BS, CA, A10	WRIT/WRITA	Begin write: Determine AP	4
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Precharge	5
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Burst stop	
	L	H	L	H	BS, CA, A10	READ/READA	Term burst, new read: Determine AP	6
	L	H	L	L	BS, CA, A10	WRIT/WRITA	Term burst, begin write: Determine AP	6,7
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Term burst, precharging	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write	H	X	X	X	X	DSL	Continue burst to end.	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Burst stop, row active	
	L	H	L	H	BS, CA, A10	READ/READA	Term burst, start read: Determine AP	6, 7
	L	H	L	L	BS, CA, A10	WRIT/WRITA	Term burst, new write: Determine AP	6
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Term burst. precharging	8
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Precharging	H	X	X	X	X	DSL	Nop → Idle after t_{RP}	
	L	H	H	H	X	NOP	Nop → Idle after t_{RP}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Nop → Idle after t_{RP}	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Row activating	H	X	X	X	X	DSL	Nop → Row active after t_{RCD}	
	L	H	H	H	X	NOP	Nop → Row active after t_{RCD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Write recovering	H	X	X	X	X	DSL	Nop → Maintain Row active after tWR	
	L	H	H	H	X	NOP	Nop → Maintain Row active after tWR	
	L	H	H	L	X	BST	Nop → Maintain Row active after tWR	
	L	H	L	H	BS, CA, A10	READ/READA	Begin Read	7
	L	H	L	L	BS, CA, A10	WRIT/WRITA	Begin new Write	
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write recovering with auto precharge	H	X	X	X	X	DSL	Nop → Enter precharge after tWR	
	L	H	H	H	X	NOP	Nop → Enter precharge after tWR	
	L	H	H	L	X	BST	Nop → Enter precharge after tWR	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Refreshing	H	X	X	X	X	DSL	Nop → Idle after tRFC	
	L	H	H	H	X	NOP	Nop → Idle after tRFC	
	L	H	H	L	X	BST	Nop → Idle after tRFC	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PREA	ILLEGAL	
	L	L	L	X	X	AREF/SELF/MRS/ EMRS	ILLEGAL	
Mode register accessing	H	X	X	X	X	DSL	Nop → Idle after tRSC	
	L	H	H	H	X	NOP	Nop → Idle after tRSC	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PREA/ AREF/SELF/MRS/ EMRS	ILLEGAL	

Note:

1. All entries assume that CKE was active (High level) during the preceding clock cycle and the current clock cycle (CKEn-1 = CKEn = ”1”)
2. Illegal if any bank is not idle.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BS), depending on the state of that bank.
4. Illegal if tRCD is not satisfied.
5. Illegal if tRAS is not satisfied.
6. Must satisfy burst interrupt condition.
7. Must avoid bus contention, bus turn around, and/or satisfy write recovery requirements.
8. Must mask preceding data which don’t satisfy tWR.

Remark: H = High level, L = Low level, X = High or Low level (Don’t care), V = Valid data

7.1.3 Function Truth Table for CKE

Current State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
	n-1	n							
Self refresh	H	X	X	X	X	X	X	N/A	
	L	H	H	X	X	X	X	Exit Self Refresh → Idle after tRFC	
	L	H	L	H	H	H	X	Exit Self Refresh → Idle after tRFC	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain Self Refresh	
Power-Down	H	X	X	X	X	X	X	N/A	
	L	H	H	X	X	X	X	Exit Power Down → Idle after 1 clock cycle	
			L	H	H	H	X		
	L	L	X	X	X	X	X	Maintain Power-Down	
Deep Power-Down	H	X	X	X	X	X	X	N/A	
	L	H	X	X	X	X	X	Exit Deep Power-Down → Exit Sequence	
	L	L	X	X	X	X	X	Maintain Deep Power-Down	
All banks idle	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power-down	2
	H	L	L	H	H	H	X	Enter Power-Down	2
	H	L	L	H	H	L	X	Enter Deep Power-Down	3
	H	L	L	L	L	H	X	Self Refresh	1
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power-Down	2
Row Active	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	2
	H	L	L	H	H	H	X	Enter Power down	2
	H	L	L	L	L	H	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power-Down → Row Active or Maintain PD	
Any state other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table	

Note:
1. Self refresh can enter only from the all banks idle state.
2. Power-down can enter only from the all banks idle or row active state.
3. Deep power-down can enter only from the all banks idle state.

Remark: H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data

7.1.4 Bank Activate Command

($\overline{RAS}$ = L, $\overline{CAS}$ = H, $\overline{WE}$ = H, BA0, BA1 = Bank, A0~An = Row Address)

The Bank Activate command activates the bank designated by the BS (Bank Select) signal.

Row addresses are latched on A0~An when this command is issued and the cell data is read out to the sense amplifiers. The maximum time that each bank can be held in the active state is specified as tRAS (max).

7.1.5 Bank Precharge Command

($\overline{RAS}$ = L, $\overline{RAS}$ = H, $\overline{WE}$ = L, BA0, BA1 = Bank, A10 =L)

The Bank Precharge command is used to close (or precharge) the bank that is activated. Using this command, systems can designated the bank to be closed by specifying the BS address bit setting in the command set. A Precharge command can be used to precharge each bank separately (Bank Precharge) or all four banks simultaneously (Precharge All). After the Bank Precharge command is issued, any one bank can close, and the closed bank transitions from the active state to the idle state. To re-activate the closed bank, a system has to wait the minimum tRP delay after issuing the Precharge command before issuing the Active Command for the device to complete the Precharge operation.

7.1.6 Precharge All Command

($\overline{RAS}$ = L, $\overline{CAS}$ = H, $\overline{WE}$ = L, BA0, BA1 = Don't care, A10 =H)

The Precharge All command is used to precharge all banks simultaneously. After this command is issued, all four banks close and transition from the active state to the idle state.

7.1.7 Write Command

($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = L, BA0, BA1 = Bank, A10 = L)

The Write command initiates a Write operation to the bank selected by BA0 and BA1 address inputs. The write data is latched at the positive edge of CLK. Users should preprogram the length of the write data (Burst Length) and the column access sequence (Addressing Mode) by setting the Mode Resister at power-up prior to using the Write command.

7.1.8 Write with Auto Precharge Command

($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = L, BA0, BA1 = Bank, A10 = H)

The Write with Auto Precharge command performs the Precharge operation automatically after the Write operation. The internal precharge starts in the cycles immediately following the cycle in which the last data is written independent of $\overline{CAS}$ Latency.

7.1.9 Read Command

($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = H, BA0, BA1 = Bank, A10 = L)

The Read command performs a Read operation to the bank designated by BA0-1. The read data is issued sequentially synchronized to the positive edges of CLK. The length of read data (Burst Length), Addressing Mode and $\overline{CAS}$ Latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode Register at power-up prior to the Write operation.

7.1.10 Read with Auto Precharge Command

($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = H, BA0, BA1 = Bank, A10 =H)

The Read with Auto Precharge command automatically performs the Precharge operation after the Read operation. When the $\overline{CAS}$ Latency = 3, the internal precharge starts two cycles before the last data is output. When the $\overline{CAS}$ Latency = 2, the internal precharge starts one cycle before the last data is output.

7.1.11 Extended Mode Register Set Command

($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = L, BA0, BA1, A0~An = Register Data)

The Extended Mode Register Set command is designed to support Partial Array Self Refresh, Temperature Compensated Self Refresh, and Output Driver Strength/Size by allowing users to program each value by setting predefined address bits. The default values in the Extended Mode Register after power-up are undefined; therefore this command must be issued during the power-up sequence. Also, this command can be issued while all banks are in the idle state.

7.1.12 Mode Register Set Command

($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = L, BA0, BA1, A0~An = Register Data)

The Mode Register Set command is used to program the values of $\overline{CAS}$ latency, Addressing Mode and Burst Length in the Mode Register. The default values in the Mode Register after power-up are undefined; therefore this command must be issued during the power-up sequence and re-issued after the Deep Power Down Exit Command. Also, this command can be issued while all banks are in the idle state.

7.1.13 No-Operation Command

($\overline{RAS}$ = H, $\overline{CAS}$ = H, $\overline{WE}$ = H)

The No-Operation command is used in cases such as preventing the device from registering unintended commands. The device performs no operation when this command is registered. This command is functionally equivalent to the Device Deselect command.

7.1.14 Burst Stop Command

($\overline{RAS}$ = H, $\overline{CAS}$ = H, $\overline{WE}$ = L)

The Burst stop command is used to stop the already activated burst operation. The activated page is left unclosed and future commands can be issued to access the same page of the active bank. If this command is issued during a burst read operation, the read data will go to a Hi-Z state after a delay equal to the $\overline{CAS}$ latency. If a burst stop command is issued during a burst write operation, then the burst data is terminated and data bus goes to Hi-Z at the same clock that the burst command is activated. Any remaining data from the burst write cycle is ignored.

7.1.15 Device Deselect Command

($\overline{CS}$ = H)

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

7.1.16 Auto Refresh Command

($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = H, CKE = H, BA0, BA1, A0~An = Don't care)

The Auto Refresh command is used to refresh the row address provided by the internal refresh counter. The Refresh operation must be performed 8192 times within 64 ms. The next command can be issued after tRC from the end of the Auto Refresh command. When the Auto Refresh command is issued, All banks must be in the idle state. The Auto Refresh operation is equivalent to the $\overline{CAS}$-before-$\overline{RAS}$ operation in a conventional DRAM.

7.1.17 Self Refresh Entry Command

($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = H, CKE = L, BA0, BA1, A0~An = Don't care)

When the Self Refresh Entry command is issued, the device enters the Self Refresh mode. While the device is in Self Refresh mode, the device automatically refreshes memory cells, and all input and I/O buffers (except the CKE buffer) are disabled. By asserting the CKE signal "high" (and by issuing the Self Refresh Exit command), the device exits the Self Refresh mode.

7.1.18 Self Refresh Exit Command

(CKE = H, $\overline{CS}$ = H or CKE = H, $\overline{RAS}$ = H, $\overline{CAS}$ = H)

This command is issued to exit out of the Self Refresh mode. One tRC delay is required prior to issuing any subsequent command from the end of the Self Refresh Exit command.

7.1.19 Clock Suspend Mode Entry/Power Down Mode Entry Command

(CKE = L)

The internal CLK is suspended for one cycle when this command is issued (when CKE is asserted "low"). The device state is held intact while the CLK is suspended. On the other hand, when the device is not operating the Burst cycle, this command performs entry into Power Down mode. All input and output buffers (except the CKE buffer) are turned off in Power Down mode.

7.1.20 Clock Suspend Mode Exit/Power Down Mode Exit Command

(CKE = H)

When the internal CLK has been suspended, operation of the internal CLK is resumed by providing this command (asserting CKE "high"). When the device is in Power Down mode, the device exits this mode and all disabled buffers are turned on to the active state. Any subsequent commands can be issued after one clock cycle from the end of this command.

7.1.21 Data Write/Output Enable, Data Mask/Output Disable Command

(DQM = L/H or LDQM, UDQM = L/H or DQM0-3=L/H)

During a Write cycle, the DQM or LDQM, UDQM or DQM0-3 signals mask write data. Each of these signals control the input buffers per byte. During a Read cycle, the DQM or LDQM, UDQM or DQM0-3 signals control of the output buffers per byte.

I/O Org.	MASK PIN	MASKED DQs
×16	LDQM	DQ0~DQ7
	UDQM:	DQ8~DQ15
×32	DQM0:	DQ0~DQ7
	DQM1:	DQ8~DQ15
	DQM2:	DQ16~DQ23
	DQM3:	DQ24~DQ31

8. OPERATION

8.1 Read Operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued after t_{RCD} from the Bank Activate command, the data is read out sequentially, synchronized to the positive edges of CLK (a Burst Read operation). The initial read data becomes available after $\overline{CAS}$ Latency from the issuing of the Read command. The $\overline{CAS}$ latency must be set in the Mode Register at power-up. In addition, the burst length of read data and Addressing Mode must be set. Each bank is held in the active state unless the Precharge command is issued, so that the sense amplifiers can be used as secondary cache.

When the Read with Auto Precharge command is issued, the Precharge operation is performed automatically after the Read cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Also, when the Burst Length is 1 and t_{RCD} (min), the timing from the $\overline{RAS}$ command to the start of the Auto Precharge operation is shorter than t_{RAS} (min). In this case, t_{RAS} (min) must be satisfied by extending t_{RCD}.

When the Precharge operation is performed on a bank during a Burst Read operation, the Burst operation is terminated.

When the Burst Length is full-page, column data is repeatedly read out until the Burst Stop command or Precharge command is issued.

8.2 Write Operation

Issuing the Write command after t_{RCD} from the Bank Activate command, the input data is latched sequentially, synchronizing with the positive edges of CLK after the Write command (Burst Write operation). The burst length of the Write data (Burst Length) and Addressing Mode must be set in the Mode Register at power-up.

When the Write with Auto Precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other command for the entire burst data duration. Also, when the Burst Length is 1 and t_{RCD} (min), the timing from the $\overline{RAS}$ command to the start of the Auto Precharge operation is shorter than tRAS (min). In this case, t_{RAS} (min) must be satisfied by extending t_{RCD}.

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated.

When the Burst Length is full-page, the input data is repeatedly latched until the Burst Stop command or the Precharge command is issued.

When the Burst Read and Single Write mode is selected, the write burst length is 1 regardless of the read burst length.

8.3 Precharge

There are two commands which perform the Precharge operation: Bank Precharge and Precharge All. When the Bank Precharge command is issued to the active bank, the bank is precharged and then switched to the idle state. The Bank Precharge command can precharge one bank independently of the other bank and hold the unprecharged bank in the active state. The maximum time each bank can be held in the active state is specified as t_{RAS} (max). Therefore, each bank must be precharged within t_{RAS} (max) from the Bank Activate command.

The Precharge All command can be used to precharge all banks simultaneously. Even if banks are not in the active state, the Precharge All command can still be issued. In this case, the Precharge operation is performed only for the active bank and the precharged bank is then switched to the idle state.

8.3.1 Auto Precharge

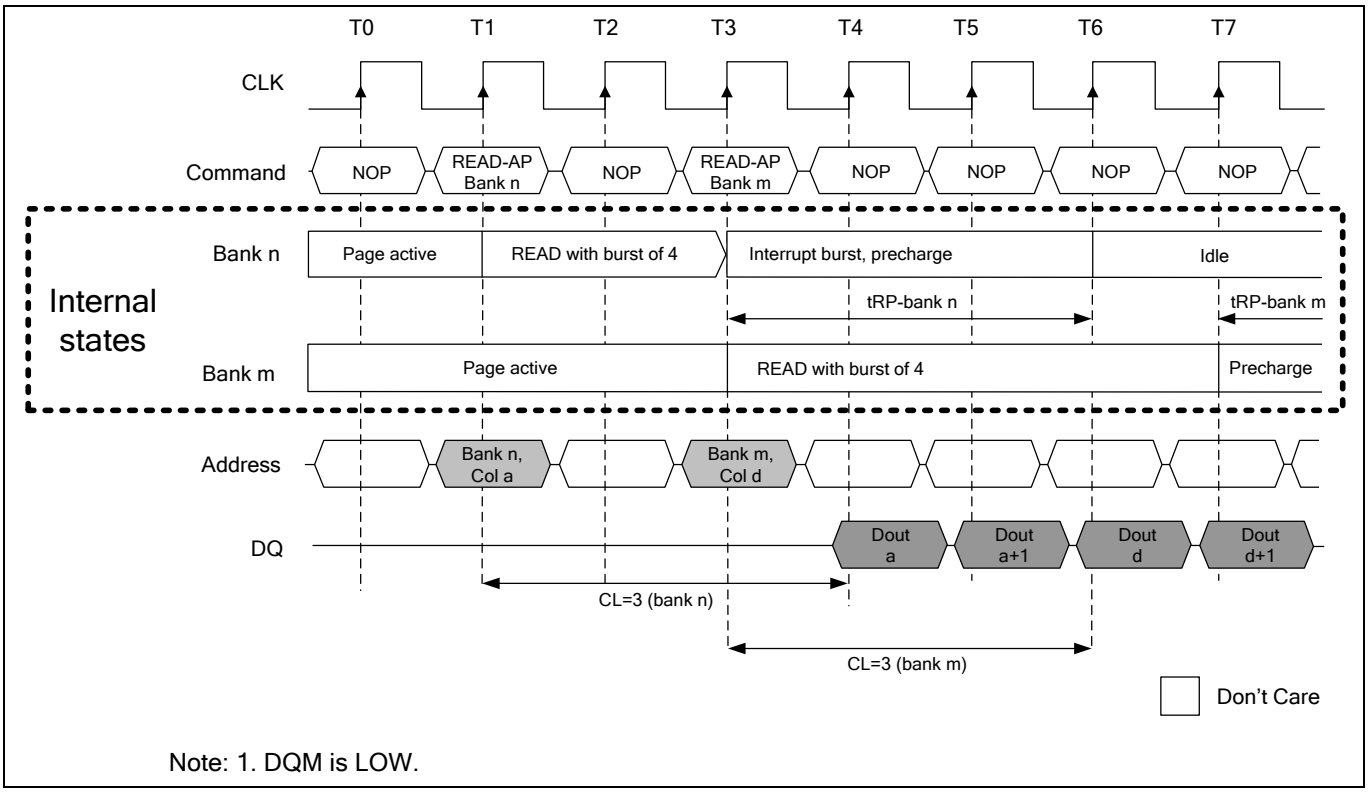
Auto precharge is a feature that performs the same individual-bank PRECHARGE function described previously, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. Another command cannot be issued to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time.

Winbond SDRAM supports concurrent auto precharge; cases of concurrent auto precharge for READs and WRITEs are defined below.

8.3.2 READ with auto precharge interrupted by a READ (with or without auto precharge)

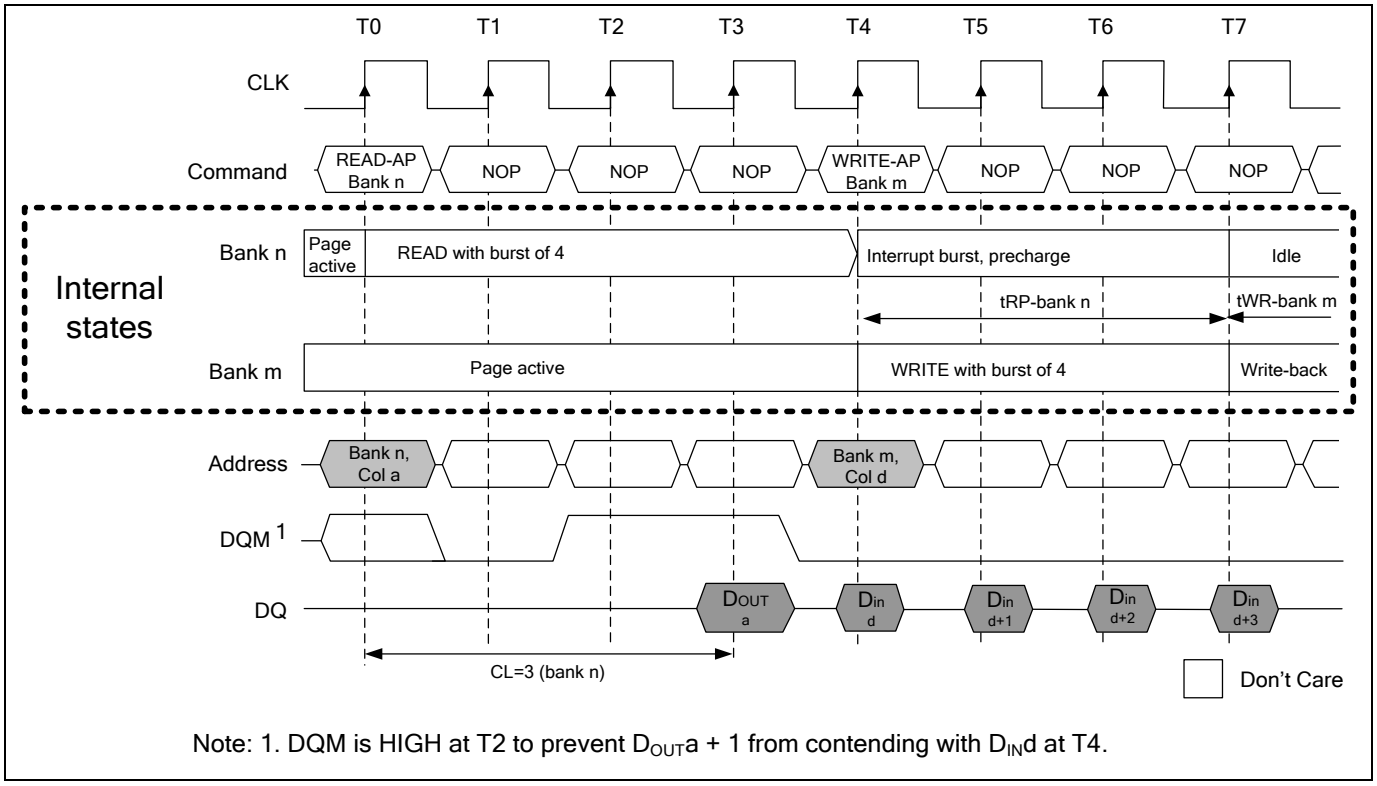
A READ to bank m will interrupt a READ on bank n following the programmed CAS latency. The precharge to bank n begins when the READ to bank m is registered.



Note: 1. DQM is LOW.

8.3.3 READ with auto precharge interrupted by a WRITE (with or without auto precharge)

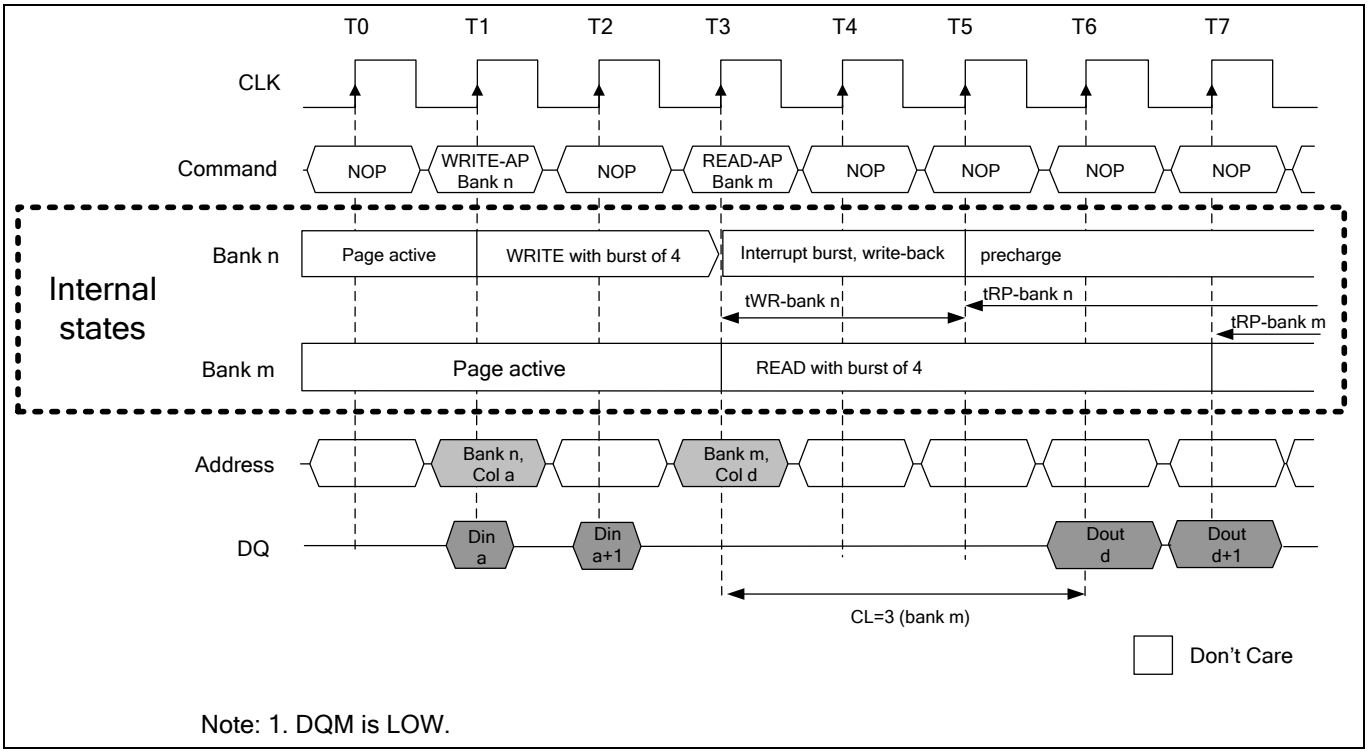
A WRITE to bank m will interrupt a READ on bank n when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank n begins when the WRITE to bank m is registered.



Note: 1. DQM is HIGH at T2 to prevent $D_{OUT}a + 1$ from contending with $D_{IN}d$ at T4.

8.3.4 WRITE with auto precharge interrupted by a READ (with or without auto precharge)

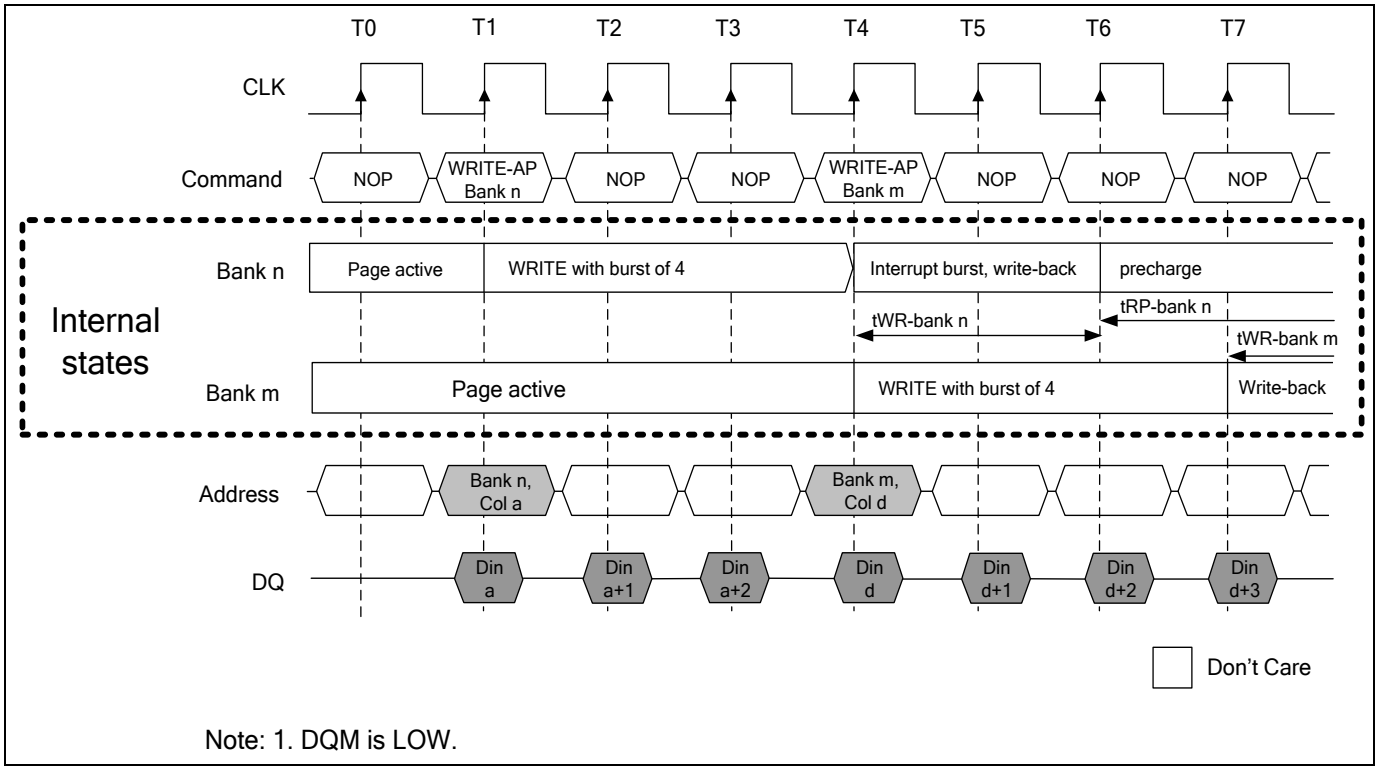
A READ to bank m will interrupt a WRITE on bank n when registered, with the data-out appearing CL later. The precharge to bank n will begin after tWR is met, where tWR begins when the READ to bank m is registered. The last valid WRITE to bank n will be data in registered one clock prior to the READ to bank m.



Note: 1. DQM is LOW.

8.3.5 WRITE with auto precharge interrupted by a WRITE (with or without auto precharge)

A WRITE to bank m will interrupt a WRITE on bank n when registered. The precharge to bank n will begin after tWR is met, where tWR begins when the WRITE to bank m is registered. The last valid data WRITE to bank n will be data registered one clock prior to a WRITE to bank m.



Note: 1. DQM is LOW.

8.4 Burst Termination

The Read or Write command can be issued on any clock cycle. Whenever a Read operation is to be interrupted by a Write command, the output data must be masked by DQM to avoid I/O conflict. Also, when a Write operation is to be interrupted by a Read command, only the input data before the Read command is enable and the input data after the Read command is disabled.

- Read Interrupted by a Precharge

  A Precharge command can be issued to terminate a Burst cycle early. When a Burst Read cycle is interrupted by a Precharge command, the read operation is terminated after ($\overline{CAS}$ latency-1) clock cycles from the Precharge command.

- Write Interrupted by a Precharge

  A burst Write cycle can be interrupted by a Precharge command, the input circuit is reset at the same clock cycle at which the Precharge command is issued. In this case, the DQM signal must be asserted high to prevent writing the invalid data to the cell array.

- Read Interrupted by a Burst Stop

  When the Burst Stop command is issued for the bank in a Burst cycle, the Burst operation is terminated. When the Burst Stop command is issued during a Burst Read cycle, the read operation is terminated after clock cycle of ($\overline{CAS}$ latency-1) from the Burst Stop command.

- Write Interrupted by a Burst Stop

  When the Burst Stop command is issued during a Burst Write cycle, the write operation is terminated at the same clock cycle that the Burst Stop command is issued.

- Write Interrupted by a Read

  A burst of write operation can be interrupted by a read command. The read command interrupts the write operation on the same clock that the read command is issued. All the burst writes that are presented on the data bus before the read command is issued will be written to the memory. Any remaining burst writes will be ignored once the read command is activated. There must be at least one clock bubble (Hi-Z state) on the data bus to avoid bus contention.

- Read Interrupted by a Write

  A burst of read operation can be interrupted by a write command by driving output drivers in a Hi-Z state using DQM before write to avoid data conflict. DQM should be utilized if there is data from a Red command on the first and second cycles of the subsequent write cycles to ensure the read data are tri-stated. From the third clock cycle, the write command will control the data bus and DQM is not needed.

8.5 Mode Register Operation

The Mode register designates the operation mode for the Read or Write cycle. This register is divided into three fields; A Burst Length field to set the length of burst data, an Addressing Mode selected bits to designate the column access sequence in a Burst cycle, and a $\overline{CAS}$ Latency field to set the access time in clock cycle.

The Mode Register is programmed by the Mode Register Set command when all banks are in the idle state. The data to be set in the Mode Register is transferred using the A0~An, BA0, BA1 address inputs. The initial value of the Mode Register after power-up is undefined; therefore the Mode Register Set command must be issued before proper operation.

8.5.1 Burst Length field (A2~A0)

This field specifies the data length for column access using the A2~A0 pins and sets the Burst Length to be 1, 2, 4, 8, words, or full-page.

A2	A1	A0	BUST LENGTH
0	0	0	1 word
0	0	1	2 words
0	1	0	4 words
0	1	1	8 words
1	1	1	Full-Page

8.5.2 Addressing Mode Select (A3)

The Addressing Mode can be one of two modes; Interleave mode or Sequential mode. When the A3 bit is 0, Sequential mode is selected. When the A3 bit is 1, Interleave mode is selected. Both Addressing modes support burst length of 1, 2, 4 and 8 words. Additionally, Sequential mode supports the full-page burst.

A3	ADDRESSING MODE
0	Sequential
1	Interleave

- Addressing sequence of Sequential mode

  A column access is performed by incrementing the column address input to the device. The address is varied by the Burst Length shown as below table.

8.5.3 Addressing Sequence for Sequential Mode

DATA	Access Address	Burst Length
Data0	n	2 words (Address bits is A0) not carried from A0 to A1
Data1	n + 1	
Data2	n + 2	4 words (Address bits is A1, A0) not carried from A1 to A2
Data3	n + 3	
Data4	n + 4	8 words (Address bits is A2, A1, A0) not carried from A2 to A3
Data5	n + 5	
Data6	n + 6	
Data7	n + 7	

- Addressing sequence of Interleave mode

  A column access is started from the input column address and is performed by inverting the address bits in the sequence shown as below table.

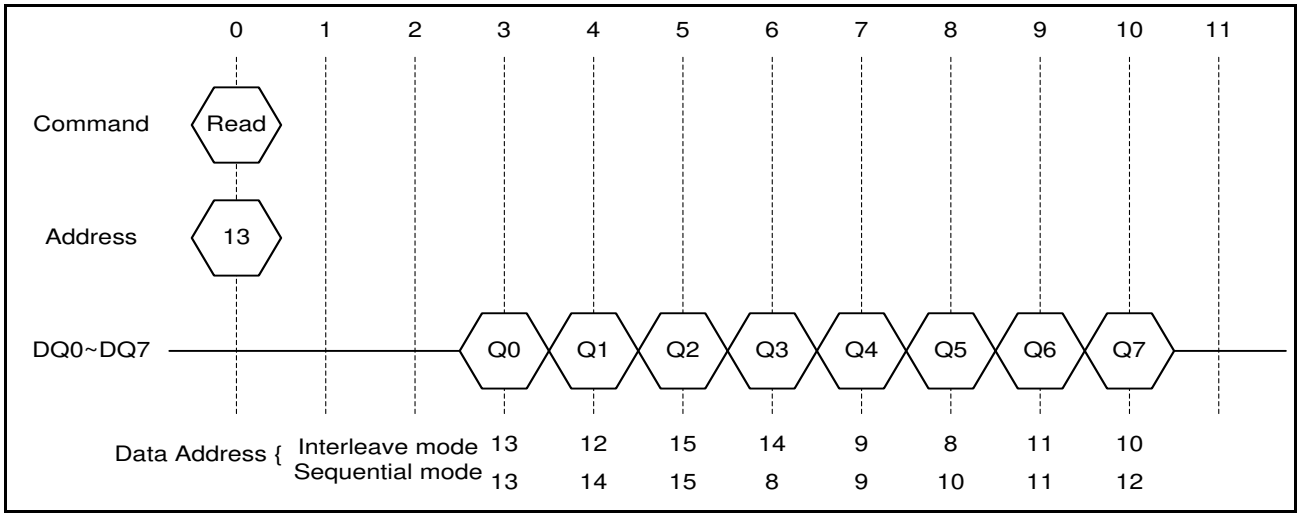
8.5.4 Addressing Sequence for Interleave Mode

DATA	Access Address	Burst Length
Data0	A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words
Data1	A8 A7 A6 A5 A4 A3 A2 A1 $\bar{A}0$	
Data2	A8 A7 A6 A5 A4 A3 A2 $\bar{A}1$ A0	4 words
Data3	A8 A7 A6 A5 A4 A3 A2 $\bar{A}1$ $\bar{A}0$	
Data4	A8 A7 A6 A5 A4 A3 $\bar{A}2$ A1 A0	8 words
Data5	A8 A7 A6 A5 A4 A3 $\bar{A}2$ A1 $\bar{A}0$	
Data6	A8 A7 A6 A5 A4 A3 $\bar{A}2$ $\bar{A}1$ A0	
Data7	A8 A7 A6 A5 A4 A3 $\bar{A}2$ $\bar{A}1$ $\bar{A}0$	

8.5.5 Addressing Sequence Example (Burst Length = 8 and Input Address is 13)

DATA	INTERLEAVE MODE										SEQUENTIAL MODE		
	A8	A7	A6	A5	A4	A3	A2	A1	A0	ADD		ADD	
Data0	0	0	0	0	0	1	1	0	1	13	13	13	
Data1	0	0	0	0	0	1	1	0	0	12	13 + 1	14	
Data2	0	0	0	0	0	1	1	1	1	15	13 + 2	15	calculated using A2, A1 and A0 bits not carry from A2 to A3 bit.
Data3	0	0	0	0	0	1	1	1	0	14	13 + 3	8	
Data4	0	0	0	0	0	1	0	0	1	9	13 + 4	9	
Data5	0	0	0	0	0	1	0	0	0	8	13 + 5	10	
Data6	0	0	0	0	0	1	0	1	1	11	13 + 6	11	
Data7	0	0	0	0	0	1	0	1	0	10	13 + 7	12	

8.5.6 Read Cycle $\overline{CAS}$ Latency = 3



8.5.7 $\overline{CAS}$ Latency field (A6~A4)

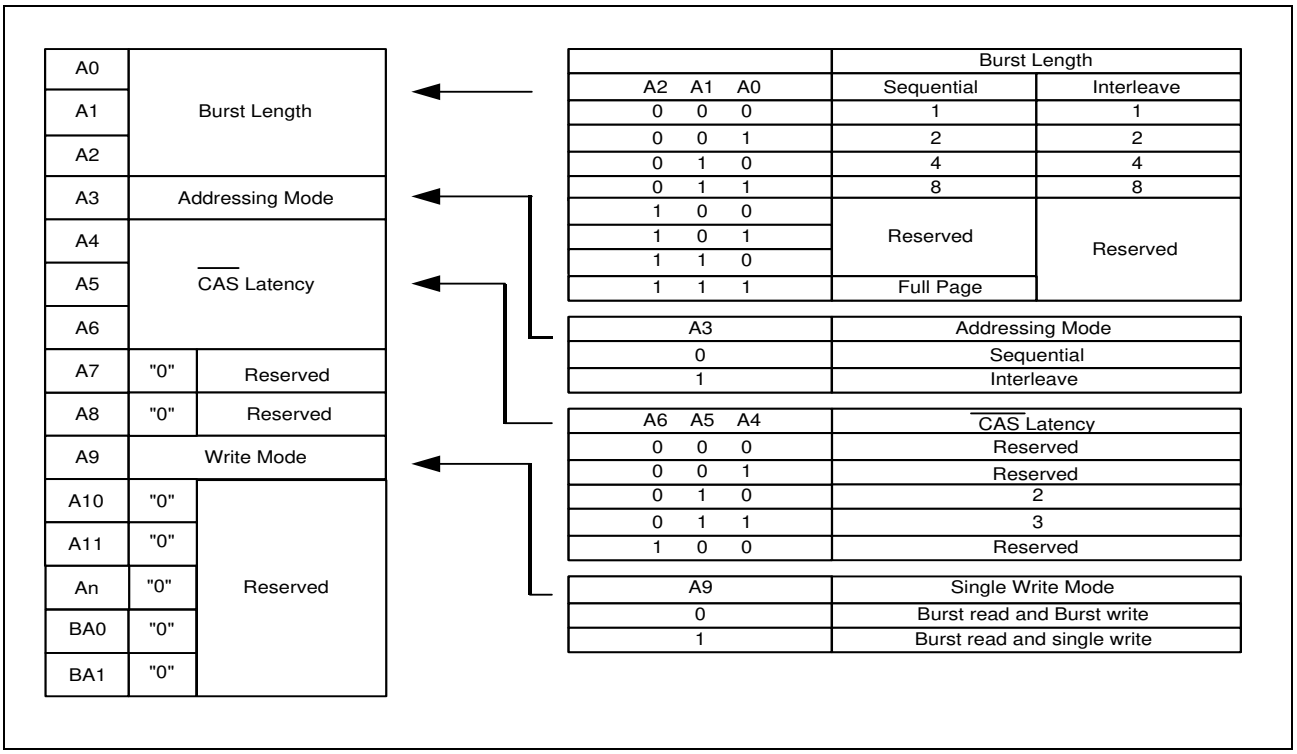
This field specifies the number of clock cycles from the assertion of the Read command to the first data read. The minimum values of $\overline{CAS}$ Latency depends on the frequency of CLK. The minimum value which satisfies the following formula must be set in this field.

A6	A5	A4	$\overline{CAS}$ Latency
0	1	0	2 clock
0	1	1	3 clock

- Reserved bits (A7, A8, A10, A11, An, BA0, BA1)
  These bits are reserved for future operations. They must be set to 0 for normal operation.
- Single Write mode (A9)
  This bit is used to select the write mode. When the A9 bit is 0, Burst Read and Burst Write mode are selected. When the A9 bit is 1, Burst Read and Single Write mode are selected.

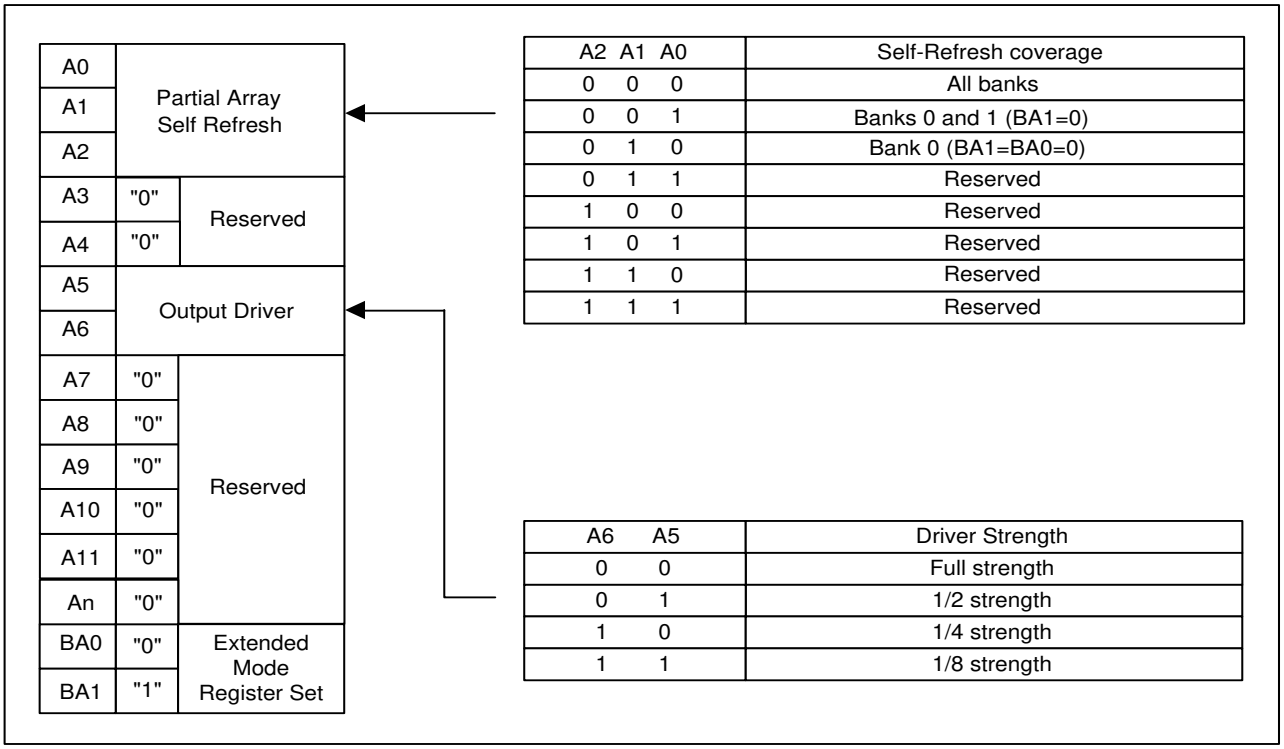
A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

8.5.8 Mode Register Definition



8.6 Extended Mode Register Description

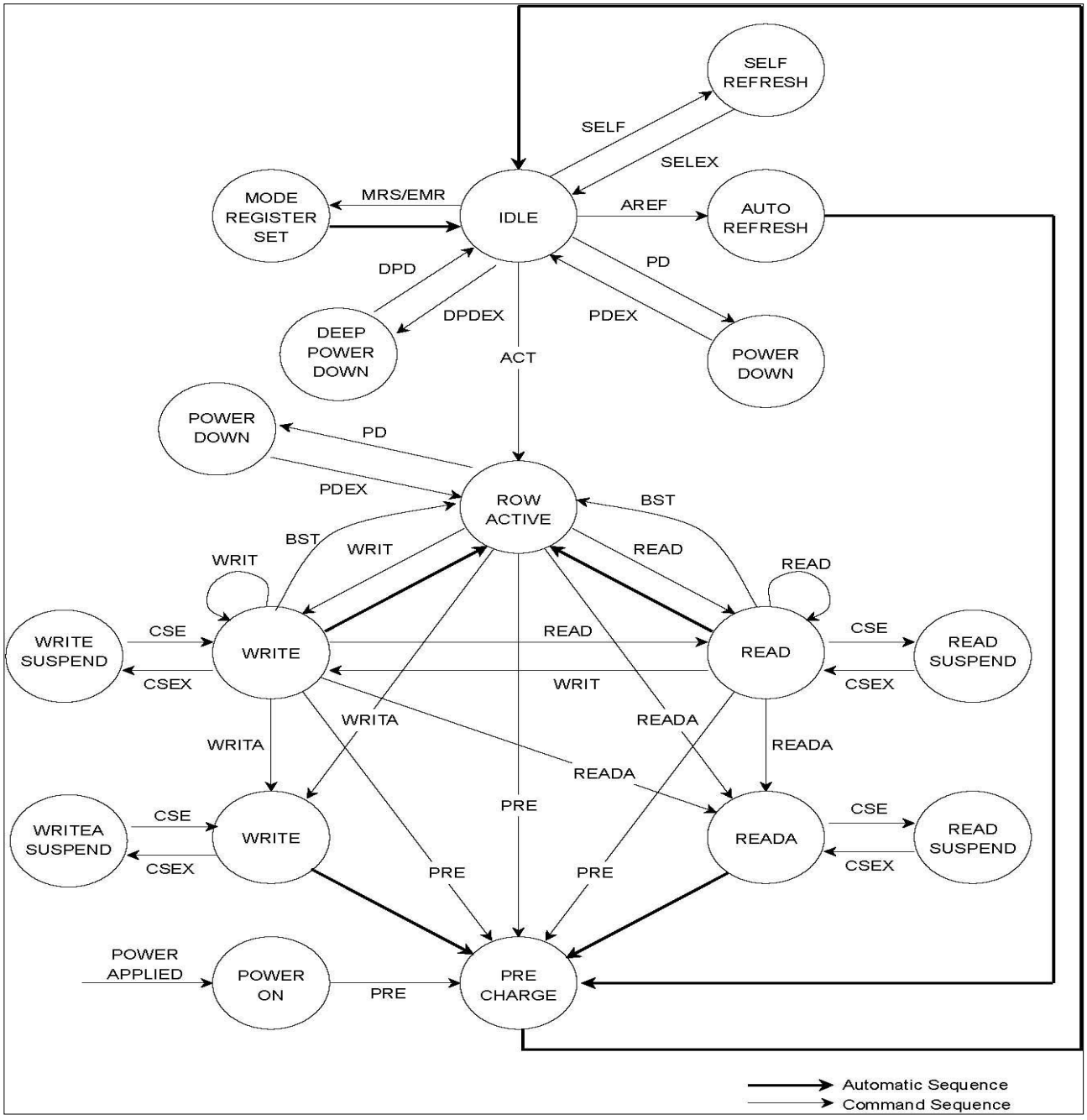
The Extended Mode Register designates the operation condition while SDRAM is in Self Refresh Mode and selects the output driver strength as full, 1/2, 1/4, or 1/8 strength. The register is divided into two fields; (1) Partial Array Self Refresh field selects how much banks or which part of a bank need to be refreshed during Self Refresh. (2) Driver Strength selected bit to control the size of output buffer. The initial value of the Extended Mode Register after power-up is Full Driver Strength, and all banks are refreshed during Self Refresh Mode.



A2	A1	A0	Self-Refresh coverage
0	0	0	All banks
0	0	1	Banks 0 and 1 (BA1=0)
0	1	0	Bank 0 (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

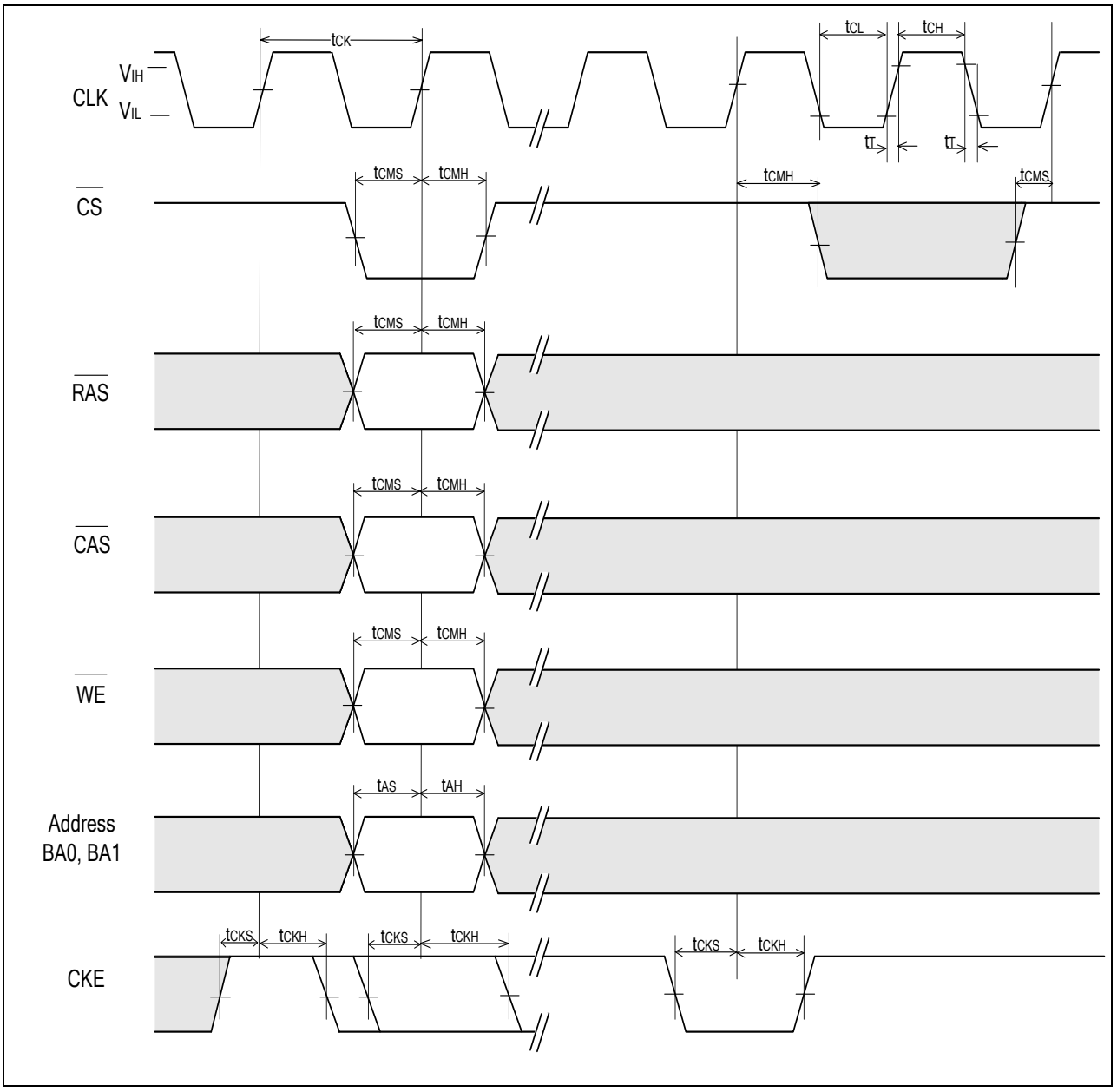
A6	A5	Driver Strength
0	0	Full strength
0	1	1/2 strength
1	0	1/4 strength
1	1	1/8 strength

8.7 Simplified State Diagram

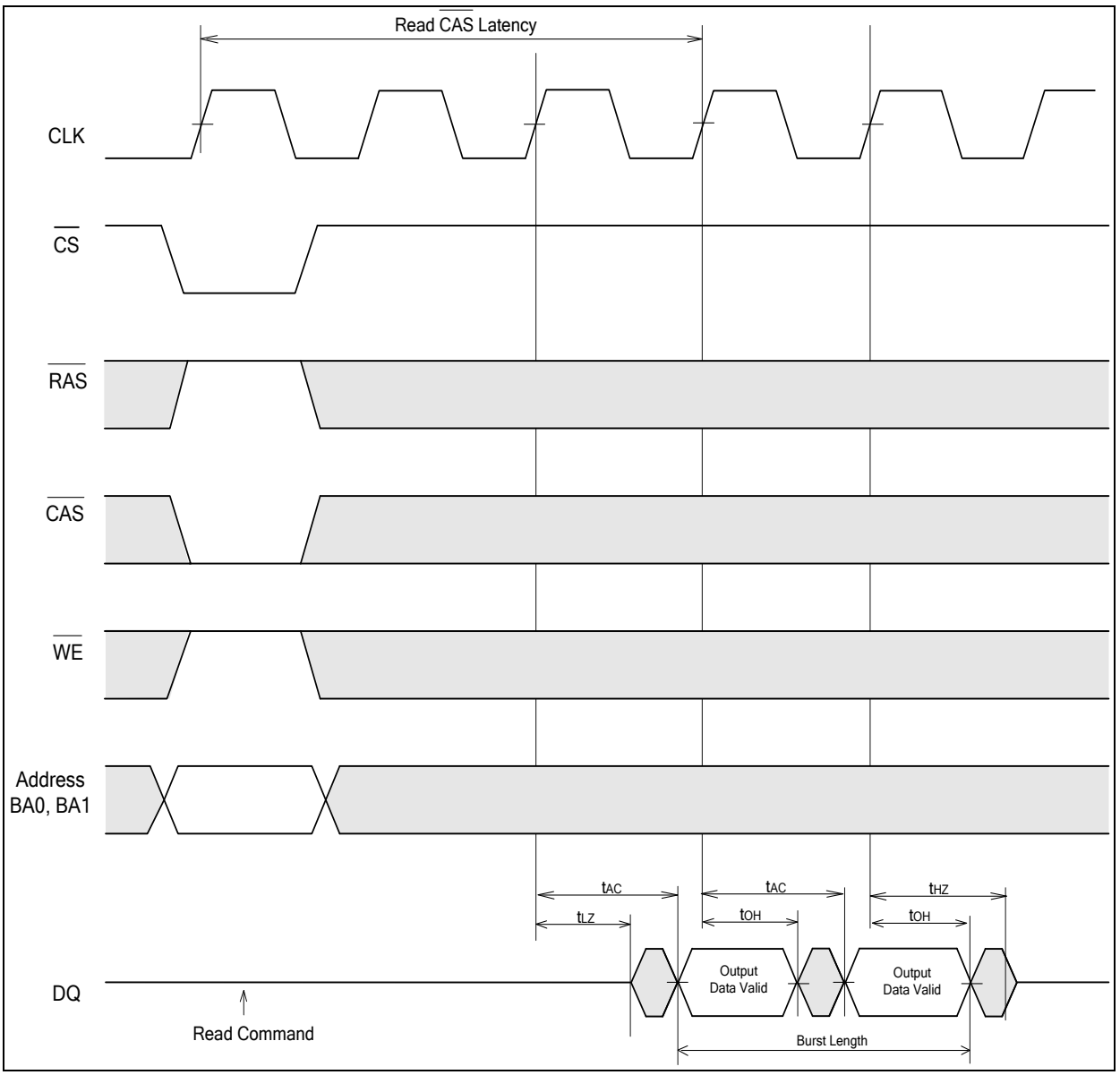


9. CONTROL TIMING WAVEFORMS

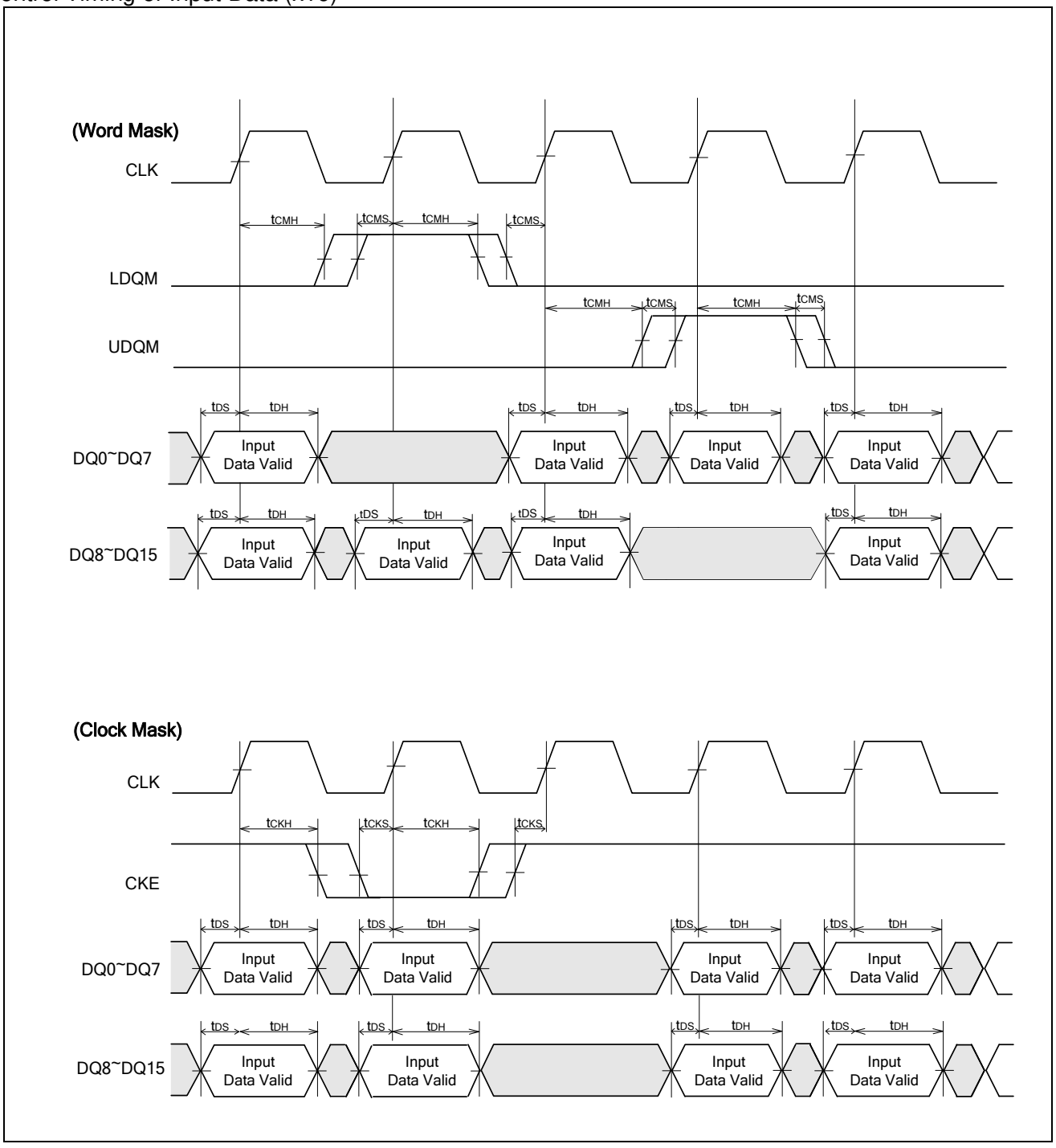
9.1 Command Input Timing



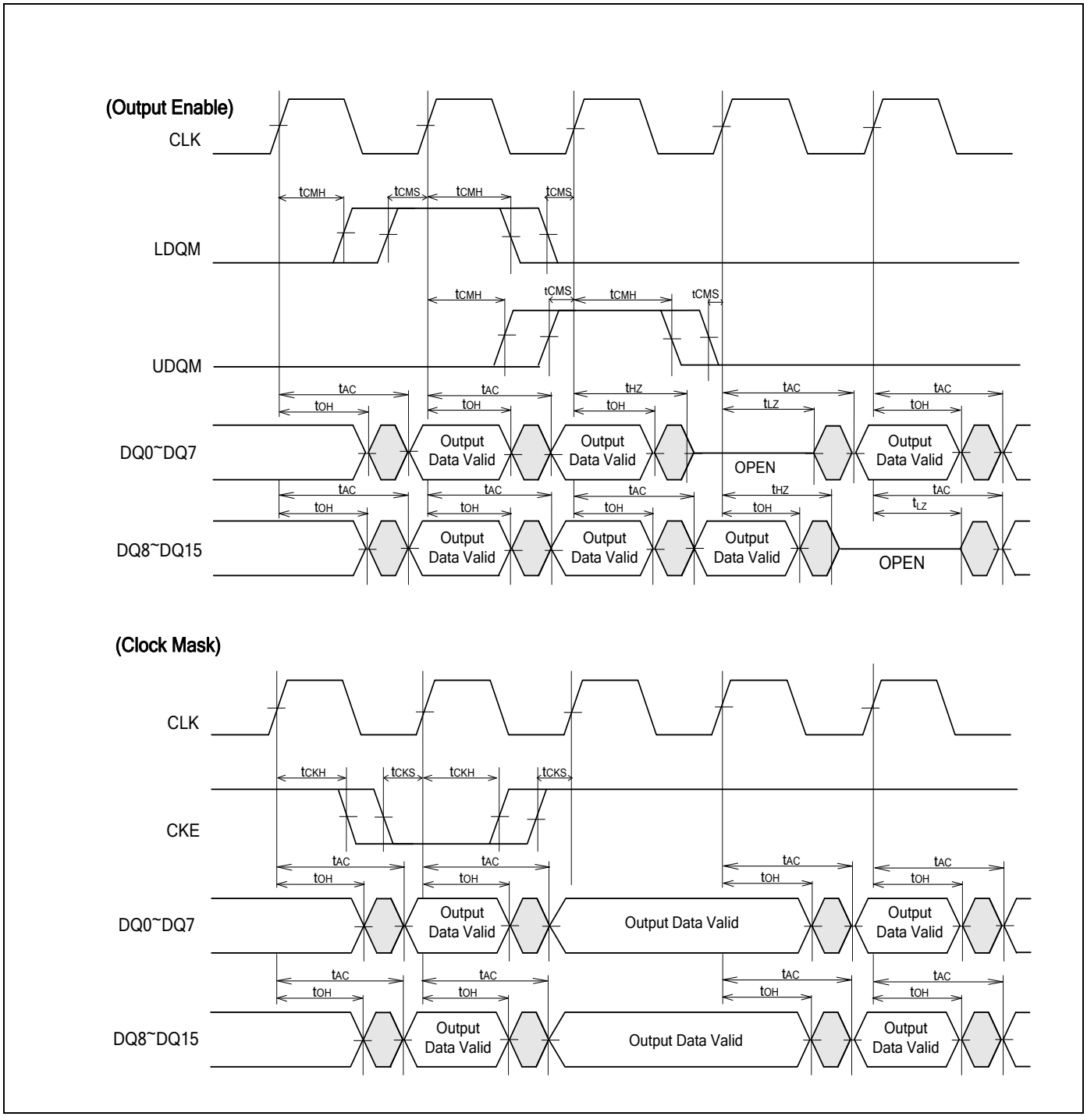
9.2 Read Timing



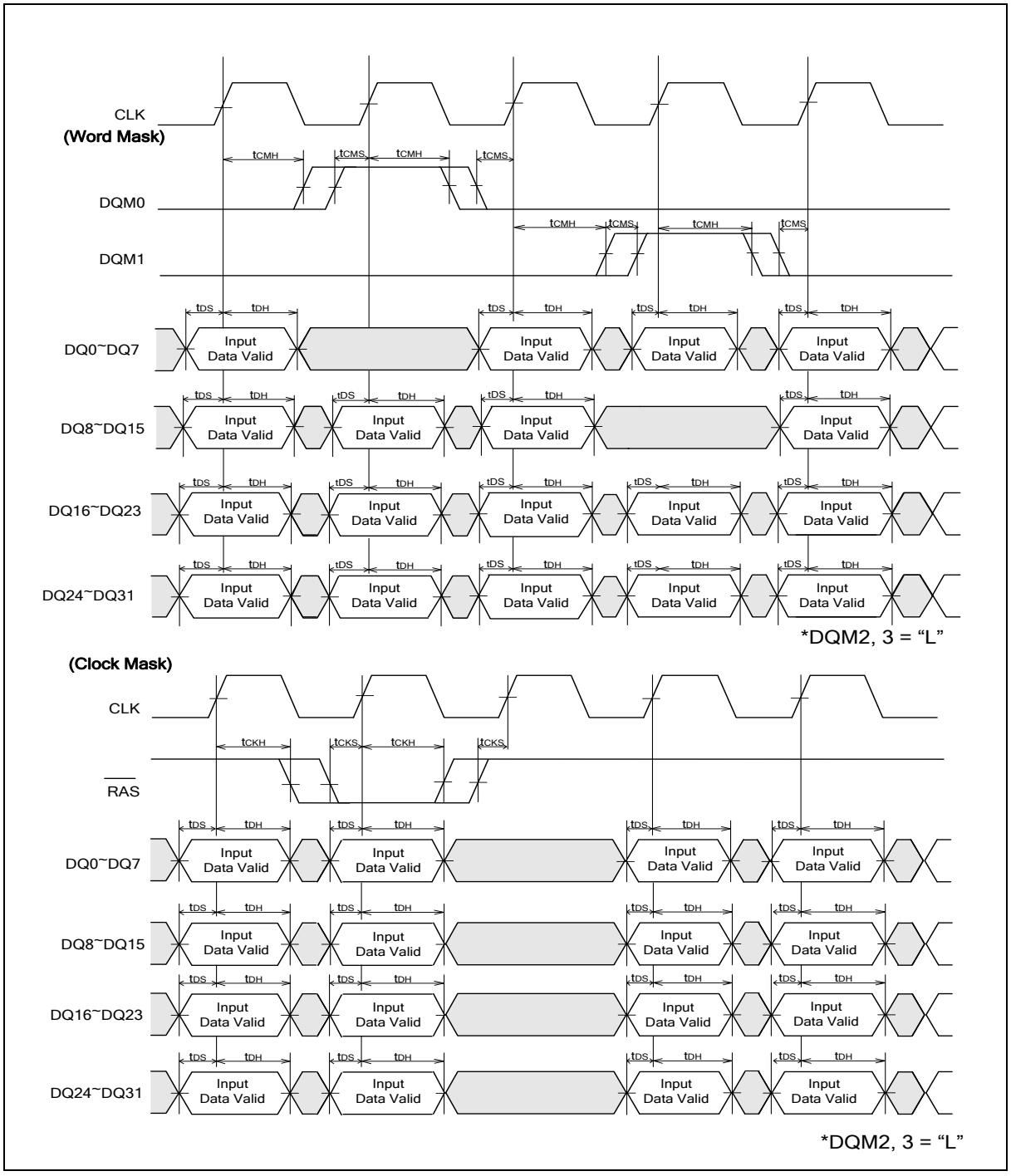
9.3 Control Timing of Input Data (x16)



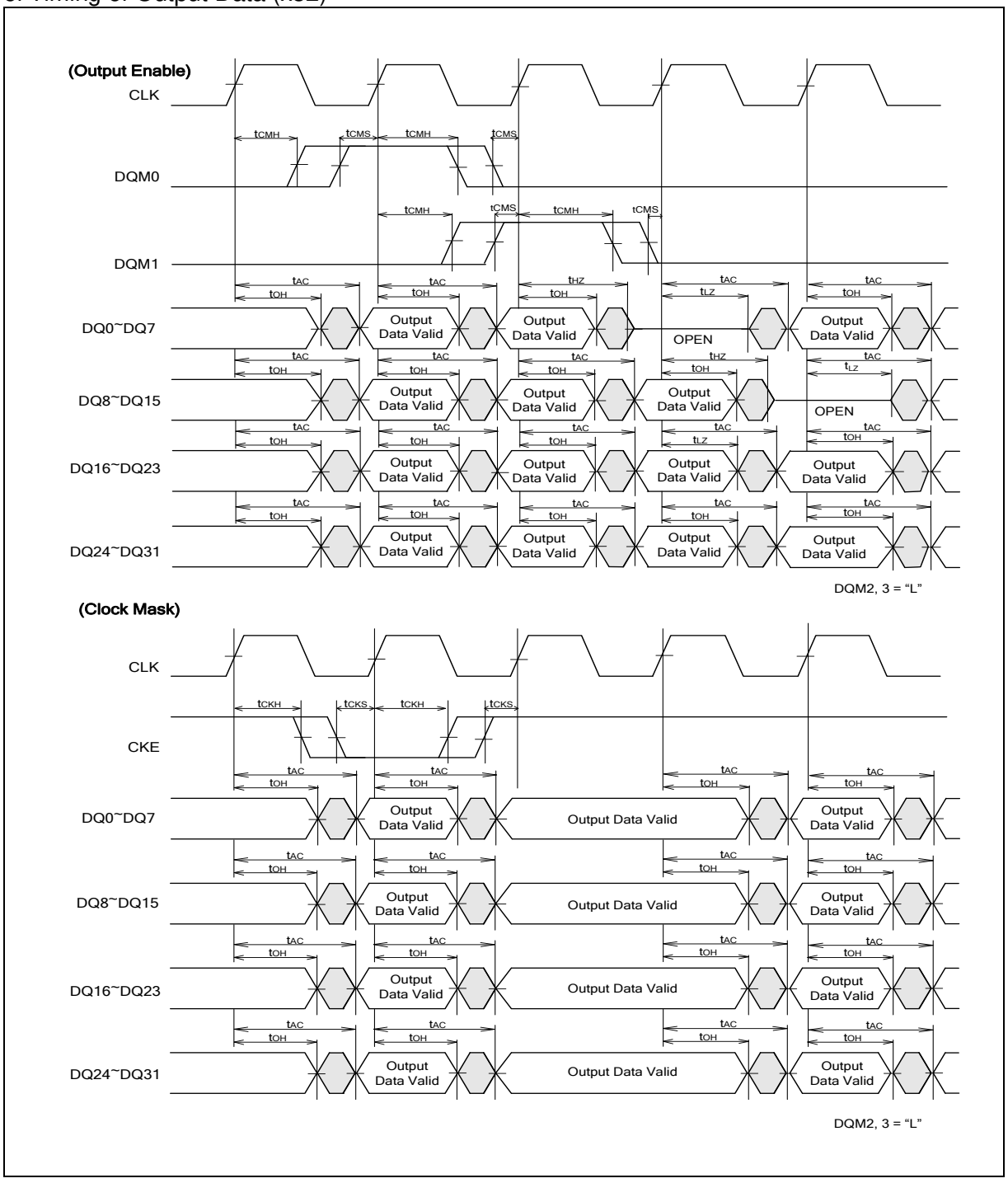
9.4 Control Timing of Output Data (x16)



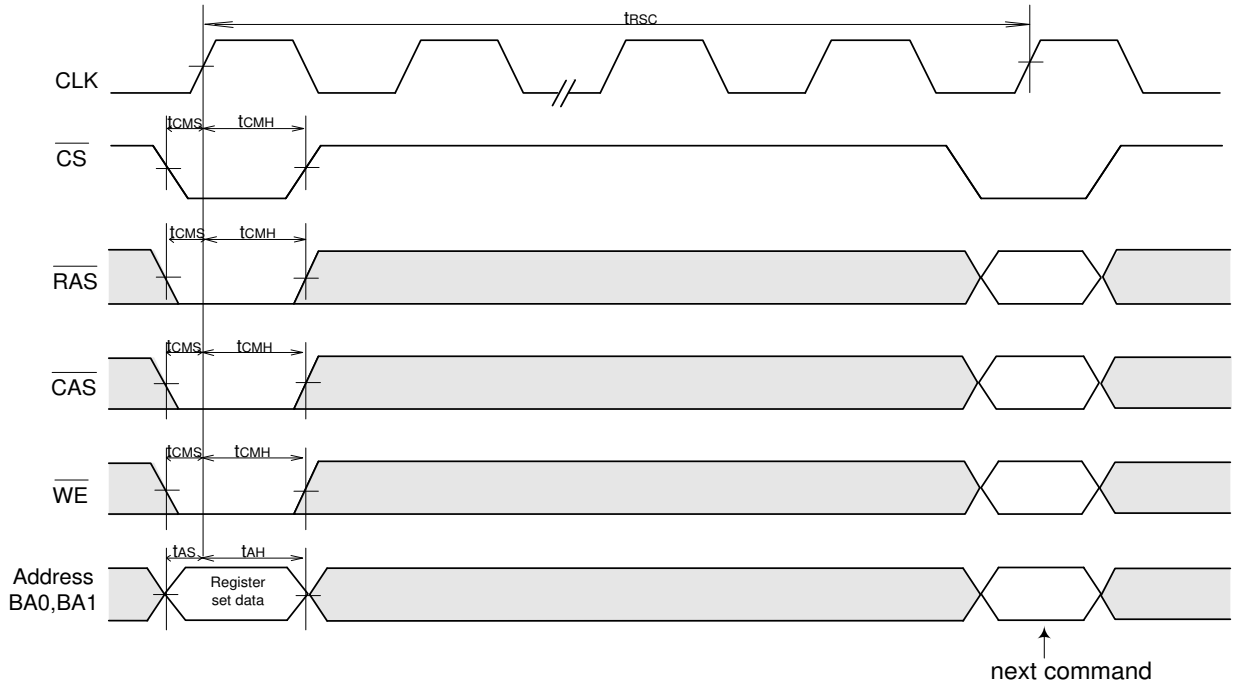
9.5 Control Timing of Input Data (x32)



9.6 Control Timing of Output Data (x32)



9.7 Mode register Set (MRS) Cycle



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	$\overline{CAS}$ Latency	
A5		
A6		
A7	0	Reserved
A8	0	Reserved
A9	Write Mode	
A10	0	Reserved
A11	0	
An	0	
BA0	0	Mode Register Set
BA1	0	

			Burst Length	
A2	A1	A0	Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

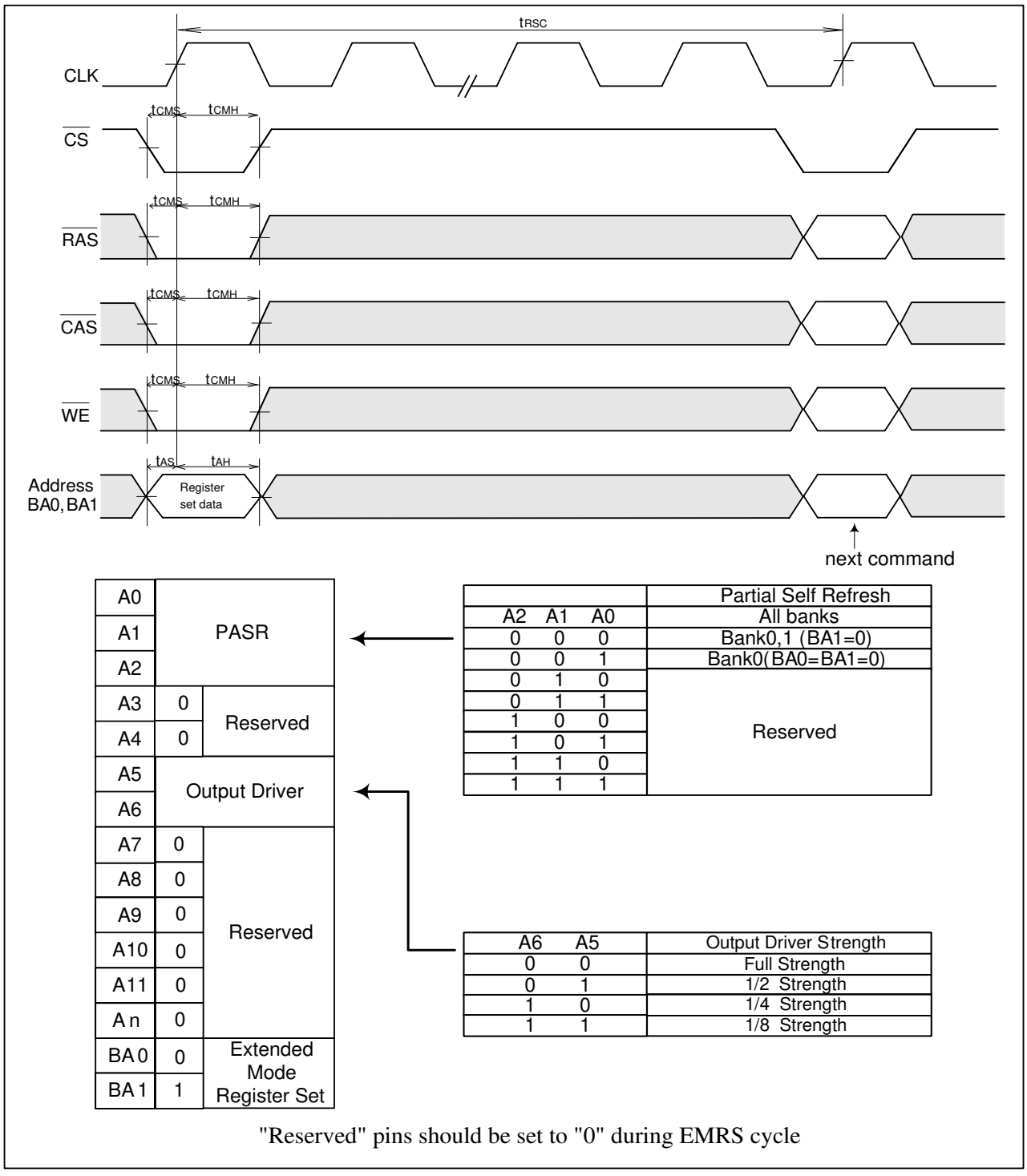
A3	Addressing Mode
0	Sequential
1	Interleave

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

"Reserved" pins should be set to "0" during MRS cycle.

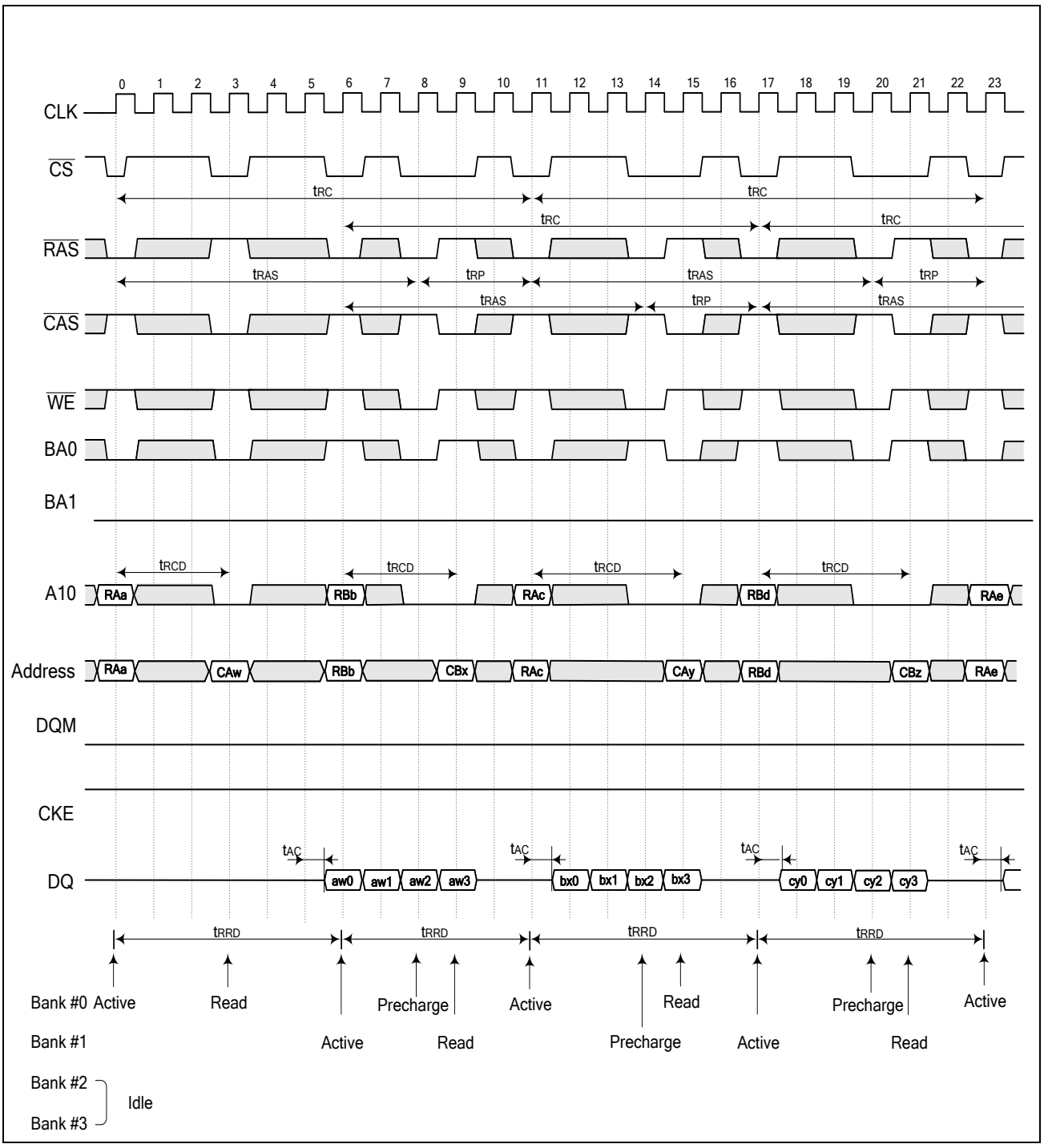
9.8 Extended Mode register Set (EMRS) Cycle



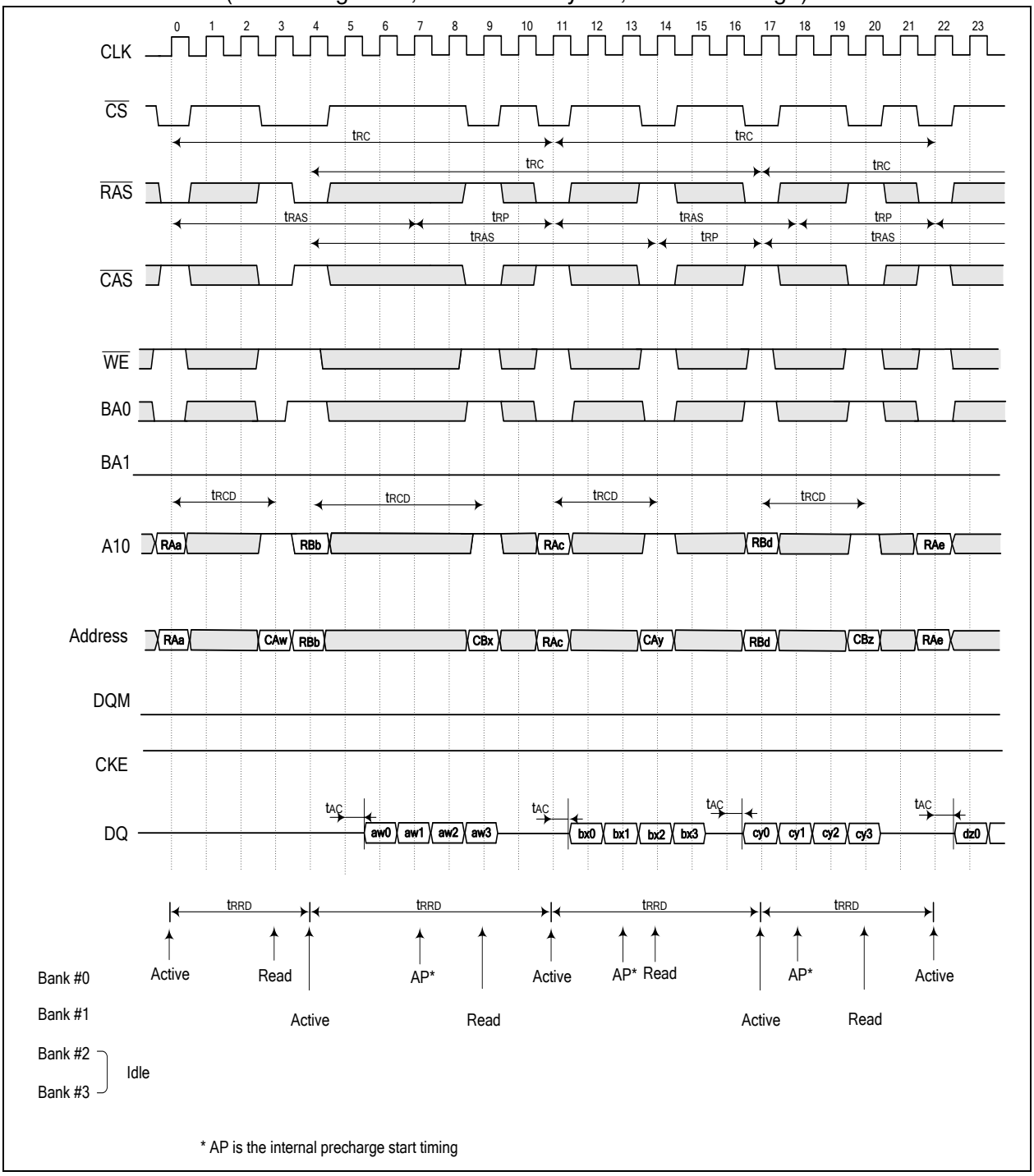
"Reserved" pins should be set to "0" during EMRS cycle

10. OPERATING TIMING EXAMPLE

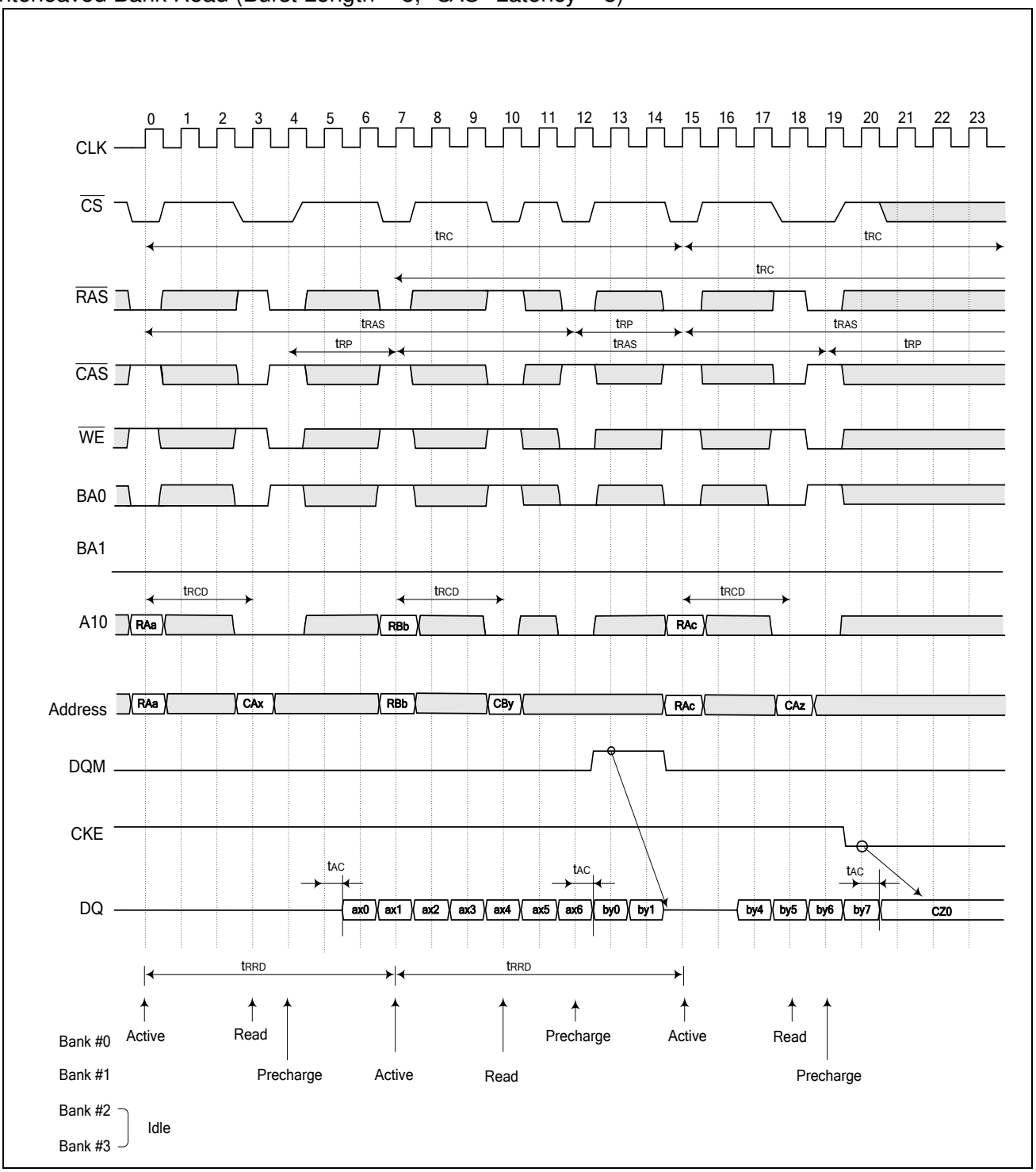
10.1 Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



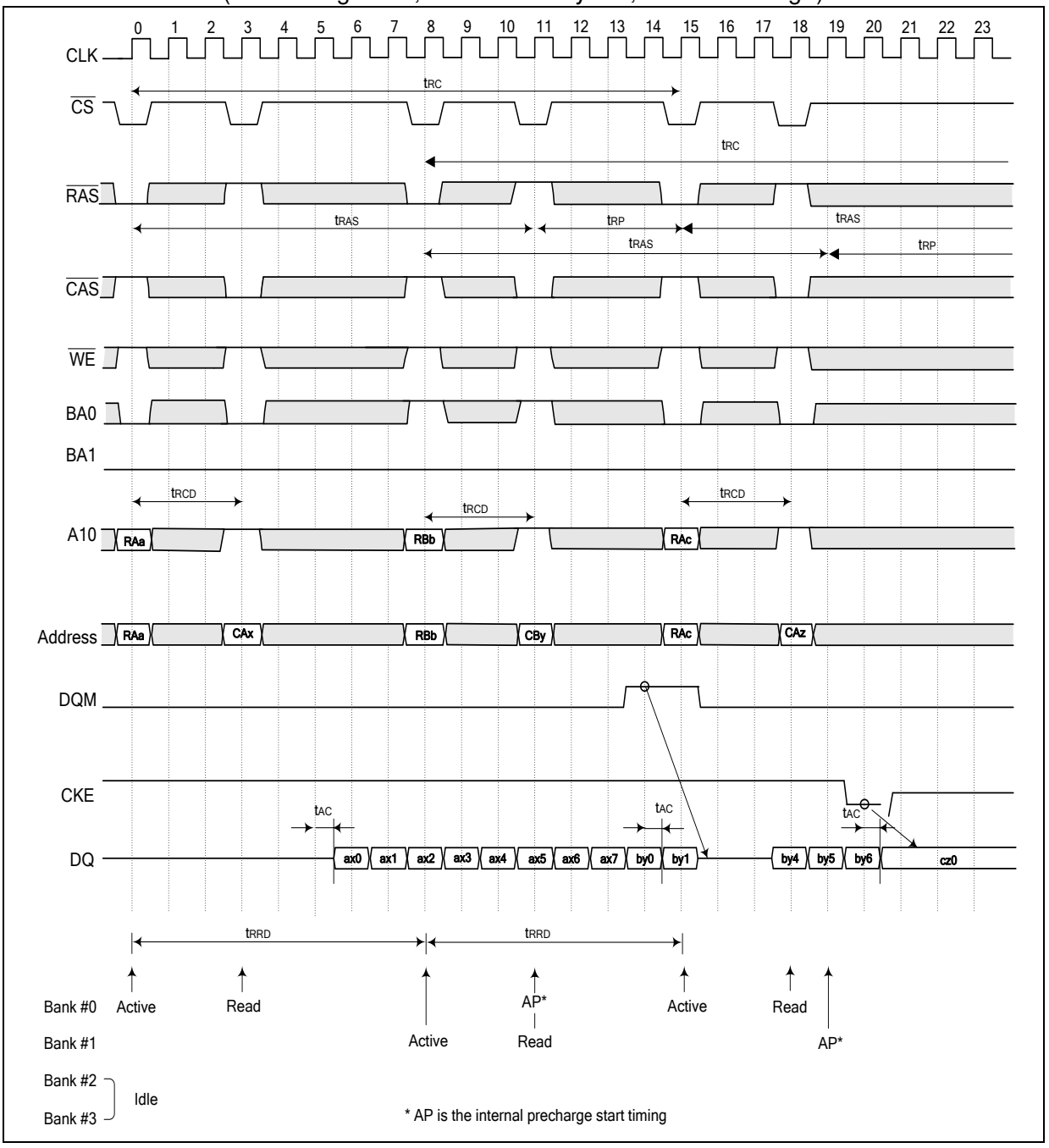
10.2 Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3, Auto Precharge)



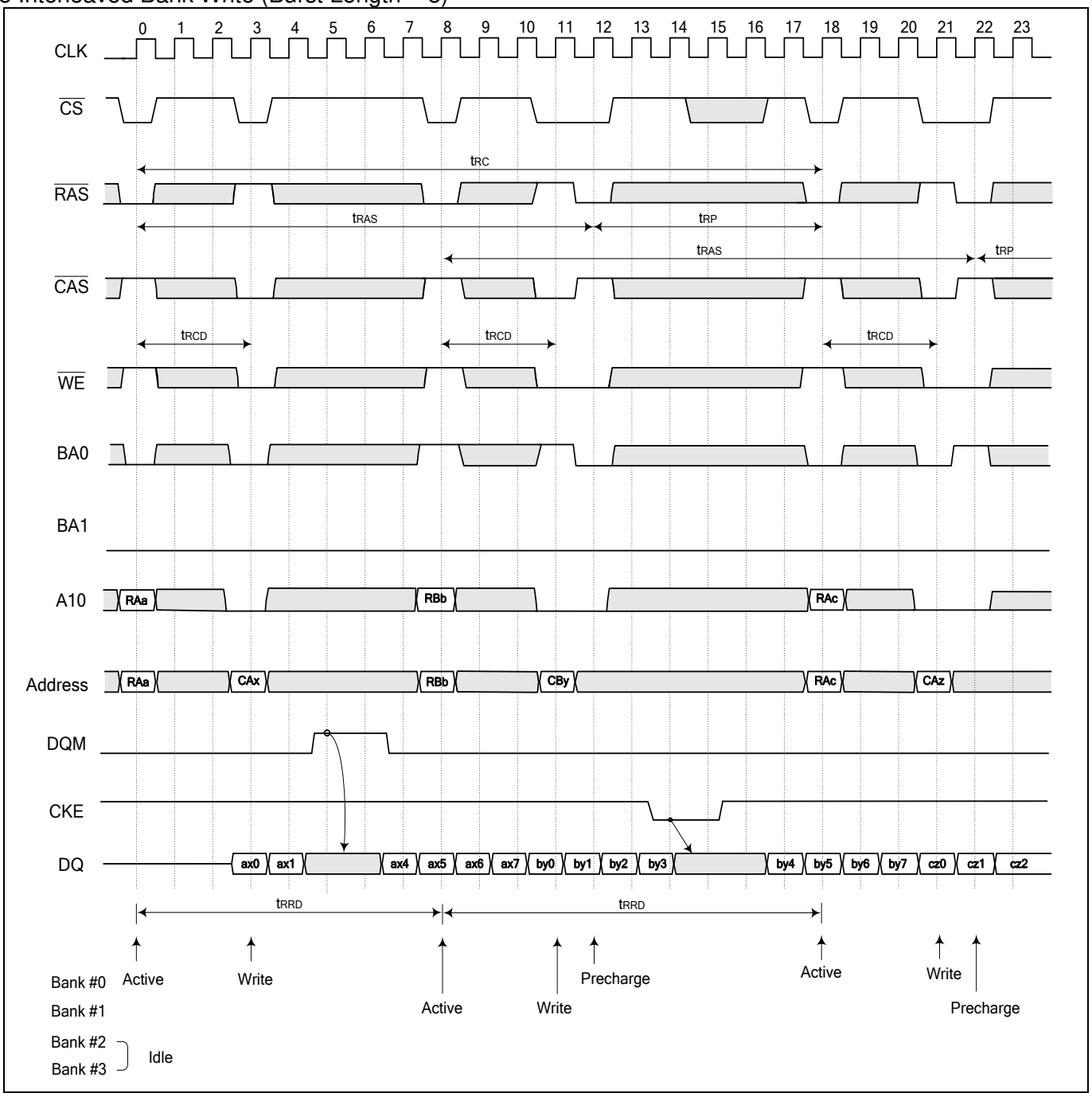
10.3 Interleaved Bank Read (Burst Length = 8, $\overline{CAS}$ Latency = 3)



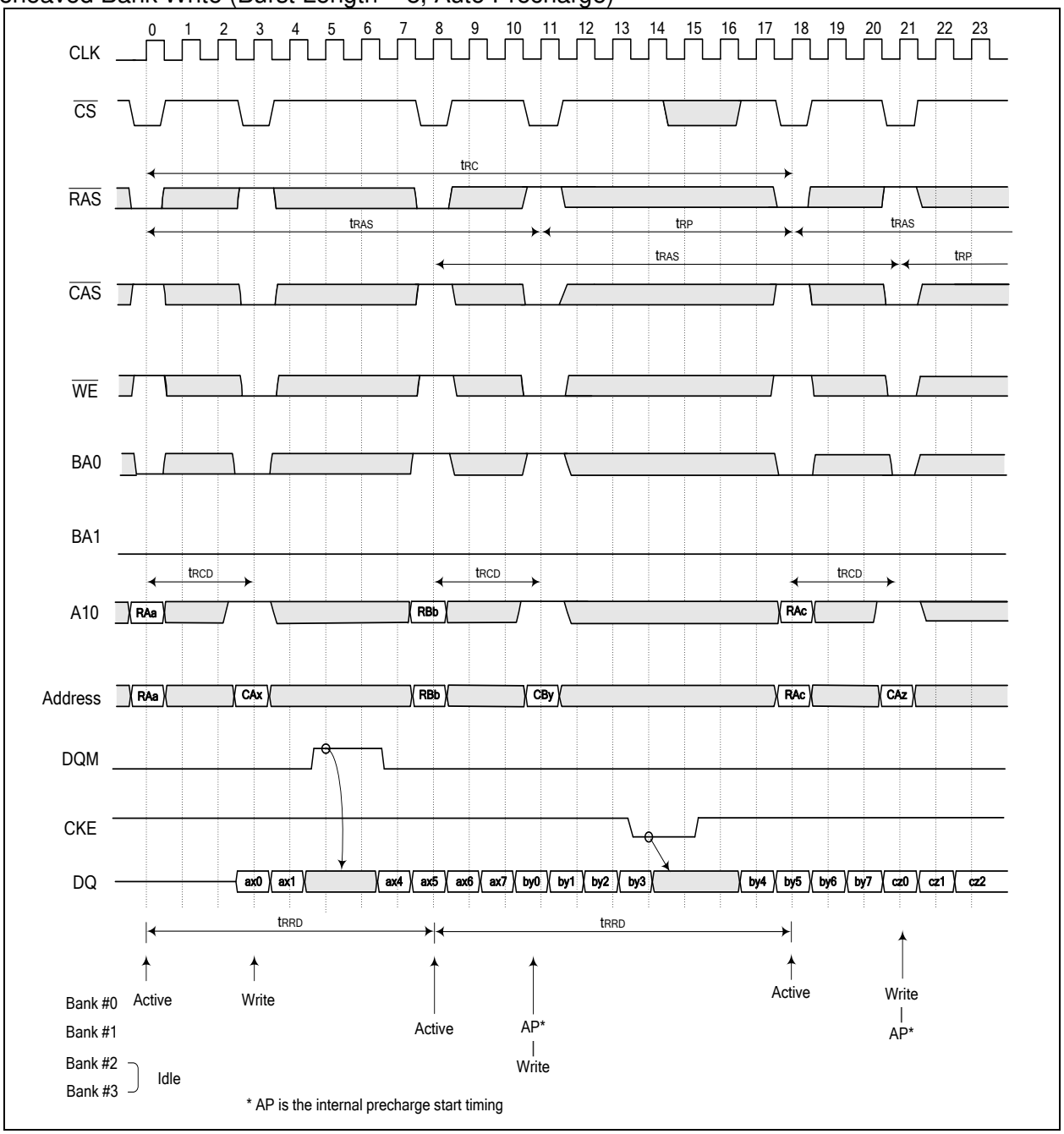
10.4 Interleaved Bank Read (Burst Length = 8, $\overline{CAS}$ Latency = 3, Auto Precharge)



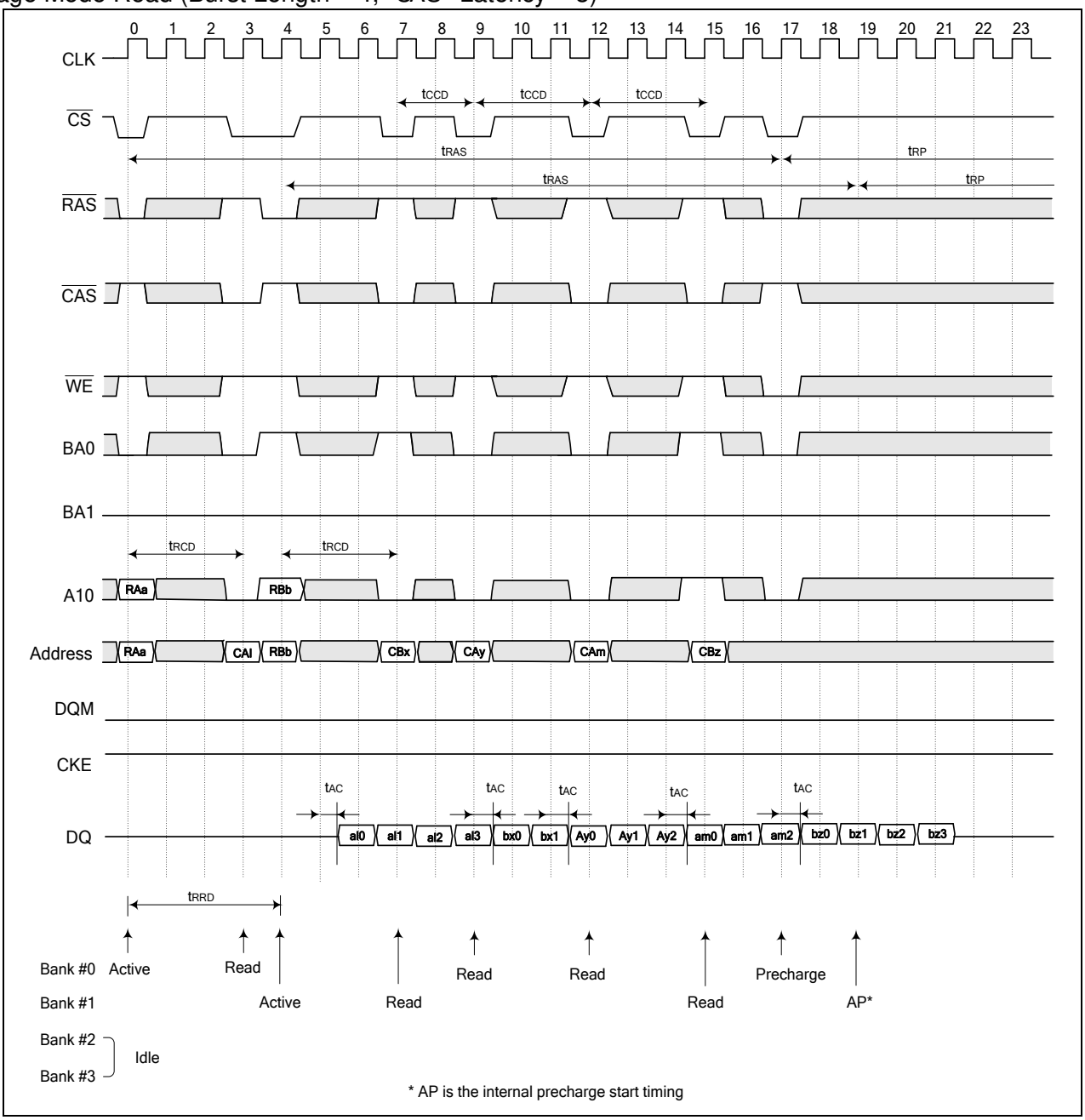
10.5 Interleaved Bank Write (Burst Length = 8)



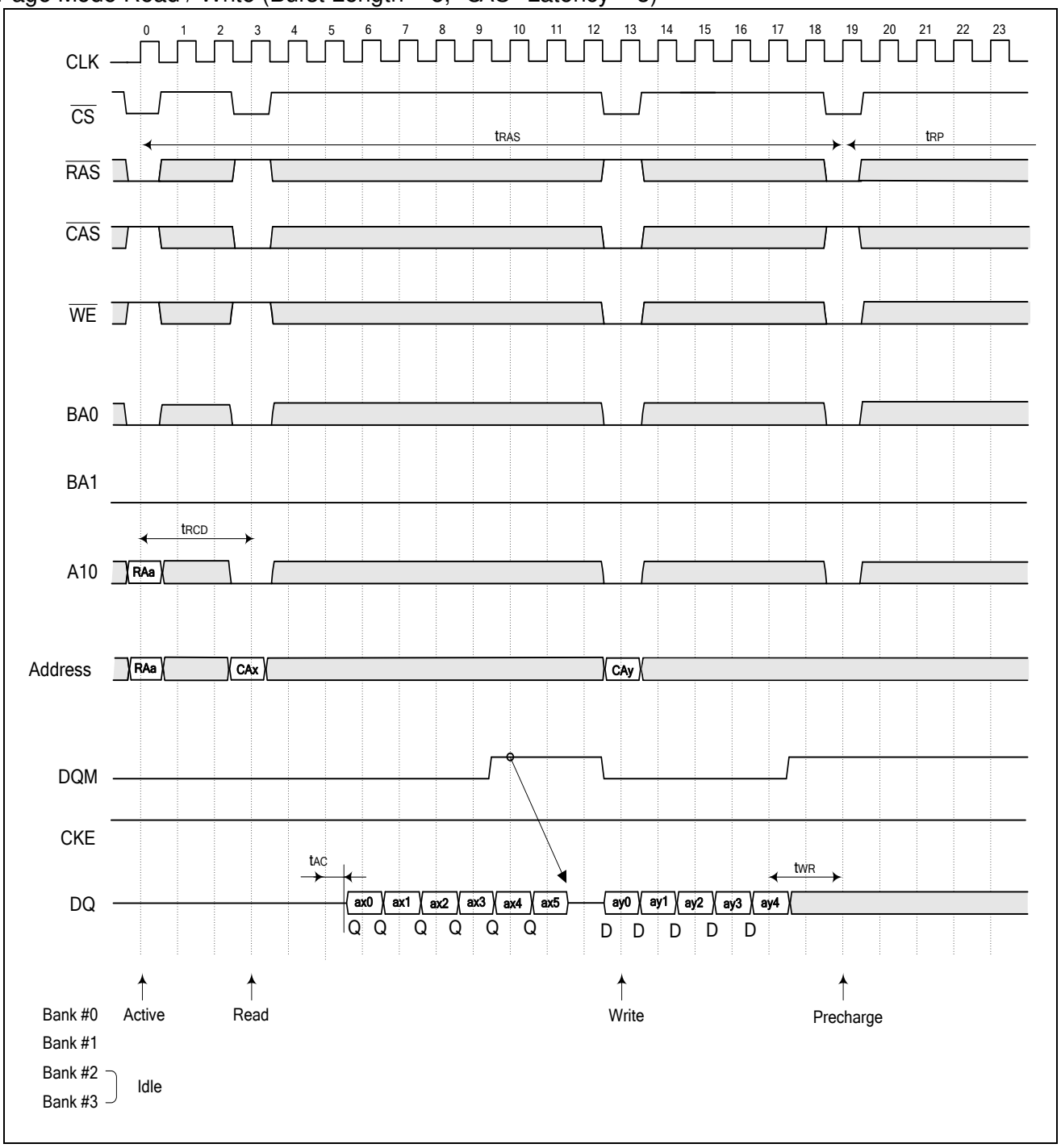
10.6 Interleaved Bank Write (Burst Length = 8, Auto Precharge)



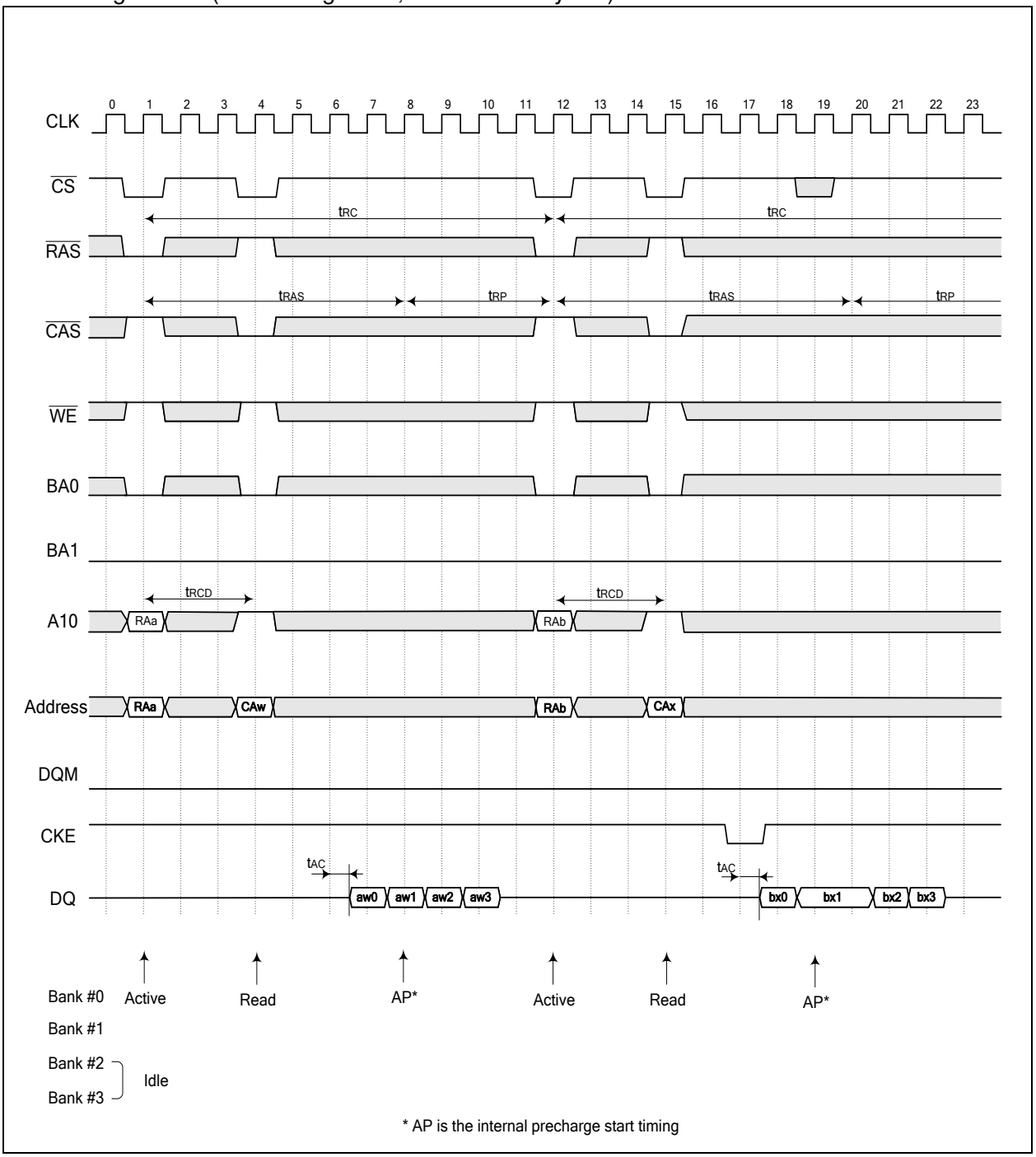
10.7 Page Mode Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



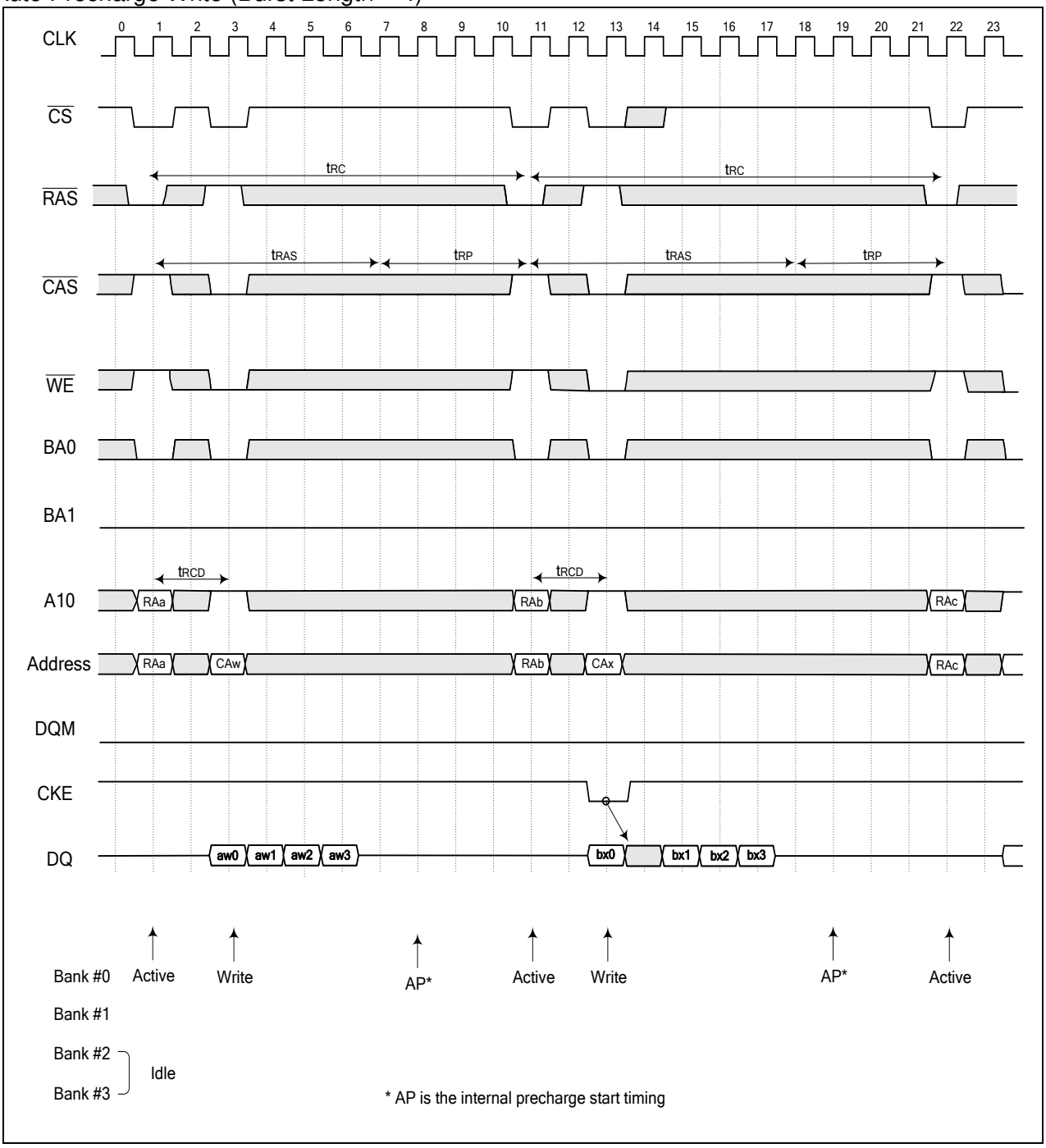
10.8 Page Mode Read / Write (Burst Length = 8, $\overline{CAS}$ Latency = 3)



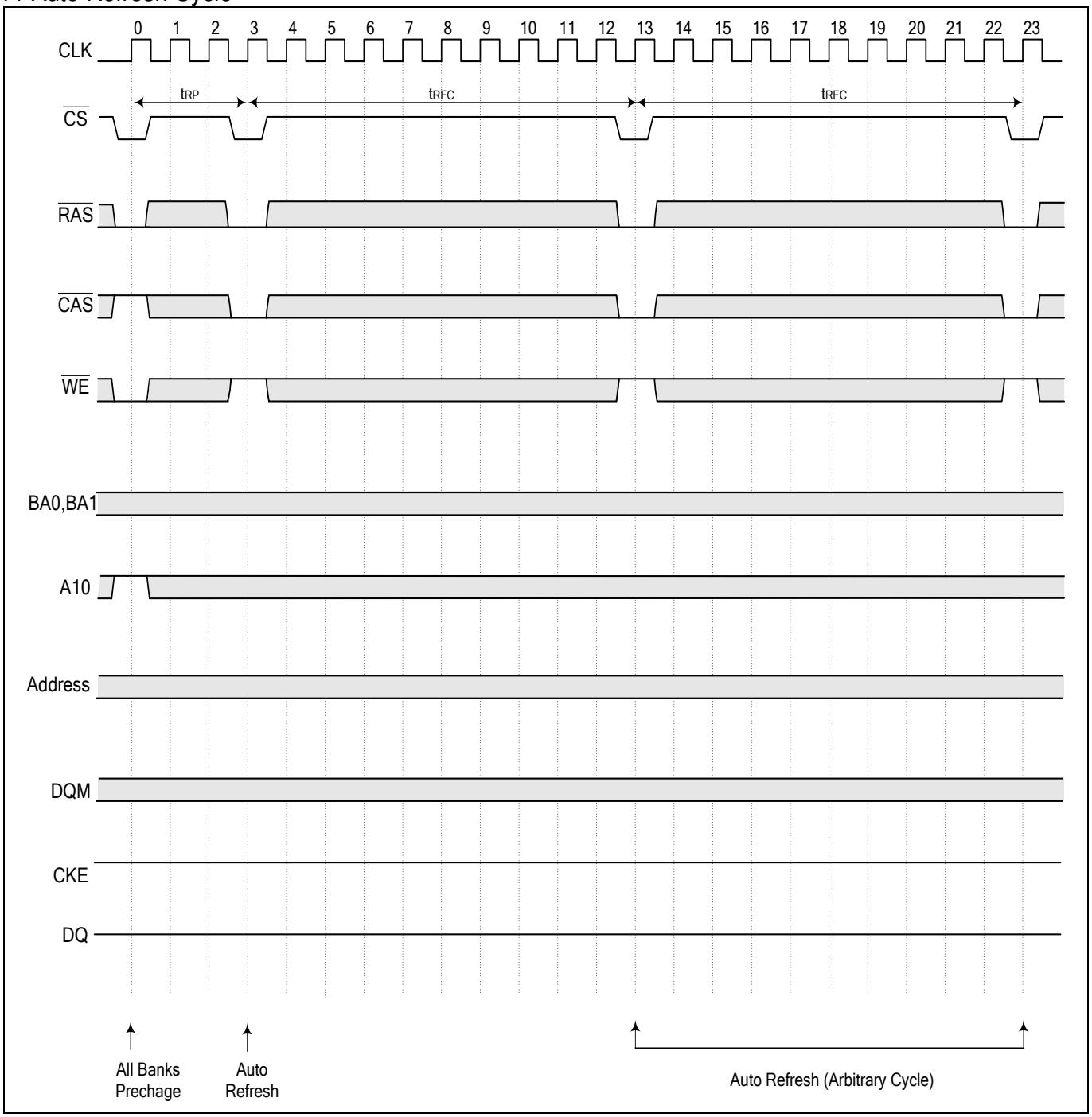
10.9 Auto Precharge Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



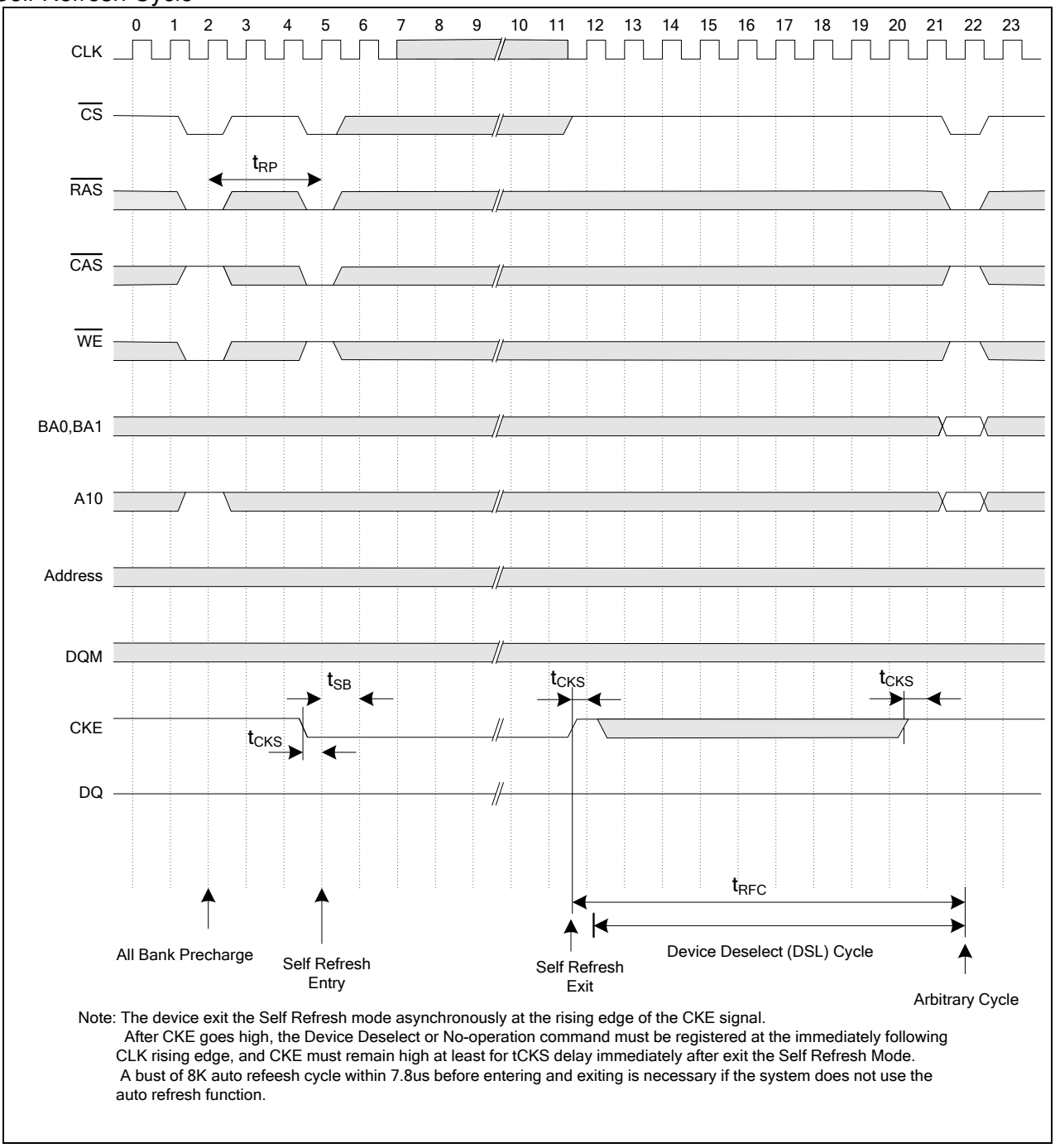
10.10 Auto Precharge Write (Burst Length = 4)



10.11 Auto Refresh Cycle

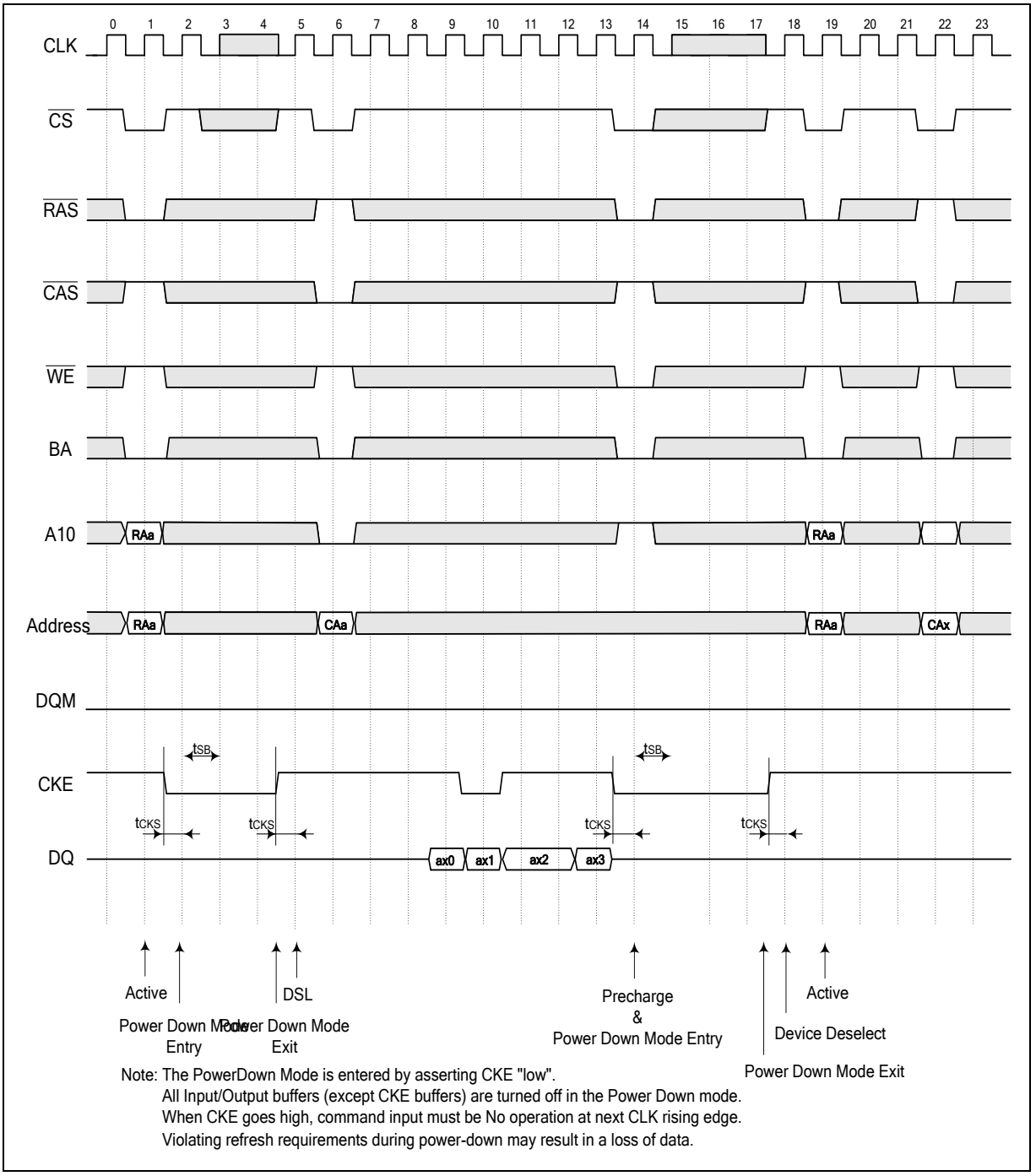


10.12 Self Refresh Cycle



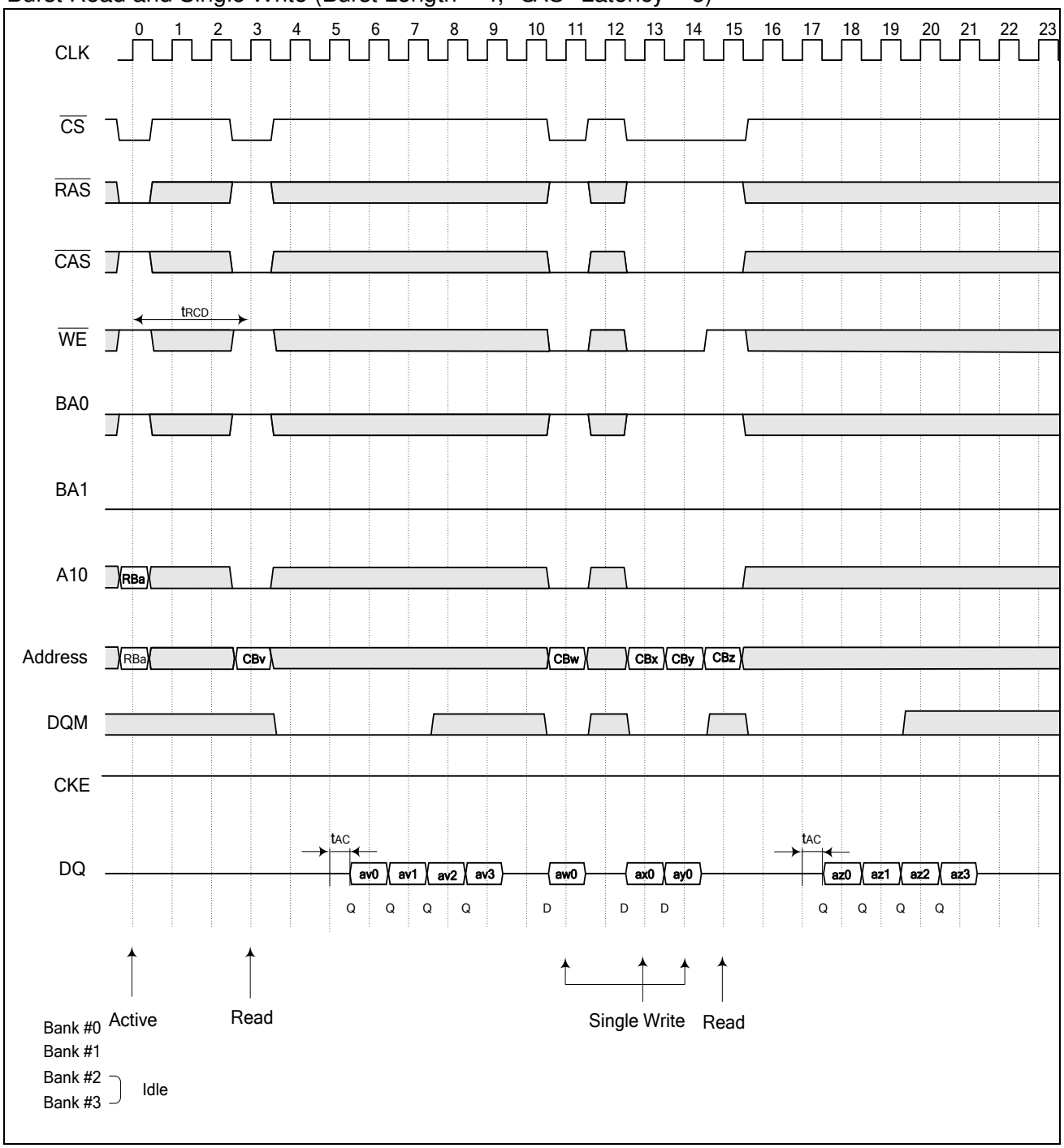
Note: The device exit the Self Refresh mode asynchronously at the rising edge of the CKE signal.
After CKE goes high, the Device Deselect or No-operation command must be registered at the immediately following CLK rising edge, and CKE must remain high at least for tCKS delay immediately after exit the Self Refresh Mode.
A bust of 8K auto refeesh cycle within 7.8us before entering and exiting is necessary if the system does not use the auto refresh function.

10.13 Power Down Mode

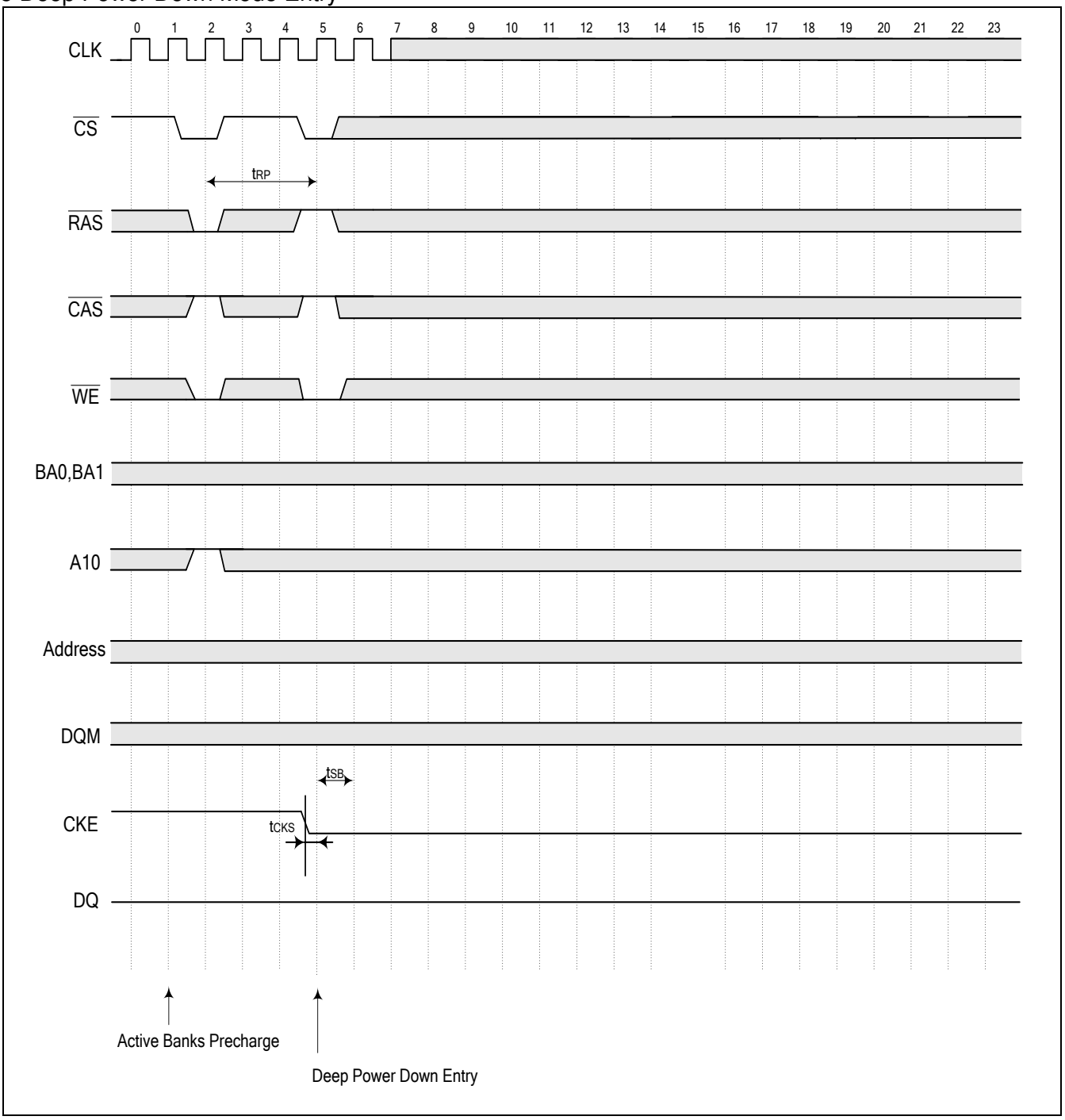


Note: The PowerDown Mode is entered by asserting CKE "low".
All Input/Output buffers (except CKE buffers) are turned off in the Power Down mode.
When CKE goes high, command input must be No operation at next CLK rising edge.
Violating refresh requirements during power-down may result in a loss of data.

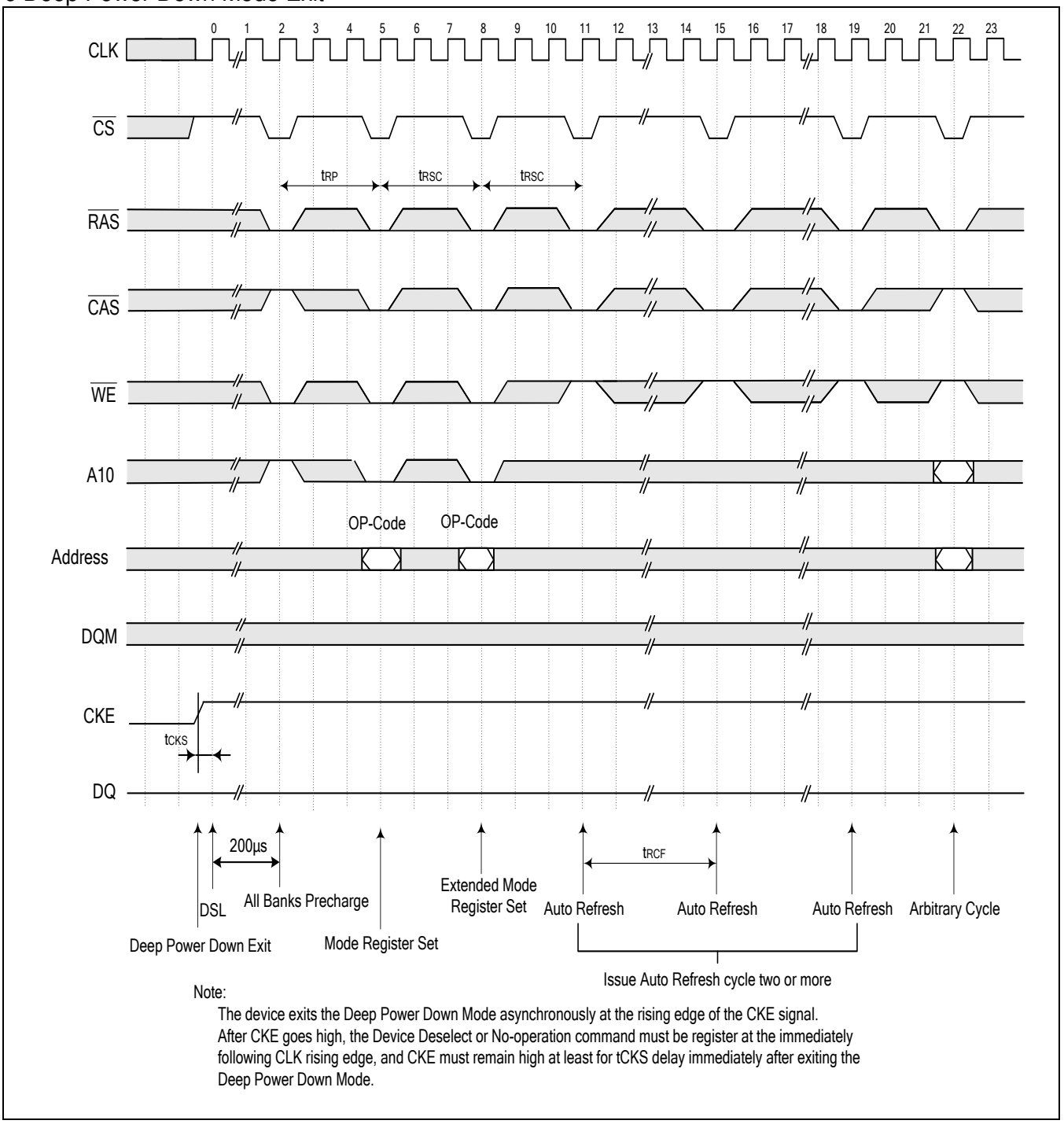
10.14 Burst Read and Single Write (Burst Length = 4, $\overline{CAS}$ Latency = 3)



10.15 Deep Power Down Mode Entry



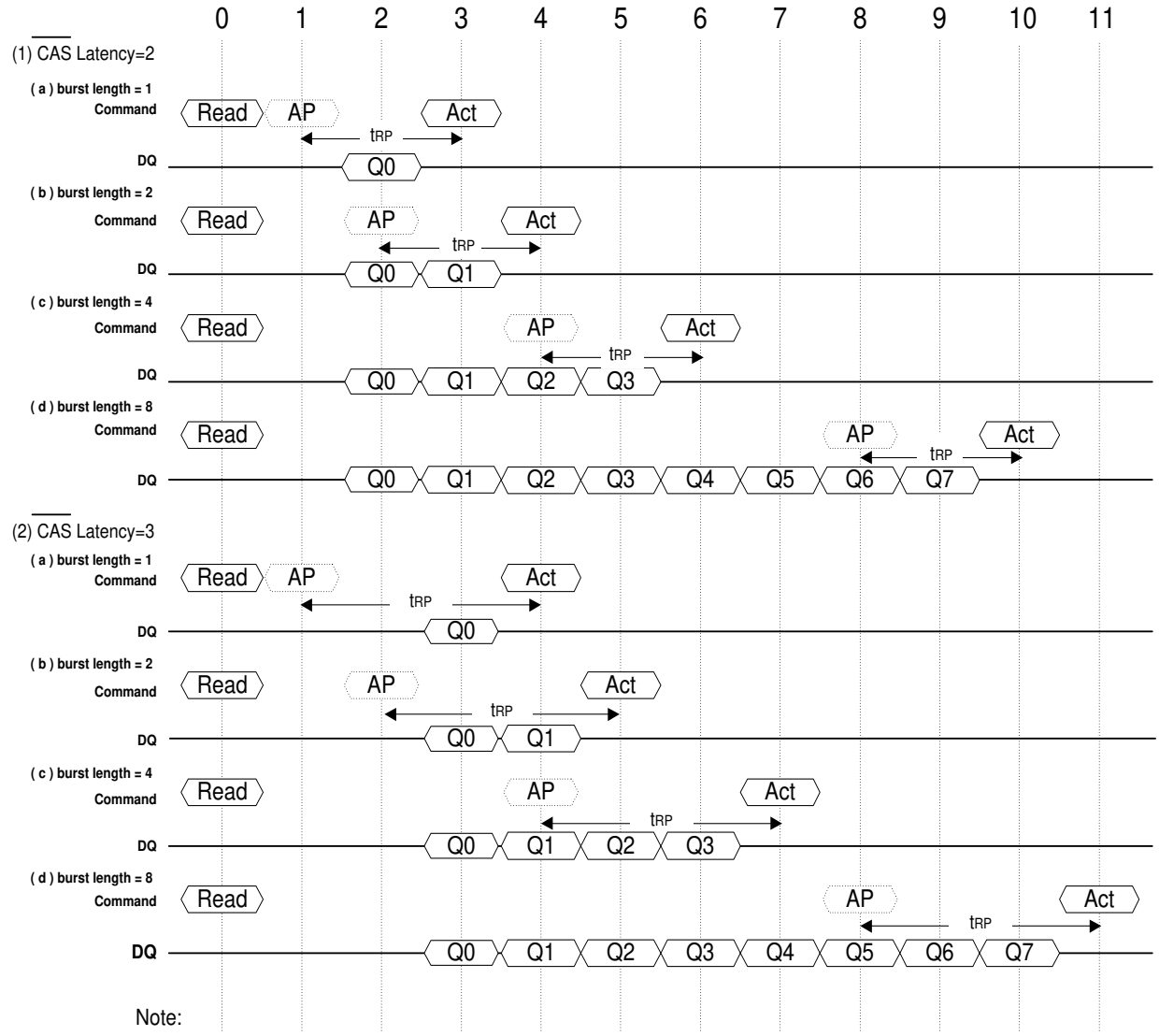
10.16 Deep Power Down Mode Exit



Note:

The device exits the Deep Power Down Mode asynchronously at the rising edge of the CKE signal. After CKE goes high, the Device Deselect or No-operation command must be register at the immediately following CLK rising edge, and CKE must remain high at least for tCKS delay immediately after exiting the Deep Power Down Mode.

10.17 Auto Precharge Timing (Read Cycle)



Note:

Read — represents the Read with Auto precharge command.

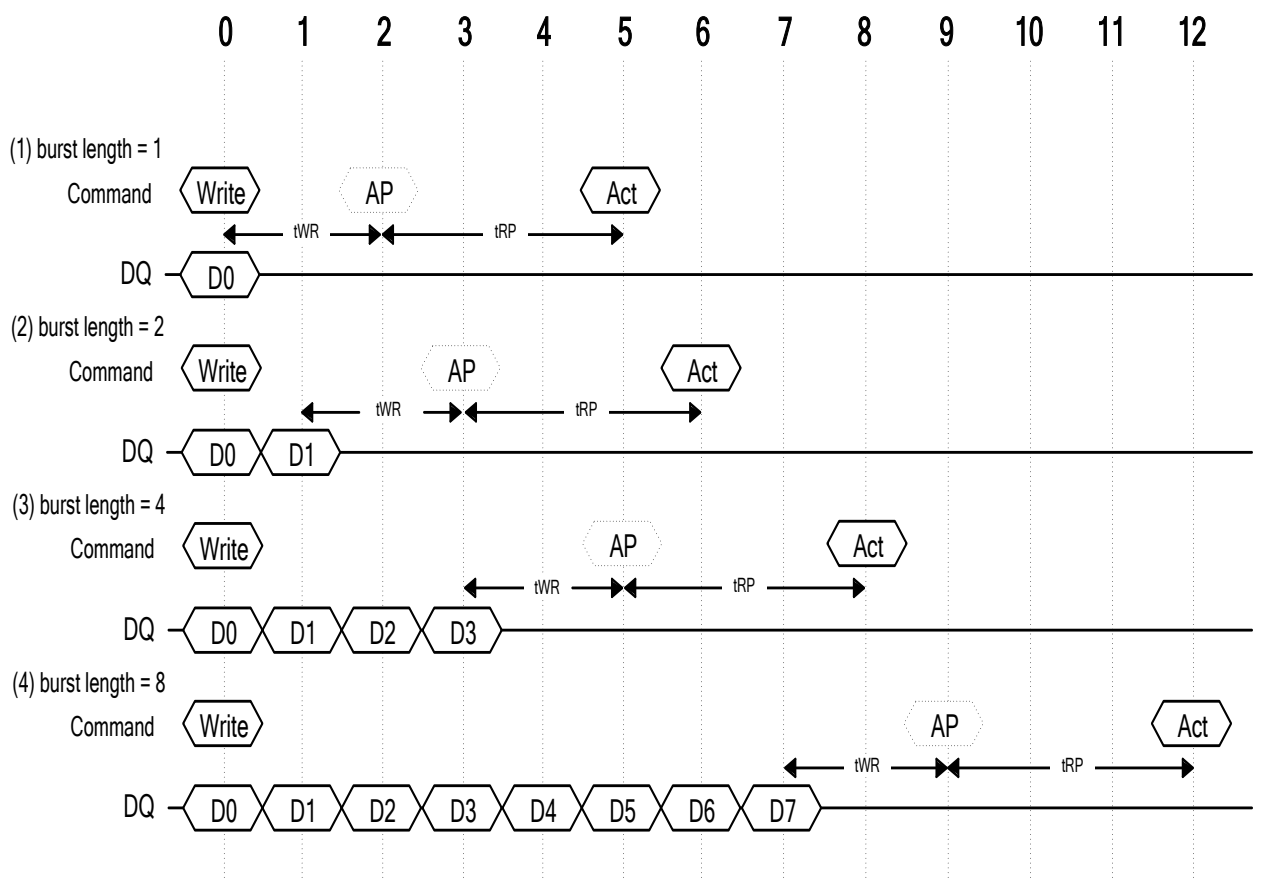
AP — represents the start of internal precharging.

Act — represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS (min).

"Dn" = Write data, and "Qn" = Read data

10.18 Auto Precharge Timing (Write Cycle)



Note: Wirte represents the Write with Auto precharge command.

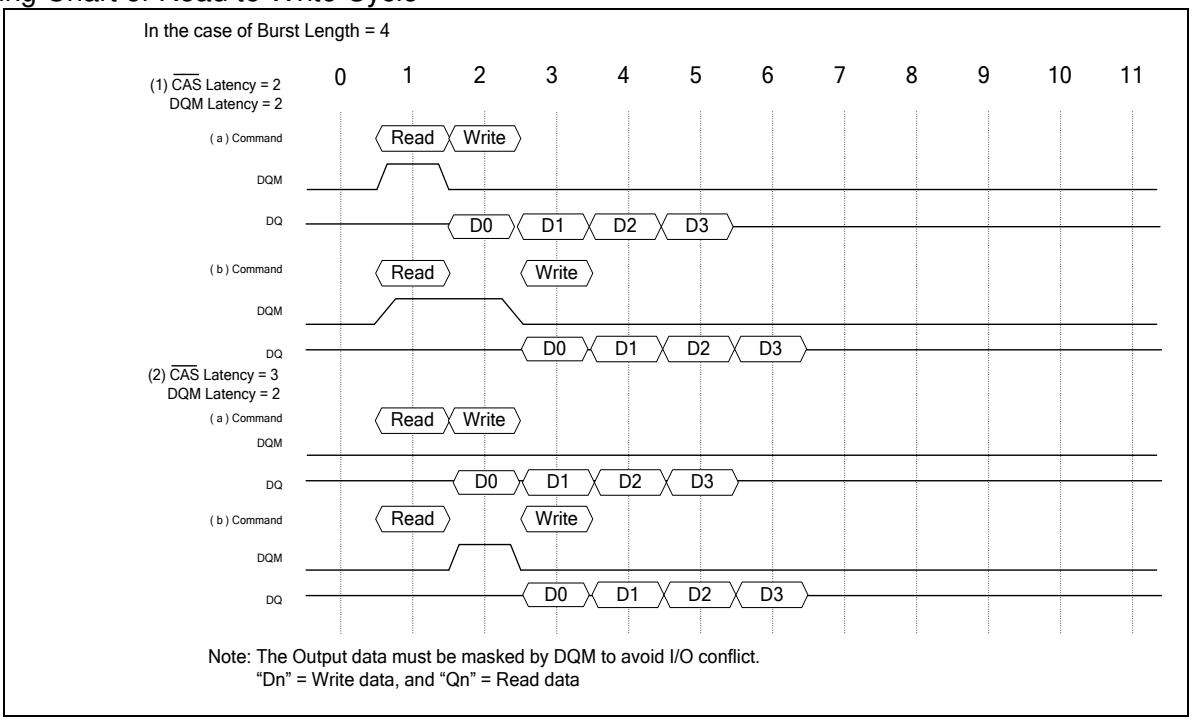
AP represents the start of internal precharging.

Act represents the Bank Activate command.

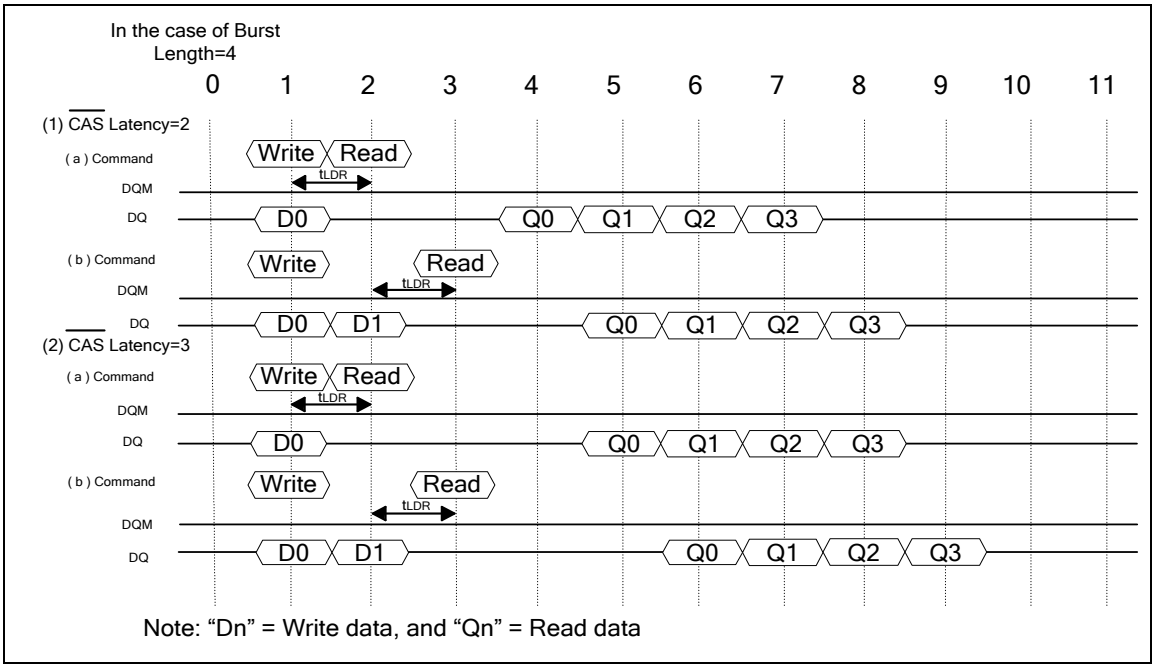
When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS (min).

"Dn" = Write data, and "Qn" = Read data

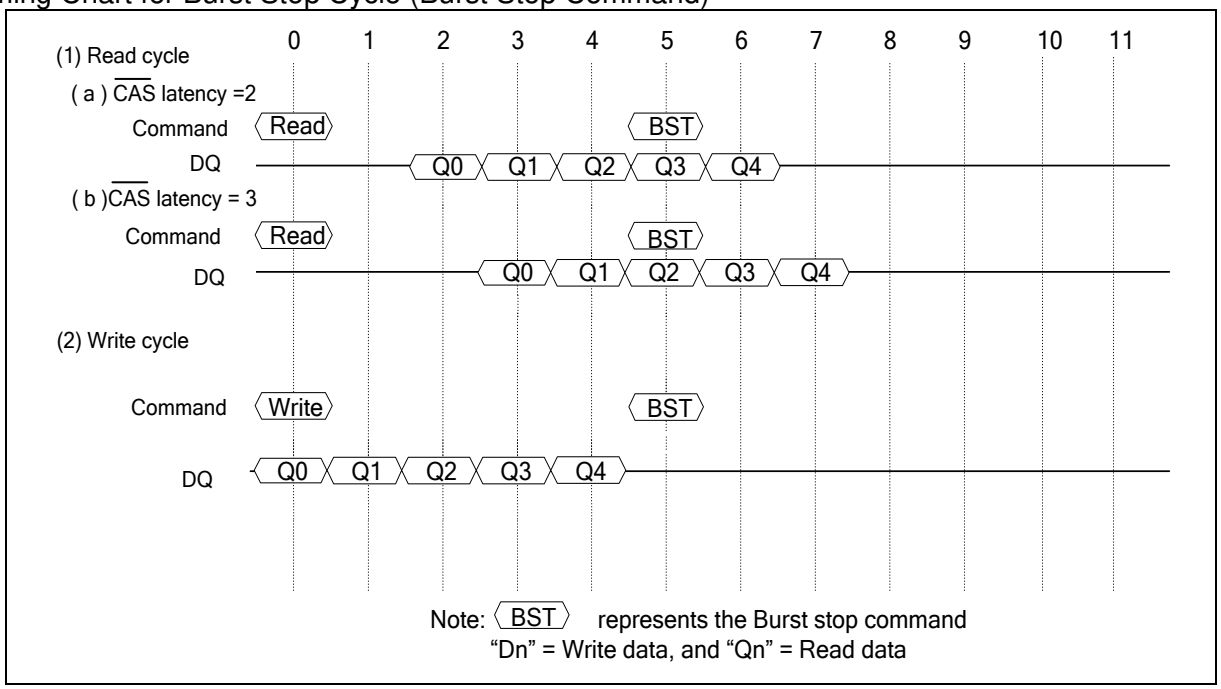
10.19 Timing Chart of Read to Write Cycle



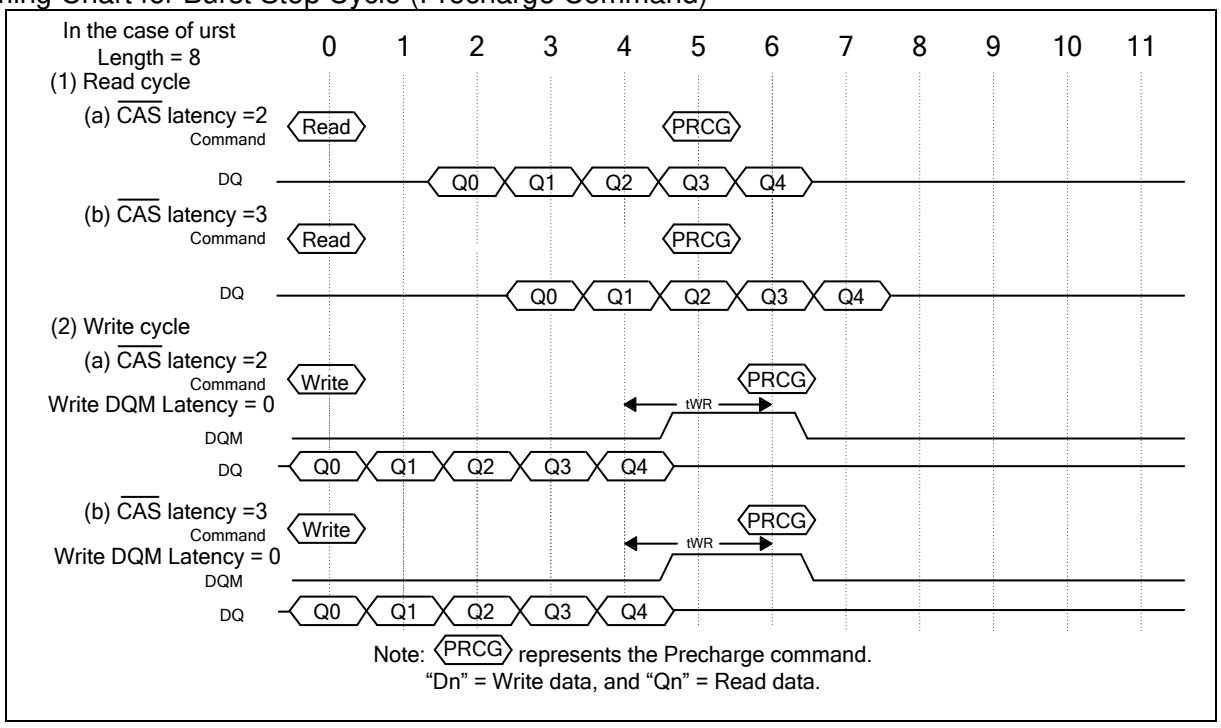
10.20 Timing Chart for Write to Read Cycle



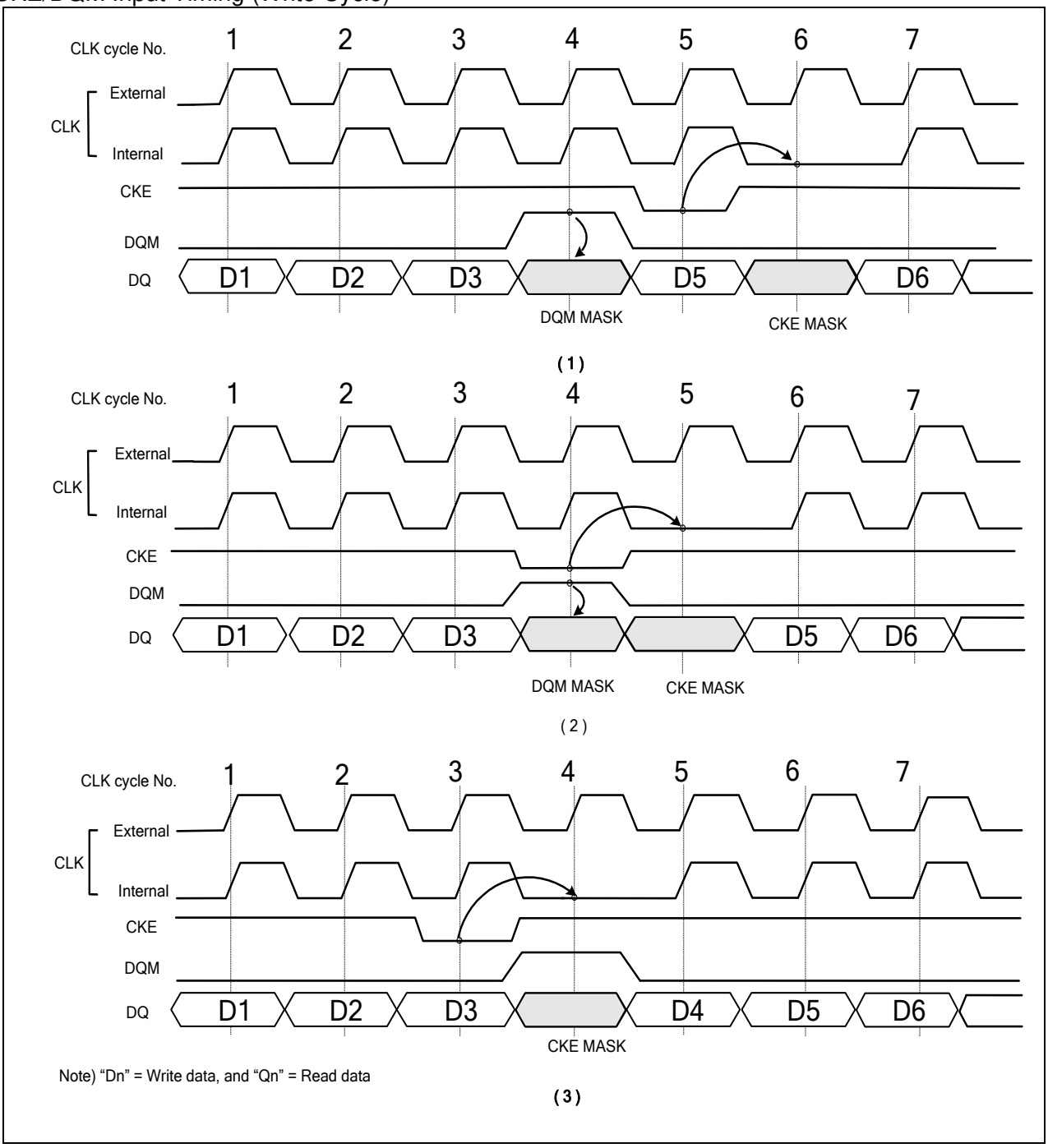
10.21 Timing Chart for Burst Stop Cycle (Burst Stop Command)



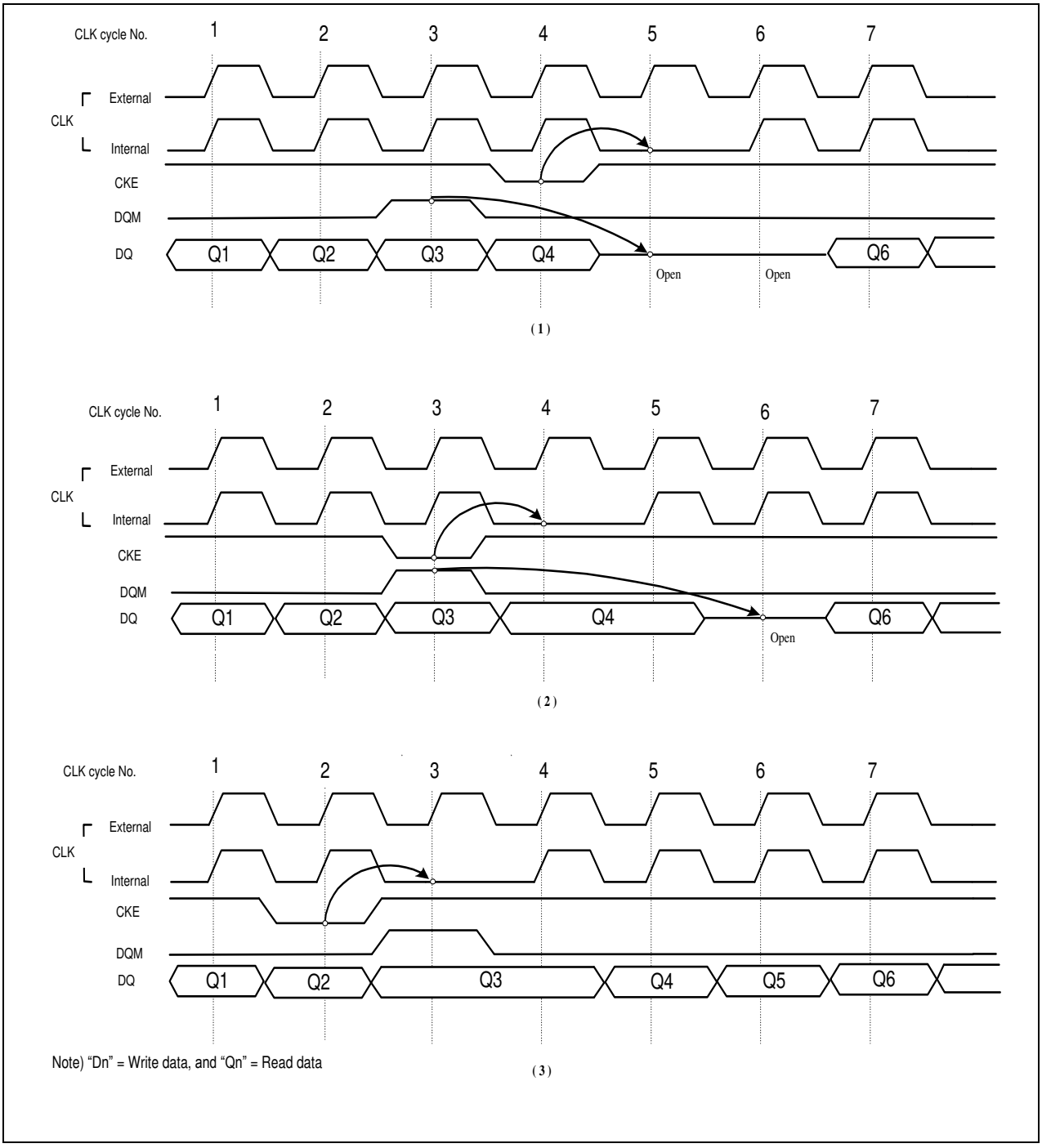
10.22 Timing Chart for Burst Stop Cycle (Precharge Command)



10.23 CKE/DQM Input Timing (Write Cycle)



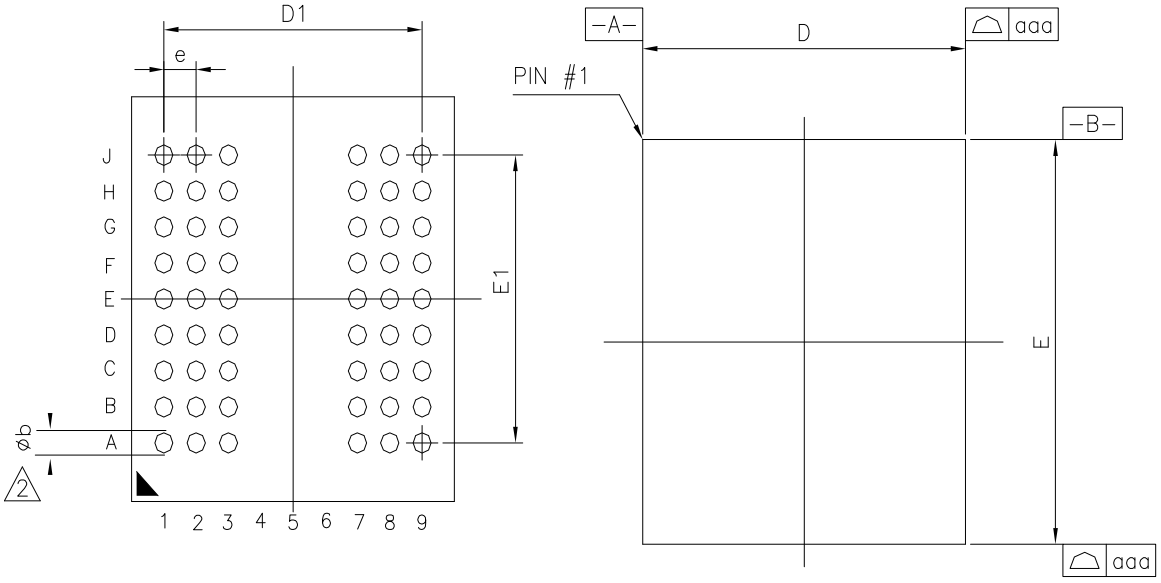
10.24 CKE/DQM Input Timing (Read Cycle)



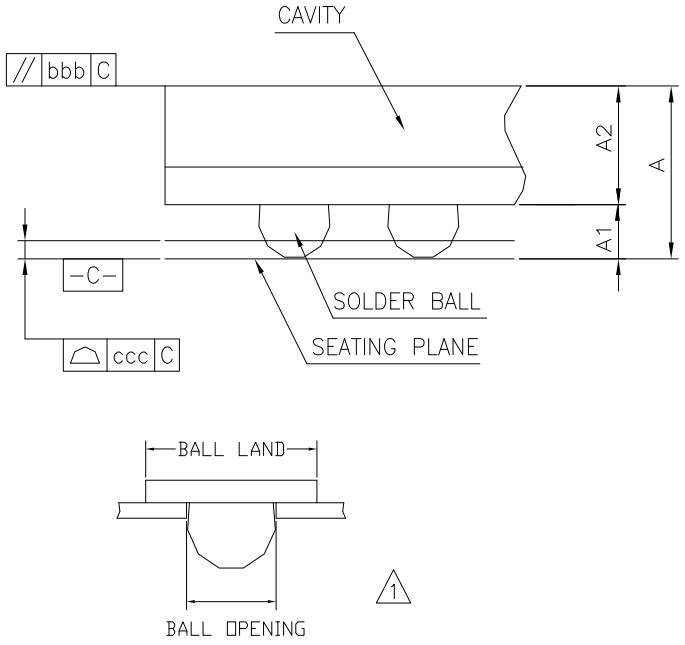
11. PACKAGE DIMENSION

11.1 : LPSDR X 16

VBGA 54Ball (8X9 MM^2, Ball pitch:0.8mm)



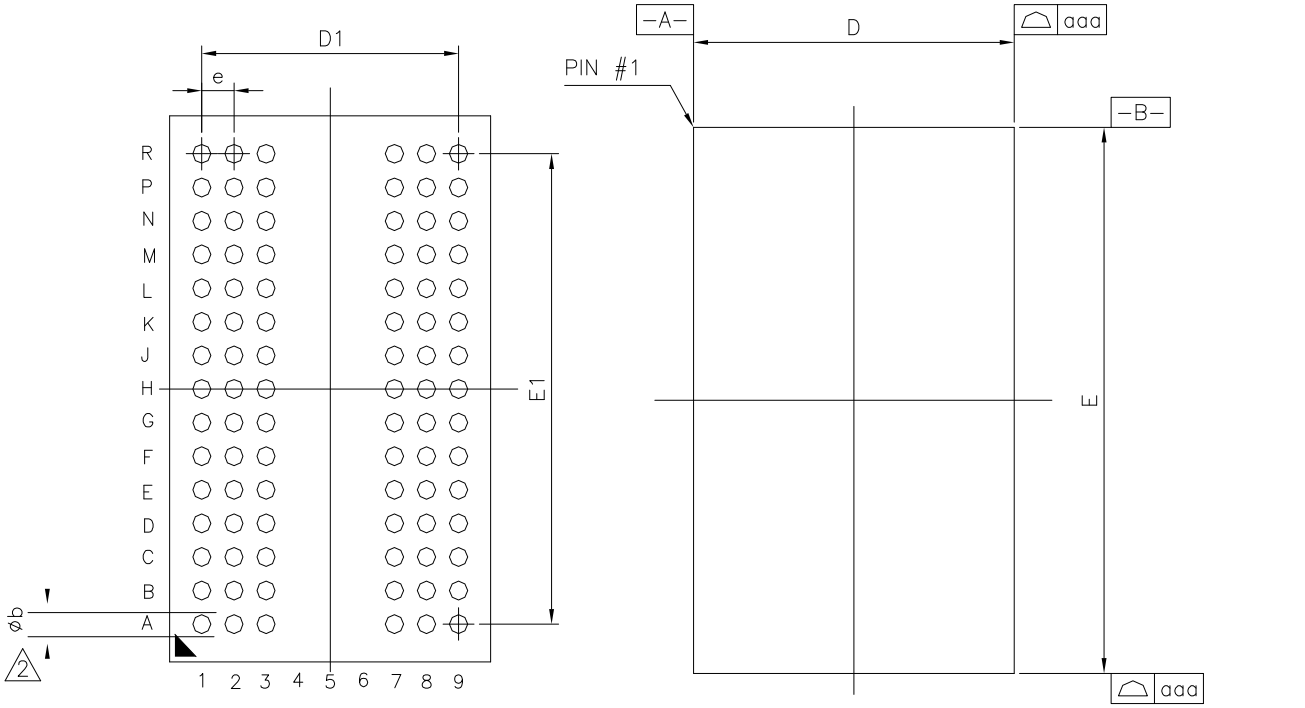
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.025	---	---	0.040
A1	0.275	0.300	0.325	0.011	0.012	0.013
A2	0.61	0.66	0.71	0.024	0.026	0.028
D	7.90	8.00	8.10	0.311	0.315	0.319
E	8.90	9.00	9.10	0.350	0.354	0.358
D1	---	6.40	---	---	0.252	---
E1	---	6.40	---	---	0.252	---
e	---	0.80	---	---	0.031	---
b	0.40	0.45	0.50	0.016	0.018	0.020
aaa		0.15			0.006	
bbb		0.20			0.008	
ccc		0.12			0.005	



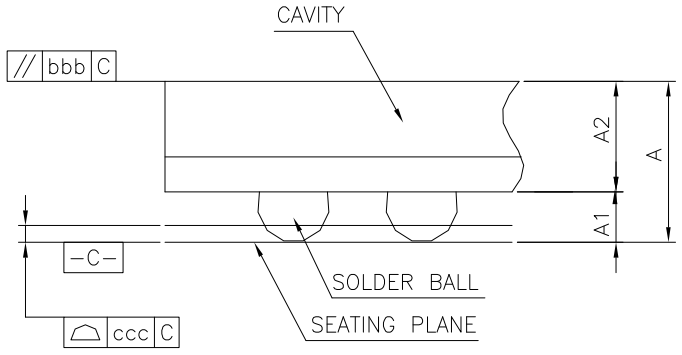
Note:
1. Ball land:0.5mm. Ball opening:0.4mm. PCB Ball land suggested ≦0.4mm
2. Dimensions apply to Solder Balls Post-Reflow.The Pre-Reflow diameter is 0.42 on a 0.4 SMD Ball Pad

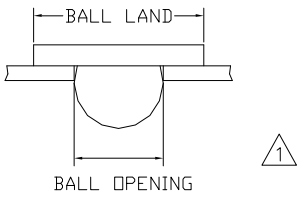
11.2 : LPSDR X 32

VBGA90Ball (8X13 MM^2, Ball pitch:0.8mm)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.025	---	---	0.040
A1	0.275	0.300	0.325	0.011	0.012	0.013
A2	0.61	0.66	0.71	0.024	0.026	0.028
D	7.90	8.00	8.10	0.311	0.315	0.319
E	12.90	13.00	13.10	0.508	0.512	0.516
D1	---	6.40	---	---	0.252	---
E1	---	11.20	---	---	0.441	---
e	---	0.80	---	---	0.031	---
b	0.40	0.45	0.50	0.016	0.018	0.020
aaa		0.15			0.006	
bbb		0.20			0.008	
ccc		0.12			0.005	

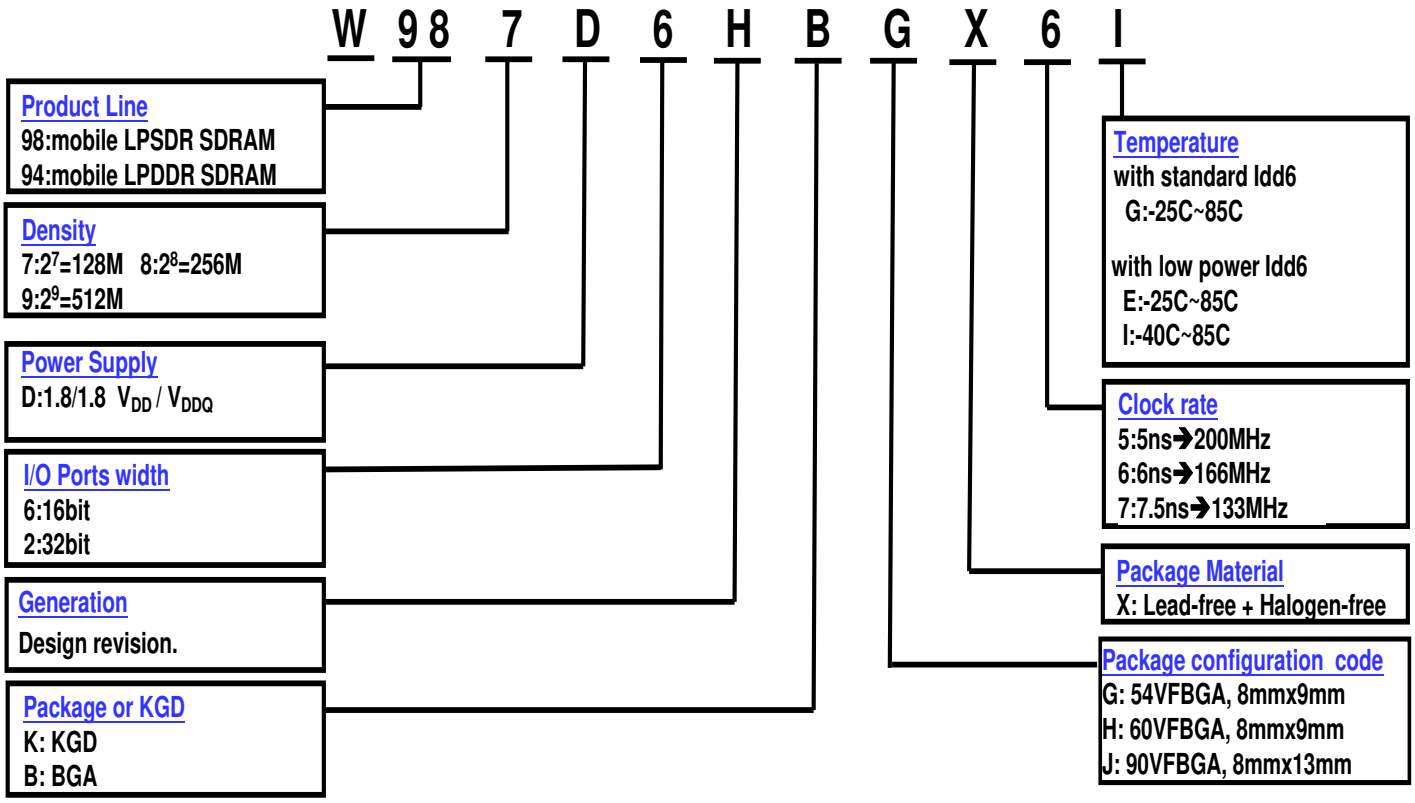




Note:
1. Ball land:0.5mm. Ball opening:0.4mm. PCB Ball land suggested ≦0.4mm
2. Dimensions apply to Solder Balls Post-Reflow. The Pre-Reflow diameter is 0.42 on a 0.4 SMD Ball Pad.

12.ORDERING INFORMATION

Mobile LPDDR/LPSDR SDRAM Package Part Numbering



Part number	VDD/VDDQ	I/O width	Package	Others
W987D6HBGX6I	1.8V/1.8V	16	54VFBGA	166MHz, -40~85C, Low Power
W987D6HBGX6E	1.8V/1.8V	16	54VFBGA	166MHz, -25~85C, Low Power
W987D6HBGX7I	1.8V/1.8V	16	54VFBGA	133MHz, -40~85C, Low Power
W987D6HBGX7E	1.8V/1.8V	16	54VFBGA	133MHz, -25~85C, Low Power
W987D6HBGX7G	1.8V/1.8V	16	54VFBGA	133MHz, -25~85C
W987D2HBGX6I	1.8V/1.8V	32	90VFBGA	166MHz, -40~85C, Low Power
W987D2HBGX6E	1.8V/1.8V	32	90VFBGA	166MHz, -25~85C, Low Power
W987D2HBGX7I	1.8V/1.8V	32	90VFBGA	133MHz, -40~85C, Low Power
W987D2HBGX7E	1.8V/1.8V	32	90VFBGA	133MHz, -25~85C, Low Power
W987D2HBGX7G	1.8V/1.8V	32	90VFBGA	133MHz, -25~85C

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01-001	04/29/2011	All	Product datasheet for customer.
A01-002	06/09/2011	9~11 66	Update IDD4 value , Add Normal power grade & PASR. Update ordering info.

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