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May 2013



FAN2502 / FAN2503 150 mA CMOS LDO Regulator

Features

- Ultra-Low Power Consumption
- 150 mV Dropout Voltage at 150 mA
- · 25 μA Ground Current at 150 mA
- Enable / Shutdown Control
- SOT23-5 package
- Thermal Limiting
- · 300 mA Peak Current

Applications

- Mobile Phones and Accessories
- · Portable Cameras and Video Recorders
- · Laptop, Notebook, and Palmtop Computers

Description

The FAN2502 / 03 family of micropower low-dropout voltage regulators utilize CMOS technology to offer a new level of cost-effective performance in mobile handsets, laptop and notebook portable computers, and other portable devices. Features include extremely low power consumption, low shutdown current, low dropout voltage, exceptional loop stability able to accommodate a wide variety of external capacitors, and a compact SOT23-5 surface-mount package. The FAN2502 / 03 family offers significant improvements over older BiCMOS designs and is pin-compatible with many popular devices. The output is thermally protected against overload.

The FAN2502 and FAN2503 devices are distinguished by the assignment of pin 4:

FAN2502-XX: pin 4 – BYP, to which a bypass capacitor

may be connected for optimal noise performance. Output

voltage is fixed, indicated by the suffix XX.

FAN2503-XX: pin $4 - \overline{\text{ERR}}$, a flag that indicates that the output voltage has dropped below the specified minimum due to a fault condition.

The standard fixed output voltages available are 2.5 V and 3.3 V.

Ordering Information

Part Number	V _{OUT}	Pin 4 Function	Top Mark	Package	Packing Method
FAN2502S25X	2.5	Bypass	AEE	SOT-23 5L	Tape and Reel
FAN2503S33X	3.3	Error Output	AF3	SOT-23 5L	Tape and Reel

Tape and Reel Information

Quantity	Reel Size	Width
3000	7 inches	8 mm

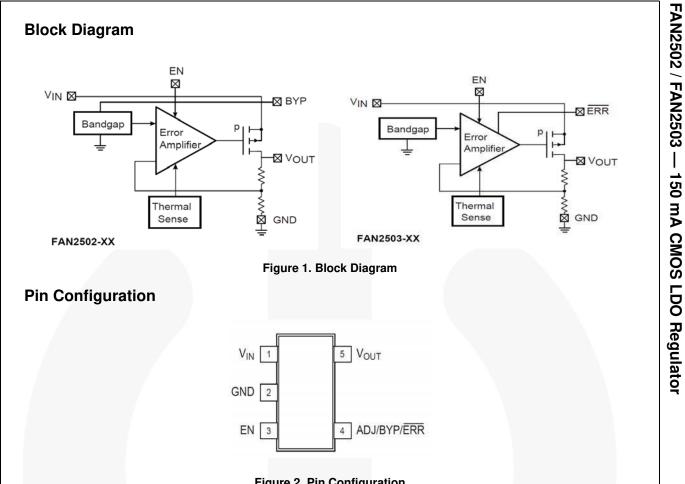


Figure 2. Pin Configuration

Pin No.	FAN2502	FAN2503
1.	V _{IN}	V _{IN}
2.	GND	GND
3.	EN	EN
4.	BYP	ERR
5.	V _{OUT}	V _{OUT}

Pin Descriptions

Pin Name	Pin No.	Туре	Functional Description
BYP	4	Passive	FAN2502-XX Bypass. Connect a 470 pF capacitor for noise reduction.
			FAN2503-XX Error. Error flag output.
ERR	4	Open drain	0: Output voltage < 95% of nominal
			1: Output voltage > 95% of nominal
			Enable
EN	3	Digital Input	0: Shutdown V _{OUT}
			1: Enable V _{OUT}
V _{IN}	1	Power In	Voltage Input. Supply voltage input.
V _{OUT}	5	Power Out	Voltage Output. Regulated output voltage.
GND	2	Power	Ground

Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Min.	Max.	Unit
Power Supply Voltages			
V _{IN} (Measured to GND)	0	7	V
Enable Input (EN)			
Applied Voltage (Measured to GND) ⁽²⁾	0	7	V
ERR Output			
Applied Voltage (Measured to GND) ⁽²⁾	0	7	V
Power			
Dissipation ⁽³⁾	Inter	nally Limited	
Temperature			
Junction	-65	150	°C
Lead Soldering (5 s)		260	°C
Storage	-65	150	°C
Electrostatic Discharge ⁽⁴⁾	4		kV

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Recommended Operating Conditions are not exceeded.

2. Applied voltage must be current limited to specified range.

3. Based upon thermally limited junction temperature:

$$P_{D} = \frac{T_{J(max)} - T_{A}}{\Theta_{JA}}$$

4. Human Body Model is 4 kV minimum using Mil Std. 883E, method 3015.7. Machine Model is 400 V minimum using JEDEC method A115-A.

Recommended Operating Conditions

The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Nom.	Max.	Unit
V _{IN}	Input Voltage Range	2.7		6.5	V
V _{OUT}	Output Voltage Range, Adjustable	V _{REF}		V _{IN-} V _{DO}	V
V _{EN}	Enable Input Voltage	0		V _{IN}	V
V _{ERR}	ERR Flag Voltage			V _{IN}	V
TJ	Junction Temperature	-40		+125	°C
θ_{JA}	Thermal Resistance, Junction to Ambient		220		°C/W
θ_{JC}	Thermal Resistance, Junction to Case		130		°C/W

FAN2502
/ FAN2503
— 150 mA
150 mA CMOS LDO
O Regulator

Electrical Characteristics^(5, 6)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
Regulator	•					
		I _{OUT} = 100 μA		2.5	4.0	mV
V	Dran Out Maltaga	I _{OUT} = 50 mA		50	75	mV
V _{DO}	Drop Out Voltage	I _{OUT} = 100 mA		100	140	mV
		I _{OUT} = 150 mA		150	180	mV
ΔV _O	Output Voltage Accuracy		-2		2	%
I _{GND}	Ground Pin Current	I _{OUT} = 150 mA			50	μA
Protection	·		•		•	
	Current Limit	Thermally Protected				
I _{GSD}	Shutdown Current	EN = 0 V			1	μΑ
T _{SH}	Thermal Protection Shutdown Temperature		150			°C
E _{TL}	ERR Trip Level	FAN2503 Only	90	95	99	%
Enable Inpu	ut					
V _{IL}	Logic Low Voltage			1.2	0.4	V
V _{IH}	Logic High Voltage		2.0	1.4		V
I _{IH}	Input Current High				1	μΑ
lı lı	Input Current Low				1	μA

Switching Characteristics^(5, 6)

Parameter	Max.	Unit
Enable Input ⁽⁷⁾		
Response Time	500	μs
Error Flag (FAN2503)		
Response Time	3	ms

Performance Characteristics^(5, 6)

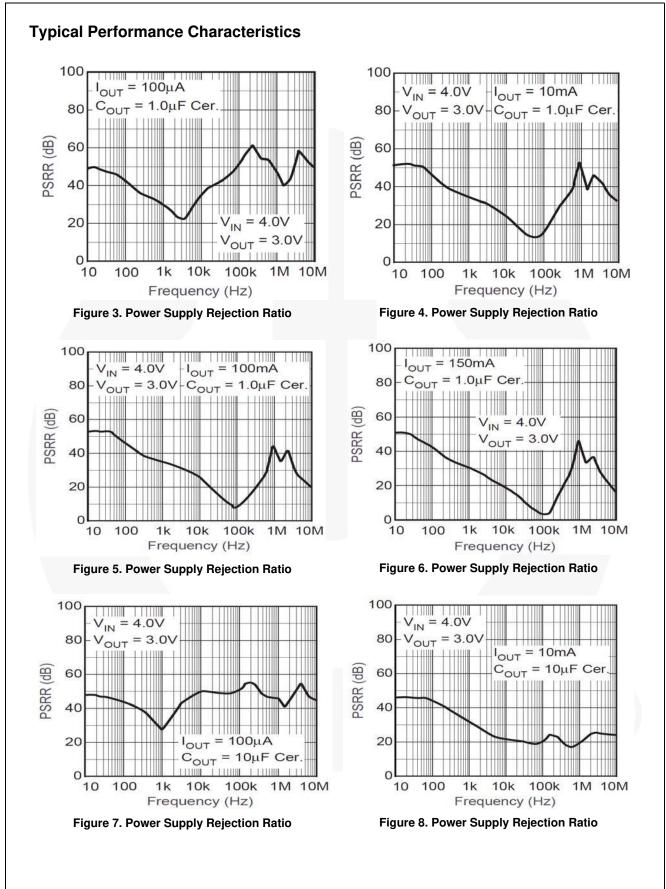
Symbol	Parameter	Conditions	Тур.	Max.	Unit
ΔV _{OUT} / ΔV _{IN}	Line Regulation	V _{IN} = (V _{OUT} + 1) to 6.5 V	0.3		% / V
ΔV _{OUT} / V _{OUT}	Load Regulation	I _{OUT} = 0.1 to 150 mA	1.0	2.0	%
	Output Noise	f = 10 Hz to 1 kHz at V _{IN} , C _{OUT} = 10 μF, C _{BYP} = 0.01 μF	< 7.00		
e _N	Output Noise	f > 10 kHz at V _{IN} , C _{OUT} = 10 μF, C _{BYP} = 0.01 μF	< 0.01		− μV /√Hz
PSRR	Power Supply Rejection	f = 120 Hz at V _{IN} , C _{OUT} = 10 μF, C _{BYP} = 0.01 μF	43		dB

Notes:

5. Unless otherwise stated; T_A = 25°C, V_{IN} = V_{OUT} + 1 V, I_{OUT} = 100 μA , and V_{IH} > 2.0 V.

6. Bold values indicate $-40 \le T_J \le 125^{\circ}C$.

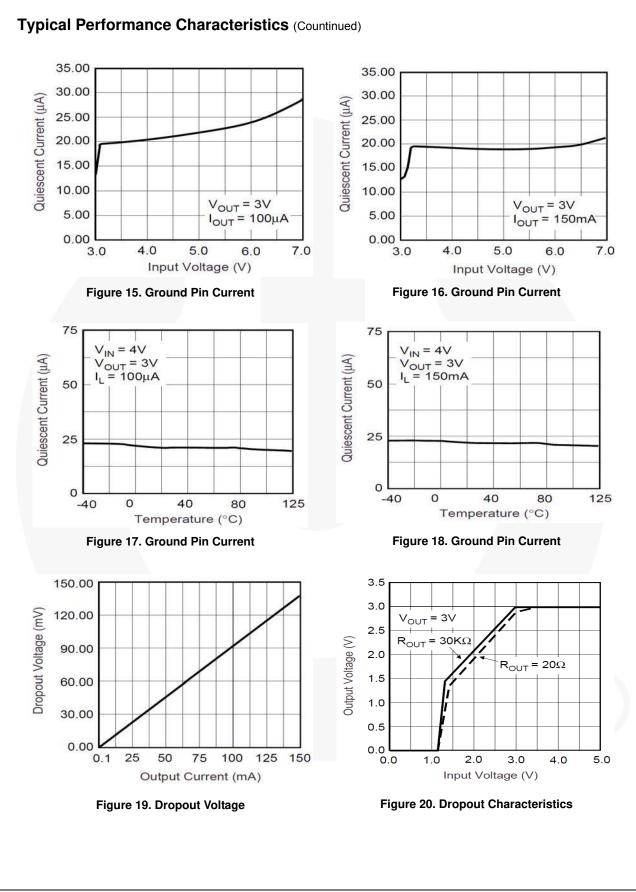
7. When using repeated cycling.



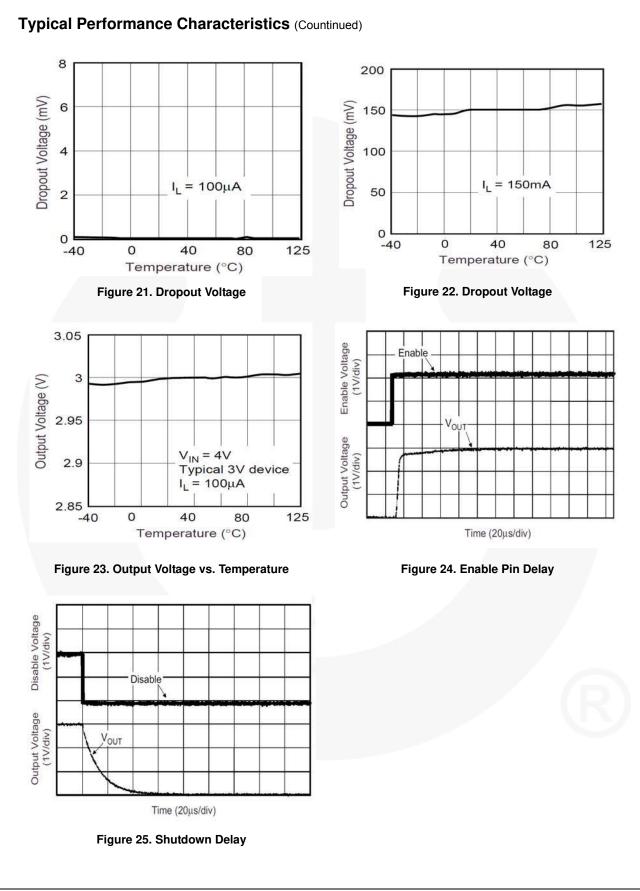
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Typical Performance Characteristics (Countinued) 100 100 = 100mA = 150mA OUT OUT $C_{OUT} = 10 \mu F Cer$ $C_{OUT} = 10 \mu F Cer$ 80 80 $V_{IN} = 4.0V$ = 4.0 VIN PSRR (dB) PSRR (dB) 60 V_{OUT} = 3.0\ V_{OUT} = 3.0\ 60 40 40 20 20 0 0 10k 100k 1M 10M 10k 100k 1M 10M 10 100 1k 10 100 1kFrequency (Hz) Frequency (Hz) Figure 9. Power Supply Rejection Ratio Figure 10. Power Supply Rejection Ratio 70 70 60 60 10mA I_{OUT} = 100μA = 100µA OUT PSRR (dB) 50 50 PSRR (dB) * 40 40 30 30 10mA $C_{OUT} = 1.0 \mu F Cer.$ 100mA 20 20 100mA COUT = 10µF Cer 10 10 150mA 150mA 0 0 3.0 3.6 4.1 3.0 3.6 4.1 Voltage (V) Voltage (V) Figure 11. PSRR vs. Voltage Drop Figure 12. PSRR vs. Voltage Drop 10 25.00 $V_{IN} = 4V$ = 4.0V IN 1 Quiescent Current (µA) 23.00 V_{OUT} = 3V 3.0 = OUT Noise (µV//Hz) 0.1 21.00 0.01 19.00 $C_{OUT} = 1.0 \mu F$ 0.001 17.00 $= 0.01 \mu$ ΒΥΡ = 10μΑ 0.0001 15.00 100 10 1k 10k 100k 1M 0.1 1 10 100 Frequency (Hz) Load Current (mA) Figure 14. Ground Pin Current Figure 13. Noise Performance

FAN2502 / FAN2503 — 150 mA CMOS LDO Regulator



FAN2502 / FAN2503 — 150 mA CMOS LDO Regulator



Functional Description

Designed utilizing CMOS process technology, the FAN2502 / 03 family of products are carefully optimized for use in compact battery-powered devices. They offer a unique combination of low power consumption, extremely low dropout voltages, high tolerance for a variety of output capacitors, and the ability to disable the output to less than 1 µA under user control. In the circuit, a differential amplifier controls the current through a series-pass P-channel MOSFET, comparing the load voltage at the output with an onboard low-drift band-gap reference. The series resistance of the pass P-channel MOSFET is approximately 1 Ω , resulting in an unusually low dropout voltage under load when compared to older bipolar pass-transistor designs. Protection circuitry is provided onboard for overload conditions. If the device reaches temperatures exceeding the specified maximums, an onboard circuit shuts down the output, where it remains suspended until it has cooled before reenabling. The user can shut down the device using the Enable control pin at any time.

Careful design of the output regulator amplifier assures loop stability over a wide range of ESR values in the external output capacitor. A wide range of values and types can be accomodated, allowing the user to select a capacitor meeting space, cost, and performance requirements; and enjoy reliable operation over temperature, load, and tolerance variations.

Depending on the model selected, a number of control and status functions are available to enhance the operation of the LDO regulator. An Enable pin, available on all devices, allows the user to shut down the regulator output to conserve power, reducing supply current to less than 1 µA. The adjustable-voltage versions of the device utilize pin 4 to connect to an external voltage divider that feeds back to the regulator error amplifier, thereby setting the voltage as desired. Two other functions are available at pin 4 in the fixed-voltage versions: in noisesensitive applications, an external bypass capacitor connection is provided that allows the user to achieve optimal noise performance at the output. The error output functions as a diagnostic flag to indicate that the output voltage has dropped more than 5% below the nominal fixed voltage.

Applications Information

External Capacitors – Selection

The FAN2502/03 supports a wide variety of capacitors compared to other LDO products. An innovative design approach offers significantly reduced sensitivity to ESR (Equivalent Series Resistance), which degrades regulator loop stability in older designs. While the improvements greatly simplify the design task, capacitor quality still must be considered if the designer is to achieve optimal circuit performance. In general, ceramic capacitors offer superior ESR performance, at a lower cost and a smaller case size than tantalums. Those with X7R or Y5Vdielectric offer the best temperature coefficient characteristics. The combination of tolerance and variation over temperature in some capacitor types can result in significant variations, resulting in unstable performance over rated conditions.

Input Capacitor

An input capacitor of 2.2 μ F (nominal value) or greater, connected between the Input pin and ground, located in close proximity to the device, improves transient response and noise rejection. Higher values offer superior input ripple rejection and transient response. An input capacitor is recommended when the input source, either a battery or a regulated AC voltage, is located far from the device. Any good-quality ceramic, tantalum, or metal film capacitor gives acceptable performance; however, tantalum capacitors with a surge current rating appropriate to the application must be selected to avoid catastrophic failure.

Output Capacitor

An output capacitor is required to maintain regulator loop stability. Unlike many other LDO regulators, the FAN2502 / 03 family of products are nearly insensitve to output capacitor ESR. Stable operation is achieved with a wide variety of capacitors with ESR values ranging from 10 m Ω to 10 Ω or more. Tantalum or aluminum electrolytic, or multilayer ceramic types can all be used. A nominal value of at least 1 μ F is recommended.

Bypass Capacitor (FAN2502 Only)

In the fixed-voltage configuration, connecting a capacitor

between the Bypass pin and ground can significantly reduce noise on the output. Values ranging from 470 pF to 10 nF can be used, depending on the sensitivity to output noise in the application.

At the high-impedance Bypass pin, care must be taken in the circuit layout to minimize noise pickup, and capacitors must be selected to minimize current loading (leakage). Noise pickup from external sources can be considerable. Leakage currents into the Bypass pin directly affects regulator accuracy and should be kept as low as possible; high-quality ceramic and film types are recommended for their low leakage characteristics. Cost-sensitive applications not concerned with noise can omit this capacitor.

Control Functions

Enable Pin

Applying a voltage of 0.4 V or less at the Enable pin disables the output, reducing the quiescent output current to less than 1 μ A; while a voltage of 2.0 V or greater enables the device. If this shutdown function is not needed, the pin can be connected to the V_{IN} pin. Allowing this pin to float causes erratic operation.

Error Flag (FAN2503 Only)

To indicate conditions such as input voltage dropout (low $V_{\rm IN})$, overheating, or overloading (excessive output current); the ERR pin indicates a fault condition. It is an open-drain output that is HIGH when the voltage at V_{OUT} is greater than 95% of the nominal rated output voltage and LOW when V_{OUT} is less than 95% or the rated output voltage, as specified in the error trip level characteristics.

A logic pull-up resistor of 100 k Ω is recommended at this output. The pin can be left disconnected if unused.

Thermal Protection

The FAN2502 / 03 can supply high peak output currents of up to 1 A for brief periods, However, this output load causes the device temperature to increase and exceed maximum ratings due to power dissipation. During output overload conditions, when the die temperature exceeds the shutdown limit temperature of 150°C, onboard thermal protection disables the output until the temperature drops below this limit; at which point, the output is reenabled. During a thermal shutdown situation, the user may assert the power-down function at the Enable pin, reducing power consumption to the minimum level $I_{GND} \cdot V_{\rm IN}$.

Thermal Characteristics

The FAN2502 / 03 can supply 150 mA at the specified output voltage with an operating die (junction) temperature of up to 125°C. Once the power dissipation and thermal resistance is known, the maximum junction temperature of the device can be calculated. While the power dissipation is calculated from known electrical parameters, the thermal resistance is a result of the thermal characteristics of the compact SOT23-5 surfacemount package and the surrounding PC board copper to which it is mounted.

The power dissipation is equal to the product of the input-to-output voltage differential and the output current plus the ground current, multiplied by the input voltage, or:

$$P_{D} = (V_{IN} - V_{OUT})I_{OUT} + V_{IN}I_{GND}$$

The ground pin current, $I_{\mbox{GND},}$ can be found in the charts

provided in the Electrical Characteristics section.

The relationship describing the thermal behavior of the package is:

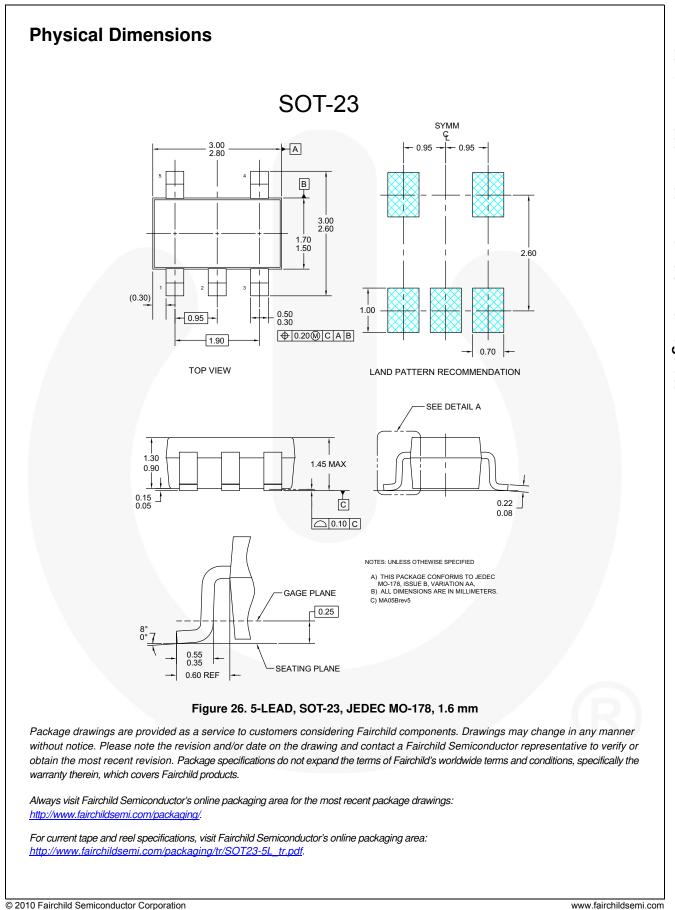
$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_{A}}{\theta_{JA}} \right\}$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die, which is 125°C, and T_A is the ambient operating temperature. θ_{JA} is dependent on the surrounding PC board layout and can be empirically obtained. While the θ_{JC} (junction-to-case) of the SOT23-5 package is specified at 130°C/W, the θ_{JA} of the minimum PCB footprint is at least 235°C/W. This can be improved by providing a heat sink of surrounding copper ground on the PCB. Depending on the size of the copper area, the resulting θ_{JA} can range from approximately 180°C/W for one square inch to nearly 130°C/W for 4 square inches. The addition of backside copper with through-holes, stiffeners, and other enhancements can also reduce this value. The heat contributed by the dissipation of other devices located nearby must be included in design considerations.

Once the limiting parameters in these two relationships have been determined, the design can be modified to ensure that the device remains within specified operating conditions. If overload conditions are not considered, it is possible for the device to enter a thermal cycling loop, in which the circuit enters a shutdown condition, cools, reenables, and then again overheats and shuts down repeatedly due to an unmanaged fault condition.

General PCB Layout Considerations

To achieve the full performance of the device, careful circuit layout and grounding techniques must be observed. Establishing a small local ground, to which the GND pin and the output and bypass capacitors are connected, is recommended. The input capacitor should be grounded to the main ground plane. The guiet local ground is routed back to the main ground plane using feed-through vias. In general, the high-frequency compensation components (input, bypass, and output capacitors) should be located as close to the device as possible. The proximity of the output capacitor is especially important to achieve optimal noise compensation from the onboard error amplifier, especially during high load conditions. A large copper area in the local ground provides the heat sinking discussed above when high power dissipation significantly increases the temperature of the device. Component-side copper provides significantly better thermal performance for this surface-mount device, compared to that obtained when using only copper planes on the underside.



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