Features

- ESD protection for 1 line with uni-directional
- Provide ESD protection for the protected line to
  IEC 61000-4-2 (ESD) ±30kV (air/contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 40A (8/20μs)
  Cable Discharge Event (CDE)
- For low operating voltage applications: **5.5V**
- **0402 small DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Vbat pin for mobile device
- USB type-C CC pin protection
- Data and control lines protection
- Power line protection
- Hand held portable applications

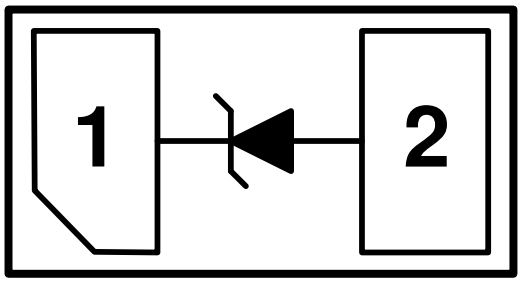
Description

AZ5815-01F is a design which includes a uni-directional surge rated clamping cell to protect one power line, or one control line, or one low-speed data line in an electronic system. The AZ5815-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ5815-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5815-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



DFN1006P2E (Bottom View)

SPECIFICATIONS

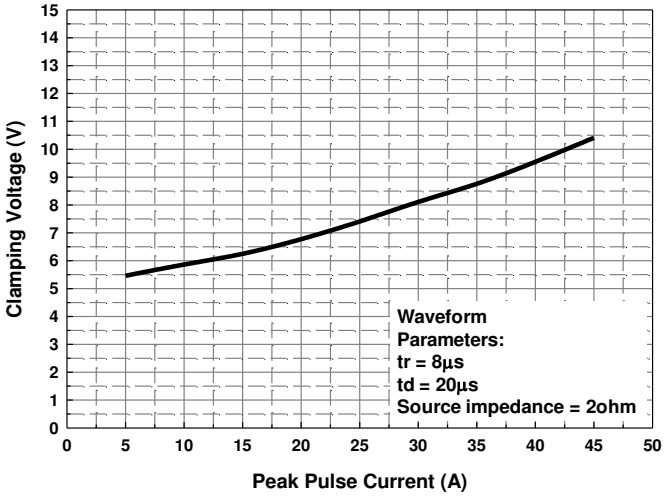
ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp=8/20μs)	I_{PP-1} (Note 1) I_{PP-2} (Note 2)	40 28	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1 to pin-2, T = 25°C.			5.5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T = 25°C, pin-1 to pin-2.			1.0	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T = 25°C, pin-1 to pin-2.	6.2		8.0	V
Forward Voltage	V_F	I_F = 15mA, T = 25°C, pin-2 to pin-1.	0.6		1.2	V
Surge Clamping Voltage (Note 1)	$V_{CL-surge}$	I_{PP} = 5A, T = 25°C, pin-1 to pin-2.		5.5		V
		I_{PP} = 40A, T = 25°C, pin-1 to pin-2.		9.5		
ESD Clamping Voltage (Note 3)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T = 25°C, Contact mode, pin-1 to pin-2.		6.0		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, Contact mode, T = 25 °C, pin-1 to pin-2.		0.04		Ω
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, pin-1 to pin-2, T = 25 °C.		85	100	pF

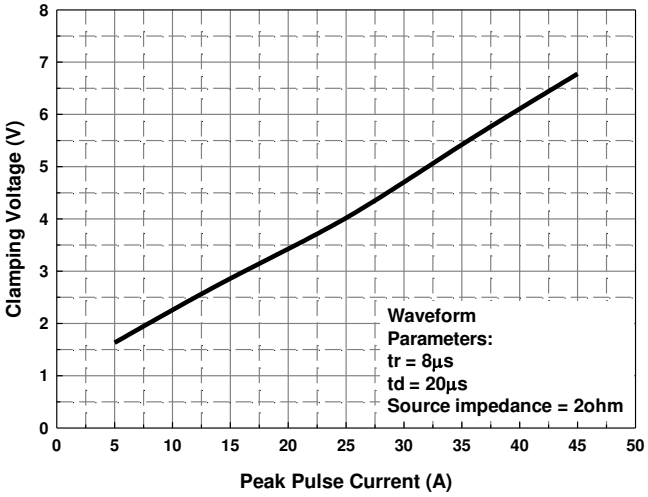
Note 1: The Peak Pulse Current measured conditions: tp = 8/20μs, 2ohm source impedance.
Note 2: The Peak Pulse Current measured conditions: tp = 8/20μs, 42ohm source impedance.
Note 3: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

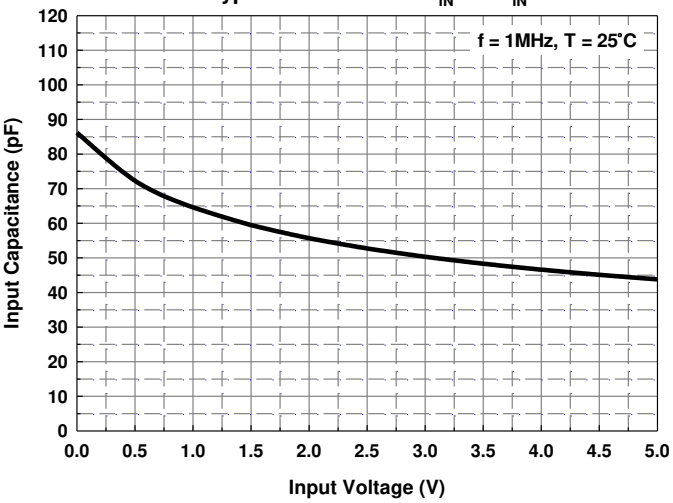
Reverse Clamping Voltage vs. Peak Pulse Current



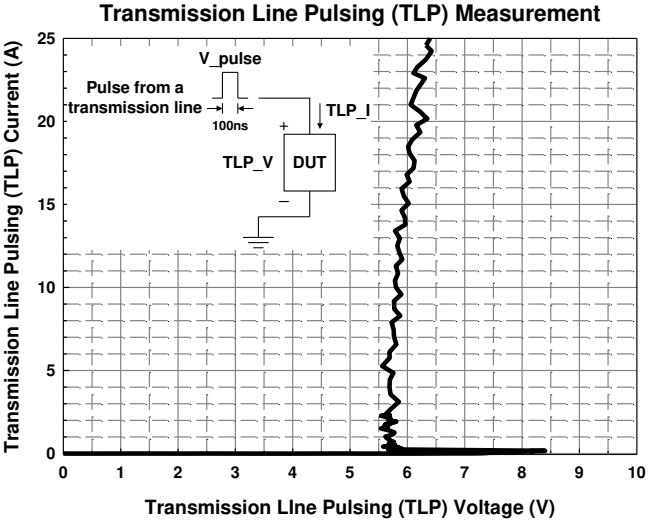
Forward Clamping Voltage vs. Peak Pulse Current



Typical Variation of C_{IN} vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement



Applications Information

The AZ5815-01F is designed to protect one line against system ESD / EFT / Lightning pulses by clamping it to an acceptable reference.

The usage of the AZ5815-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected to pin 1. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ5815-01F should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5815-01F.
- Place the AZ5815-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

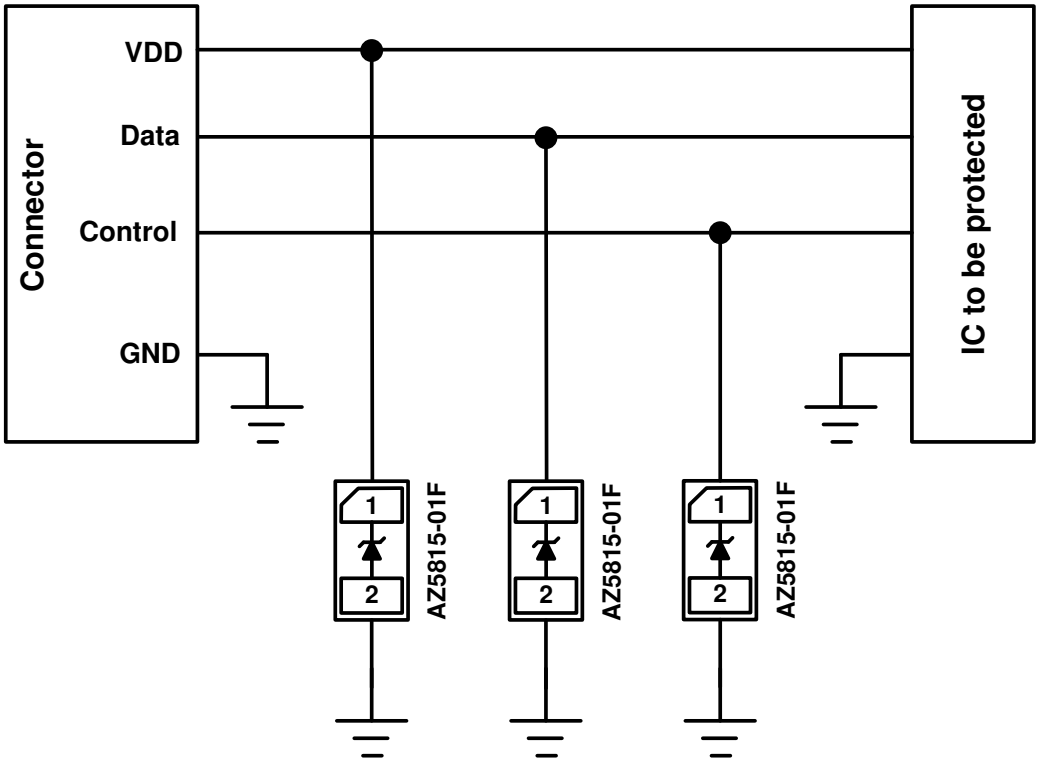
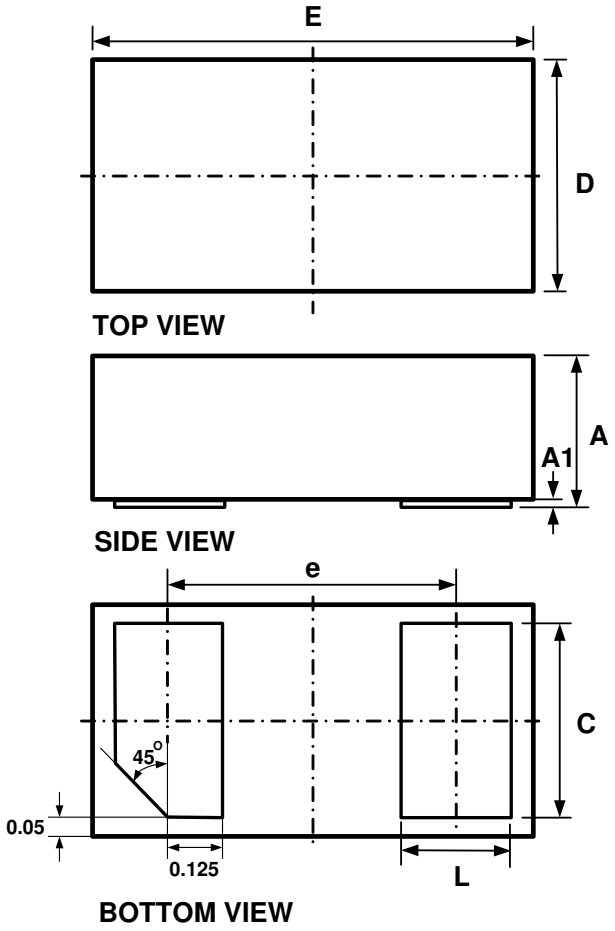


Fig. 1

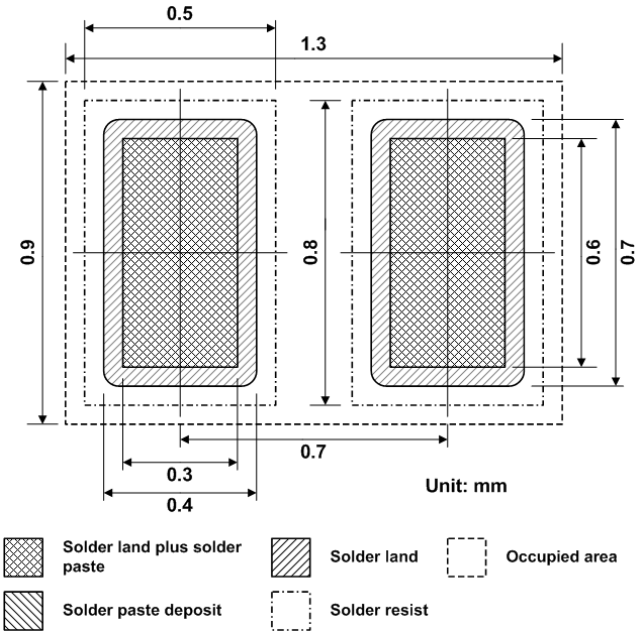
Mechanical Details

DFN1006P2E
PACKAGE DIAGRAMS



Symbol	Millimeters			Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
E	0.95	1.00	1.05	0.037	0.039	0.041
D	0.55	0.60	0.65	0.022	0.024	0.026
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
L	0.20	0.25	0.30	0.008	0.010	0.012
C	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		

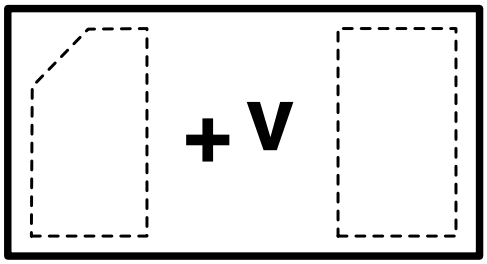
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

v = Device Code

Part Number	Marking Code
AZ5815-01F.R7GR (Green Part)	v

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5815-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels = 48,000/box	6 boxes = 288,000/carton

Revision History

Revision	Modification Description
Revision 2017/08/04	Formal Release.
Revision 2017/08/28	1. Update the maximum Reverse Stand-off Voltage (V_{RWM}) from 5V to 5.5V. 2. Update the minimum Reverse Breakdown Voltage (V_{BV}) from 6.0V to 6.2V.