

MOSFETs Silicon P-Channel MOS (U-MOSVI)

## TJ60S04M3L

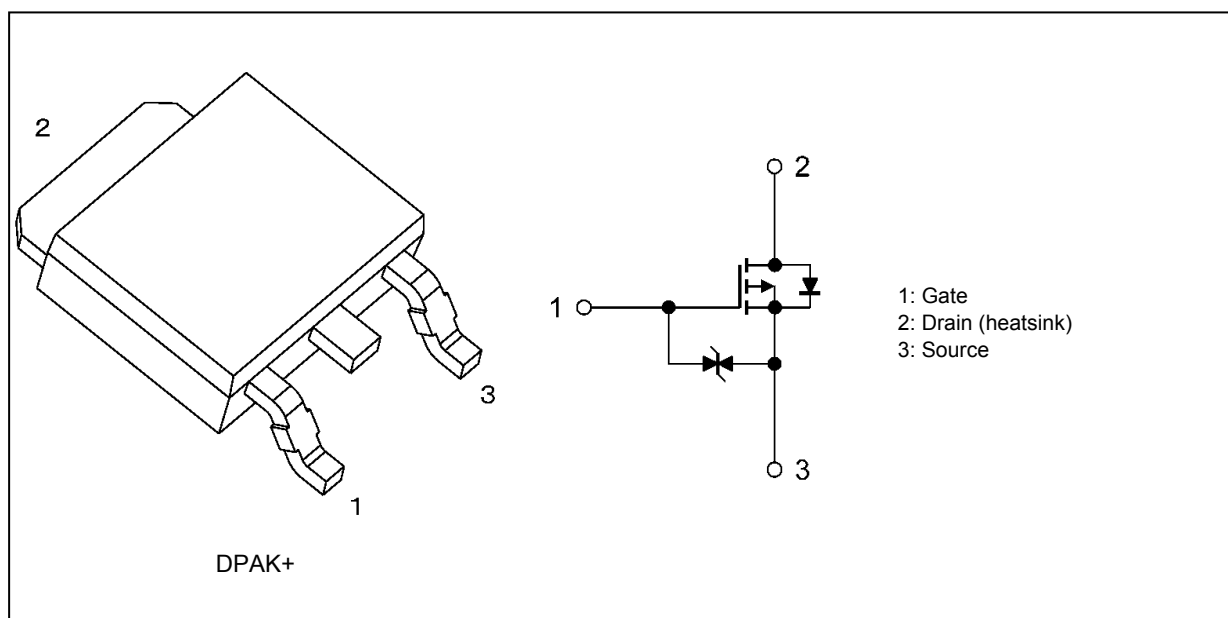
### 1. Applications

- Automotive
- Motor Drivers
- DC-DC Converters
- Switching Voltage Regulators

### 2. Features

- (1) AEC-Q101 qualified
- (2) Low drain-source on-resistance:  $R_{DS(ON)} = 4.8 \text{ m}\Omega$  (typ.) ( $V_{GS} = -10 \text{ V}$ )
- (3) Low leakage current:  $I_{DSS} = -10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = -40 \text{ V}$ )
- (4) Enhancement mode:  $V_{th} = -2.0$  to  $-3.0 \text{ V}$  ( $V_{DS} = -10 \text{ V}$ ,  $I_D = -1 \text{ mA}$ )

### 3. Packaging and Internal Circuit



Start of commercial production

2011-03

## 4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	-40	V
Gate-source voltage	$V_{GSS}$	-20/+10	
Drain current (DC) (Note 1)	$I_D$	-60	A
Drain current (pulsed) (Note 1)	$I_{DP}$	-120	
Power dissipation ( $T_c = 25^\circ\text{C}$ )	$P_D$	90	W
Single-pulse avalanche energy (Note 2)	$E_{AS}$	146	mJ
Avalanche current	$I_{AR}$	-60	A
Channel temperature (Note 3)	$T_{ch}$	175	$^\circ\text{C}$
Storage temperature (Note 3)	$T_{stg}$	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	1.65	$^\circ\text{C}/\text{W}$

Note 1: Ensure that the channel temperature does not exceed  $175^\circ\text{C}$ .

Note 2:  $V_{DD} = -25\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 42\ \mu\text{H}$ ,  $R_G = 25\ \Omega$ ,  $I_{AR} = -60\text{ A}$

Note 3: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

## 6. Electrical Characteristics

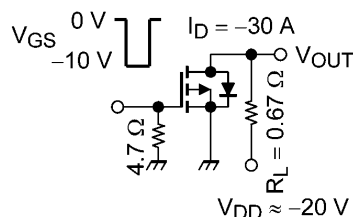
### 6.1. Static Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = -16/+10\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$	—	—	-10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$	-40	—	—	V
Drain-source breakdown voltage (Note 4)	$V_{(BR)DSX}$	$I_D = -10\text{ mA}, V_{GS} = 10\text{ V}$	-30	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-2.0	—	-3.0	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = -6\text{ V}, I_D = -30\text{ A}$	—	6.1	9.4	$\text{m}\Omega$
		$V_{GS} = -10\text{ V}, I_D = -30\text{ A}$	—	4.8	6.3	

Note 4: If a forward bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

### 6.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	6510	—	pF
Reverse transfer capacitance	$C_{rss}$		—	570	—	
Output capacitance	$C_{oss}$		—	780	—	
Switching time (rise time)	$t_r$	See Figure 6.2.1.	—	96	—	ns
Switching time (turn-on time)	$t_{on}$		—	126	—	
Switching time (fall time)	$t_f$		—	240	—	
Switching time (turn-off time)	$t_{off}$		—	730	—	



Duty  $\leq 1\%$ ,  $t_w = 10\ \mu\text{s}$

Fig. 6.2.1 Switching Time Test Circuit

### 6.3. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

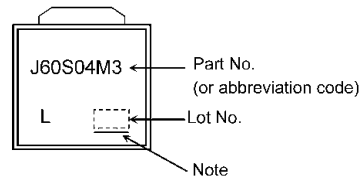
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx -32\text{ V}, V_{GS} = -10\text{ V}, I_D = -60\text{ A}$	—	125	—	nC
Gate-source charge	$Q_{gs}$		—	81	—	
Gate-drain charge	$Q_{gd}$		—	44	—	

### 6.4. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (DC) (Note 5)	$I_{DR}$	—	—	—	-60	A
Reverse drain current (pulsed) (Note 5)	$I_{DRP}$	—	—	—	-120	
Diode forward voltage	$V_{DSF}$	$I_{DR} = -60\text{ A}, V_{GS} = 0\text{ V}$	—	—	1.2	V
Reverse recovery time	$t_{rr}$	$I_{DR} = -60\text{ A}, V_{GS} = 0\text{ V}$ $dI_{DR}/dt = 50\text{ A}/\mu\text{s}$	—	45	—	ns
Reverse recovery charge	$Q_{rr}$		—	27	—	nC

Note 5: Ensure that the channel temperature does not exceed  $175^\circ\text{C}$ .

## 7. Marking (Note)



**Fig. 7.1 Marking**

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

## 8. Characteristics Curves (Note)

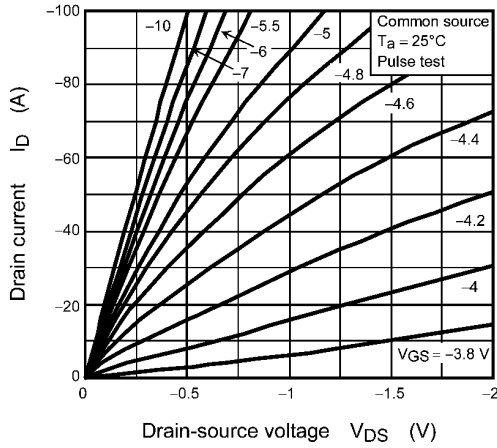


Fig. 8.1  $I_D - V_{DS}$

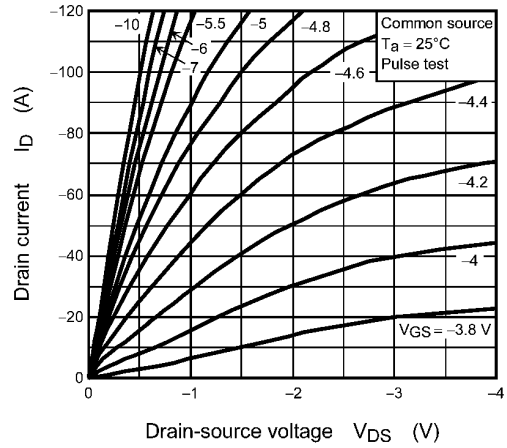


Fig. 8.2  $I_D - V_{DS}$

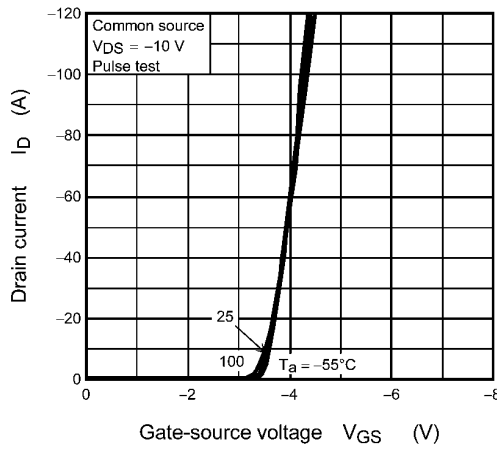


Fig. 8.3  $I_D - V_{GS}$

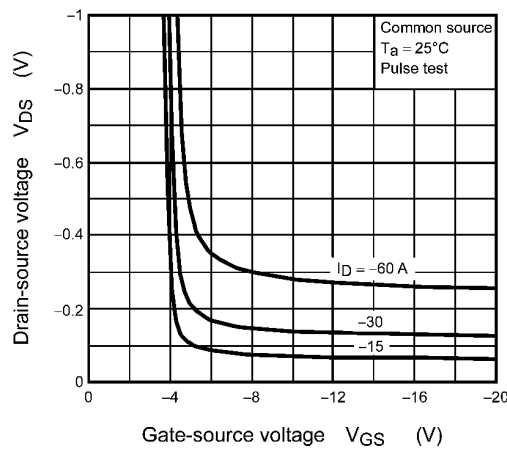


Fig. 8.4  $V_{DS} - V_{GS}$

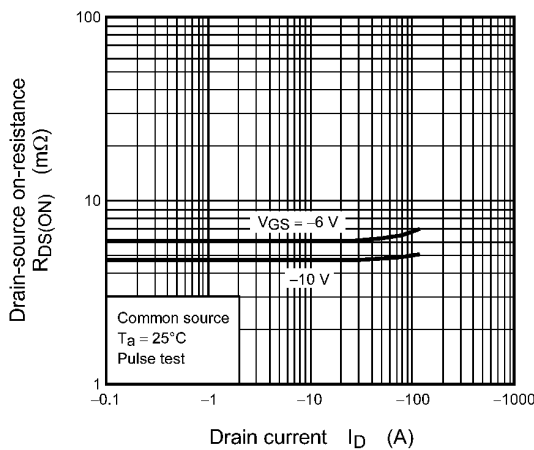


Fig. 8.5  $R_{DS(ON)} - I_D$

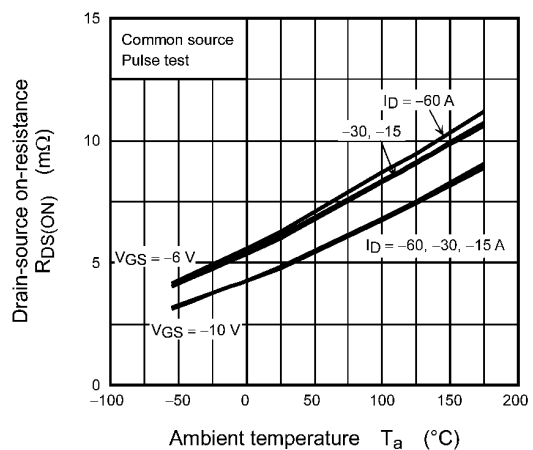
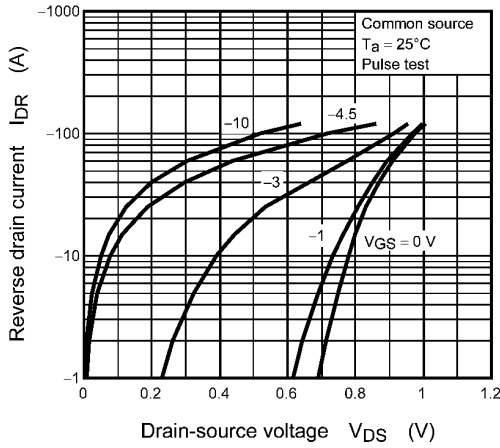
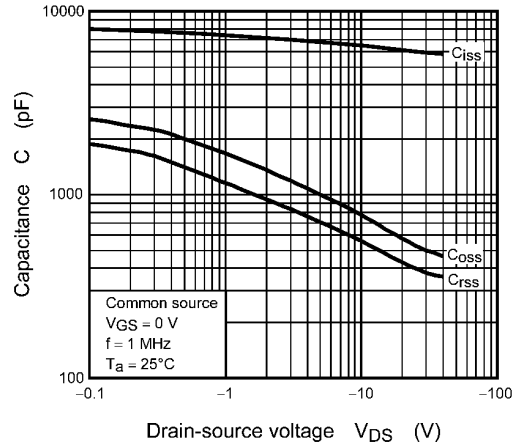


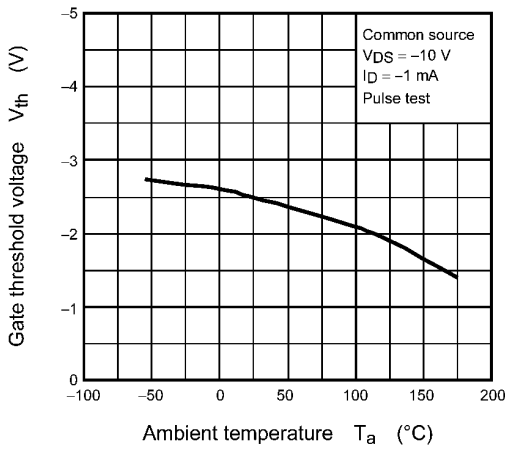
Fig. 8.6  $R_{DS(ON)} - T_a$



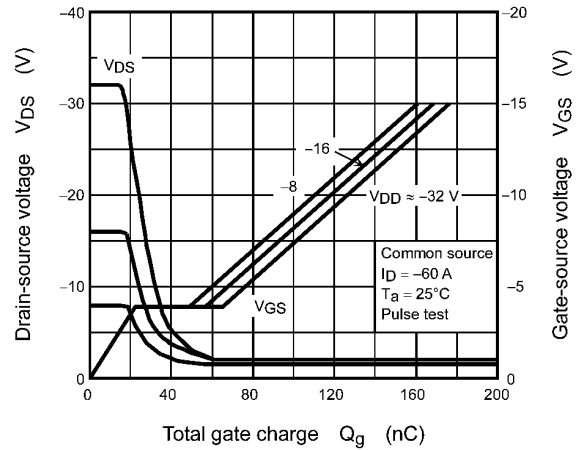
**Fig. 8.7  $I_{DR} - V_{DS}$**



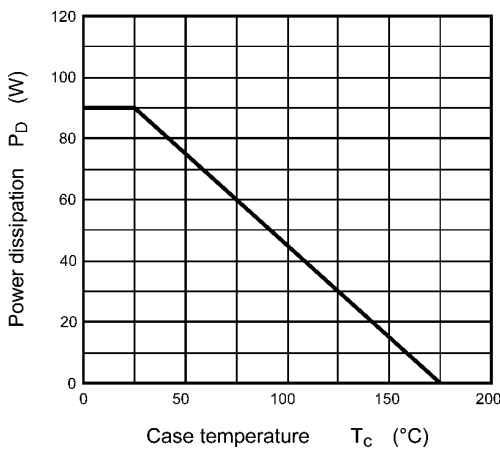
**Fig. 8.8 Capacitance -  $V_{DS}$**



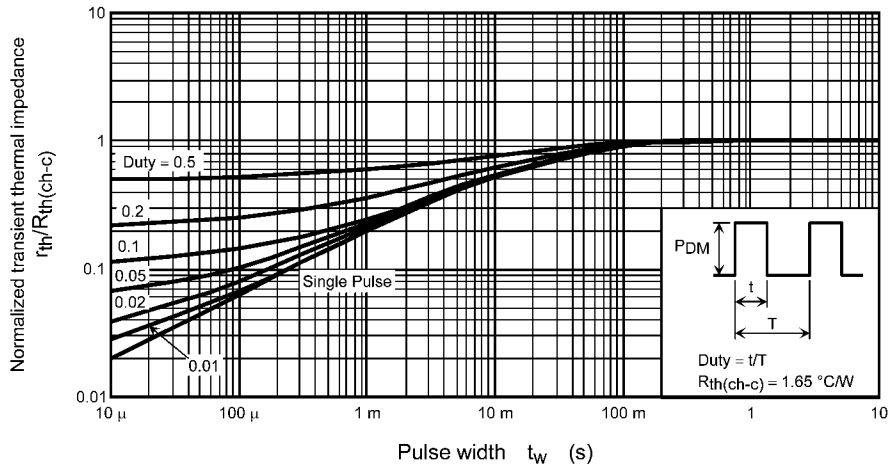
**Fig. 8.9  $V_{th} - T_a$**



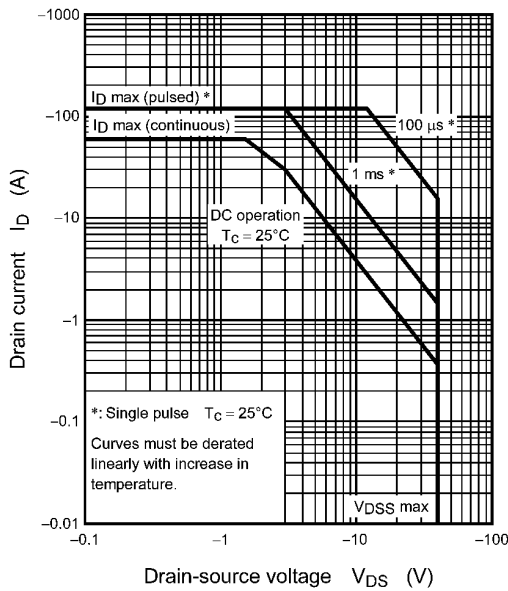
**Fig. 8.10 Dynamic Input/Output Characteristics**



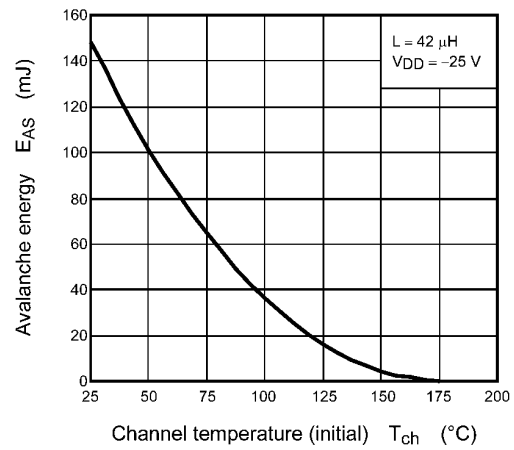
**Fig. 8.11  $P_D - T_c$   
 (Guaranteed Maximum)**



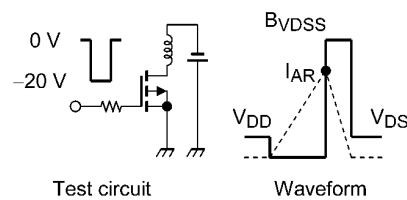
**Fig. 8.12**  $r_{th}/R_{th(ch-c)} - t_w$   
(Guaranteed Maximum)



**Fig. 8.13** Safe Operating Area  
(Guaranteed Maximum)



**Fig. 8.14**  $E_{AS} - T_{ch}$   
(Guaranteed Maximum)



$$R_G = 25 \Omega, V_{DD} = -25 \text{ V}, L = 42 \mu\text{H} \quad E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

**Fig. 8.15** Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.





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