CLOCK SYNTHESIZER FOR PDA

ICS620A-06

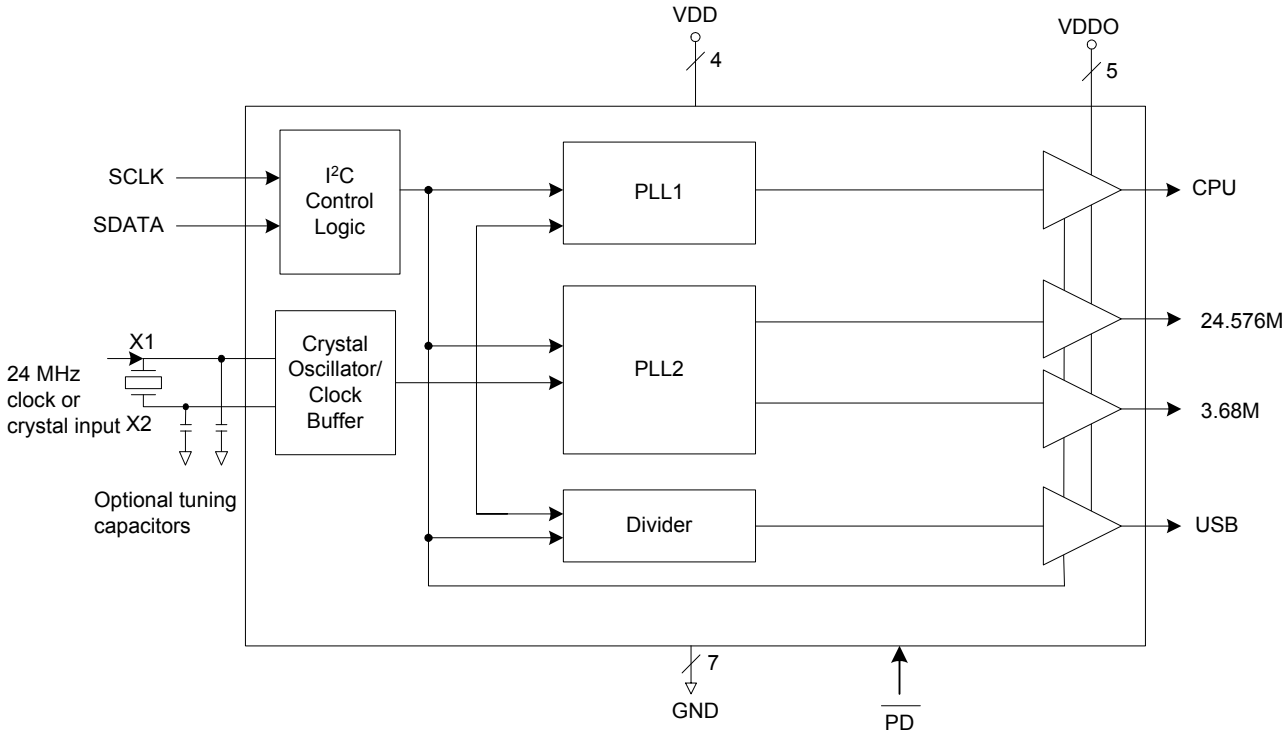
Description

The ICS620A-06 generates four high-quality, high-frequency clock outputs. It is a low-power, low-jitter clock synthesizer developed for PDA (personal digital assistant) applications, to replace multiple crystals and crystal oscillators. This chip offers all of the standard clocks required for a PDA. This chip uses ICS' proprietary mix of analog and digital Phase-Locked Loop (PLL) technology. I^2C bus programming is used to change the CPU and the USB clocks in circuit. In addition, the I^2C serial bus allows the individual clock outputs to be enabled or disabled through software to offer further power savings.

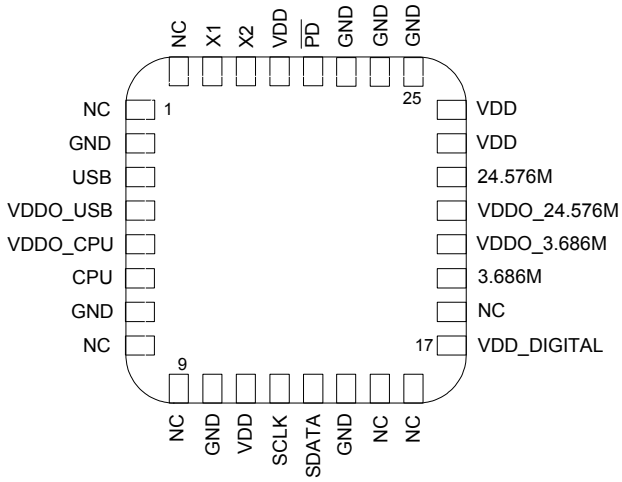
Features

- Extremely low operating current (5 mA)
- Input crystal or clock frequency of 24 MHz
- I^2C programmable processor clock frequency for CPU and USB
- Fixed 24.576 MHz and 3.68 MHz outputs
- Individual clock enable/disable control through I^2C
- Individual PLL and chip power down features
- Operating voltage of 1.8 V core
- Output voltage of either 1.8 V or 2.5 V
- Advanced, low-power CMOS process
- Packaged in 32-pin QFN (RoHS compliant)
- Industrial temperature range available (-40 to +85°C)
- Chip Power-down

Block Diagram



Pin Assignment



32-pin QFN

Table 1

Clock	Available Frequencies (MHz)
CPU	13, 12, 10, 8, 6, 4, 2,1
USB	6, 12, 24,

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	NC	—	No connect. Do not connect this pin to anything.
2	GND	Power	Connect to ground.
3	USB	Output	USB Clock Selection per Table 1 and Table 2 Byte 2.
4	VDDO_USB	Power	Output voltage supply for USB clock, 1.8 V or 2.5 V.
5	VDDO_CPU	Power	Output voltage supply for CPU clock, 1.8 V or 2.5 V.
6	CPU	Output	Processor clock output. Selection per Table 1 and Table 2 Byte 1.
7	GND	Power	Connect to ground.
8	NC	—	No connect. Do not connect this pin to anything.
9	NC	—	No connect. Do not connect this pin to anything.
10	GND	Power	Connect to ground.
11	VDD	Power	Connect to +1.8 V.
12	SCLK	Input	I^2C bus clock pin. Internal pull-up resistor. See note1.
13	SDATA	Input	I^2C bus data pin. Internal pull-up resistor. See note1.
14	GND	Power	Connect to ground.
15	NC	—	No connect. Do not connect this pin to anything.
16	NC	—	No connect. Do not connect this pin to anything.
17	VDD_DIGITAL	Power	Voltage supply for $\overline{PD}$, SCLK, and SDATA pins.
18	NC	—	No connect. Do not connect this pin to anything.
19	3.6864M	Output	3.6864MHz clock output.

Pin Number	Pin Name	Pin Type	Pin Description
20	VDDO_3.686M	Power	Output voltage supply for 3.686 MHz clock – 1.8 V or 2.5 V.
21	VDDO_24.576M	Power	Output voltage supply for 24.576 MHz clock – 1.8 V or 2.5 V.
22	24.576M	Output	24.576 MHz clock for audio.
23	VDD	Power	Connect to +1.8 V.
24	VDD	Power	Connect to +1.8 V.
25	GND	Power	Connect to ground.
26	GND	Power	Connect to ground.
27	GND	Power	Connect to ground.
28	$\overline{PD}$	Input	$\overline{PD}$ =1, chip operates normally. $\overline{PD}$ = 0, chip powers down. Internal pull-up. This pin over rides the PLL power down feature from I2C bus.
29	VDD	Power	Connect to +1.8 V.
30	X2	Output	Connect to 24 MHz crystal. No connect if clock input on pin 20.
31	X1	Input	Crystal connection. Connect to 24 MHz crystal or clock input.
32	NC	—	No connect. Do not connect this pin to anything.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS620A-06 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2] = 20.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if

needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS620A-06. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS620A-06. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 3.6 V
All Inputs	-0.5 V to VDD+0.5 V
All Outputs	-0.5 V to 2.5 V+0.5 V
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD (HBM)	2000 V min.
MSL (Moisture Sensitivity Level)	3

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	°C
Ambient Operating Temperature (industrial)	-40		+85	°C
Output Power Supply Voltage (with respect to GND)	+1.71		+2.625	V
Power Supply Voltage (with respect to GND)	+1.71		+1.89	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 1.8 V ±5%, VDDO = 2.5 V ±5% ,** T_A = 0 to +70°C or -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Output Voltage	VDDO		1.71		2.625	V
Supply Current	IDD	No load, VDD = 1.8 V, VDDO = 1.8 V		4.5		mA
		No load, VDD = 1.8 V, VDDO = 2.5 V		5.5		mA
Standby Current	IDD Standby	No load, $\overline{PD}$ = 0, VDD = 1.8 V, VDDO = 2.5 V		50		µa
Input High Voltage	V_{IH}		0.7VDD			V
Input Low Voltage	V_{IL}				0.3VDD	V
Output High Voltage	V_{OH}	I_{OH} = -2 mA	0.8VDDO			V
Output Low Voltage	V_{OL}	I_{OL} = +2 mA			0.2VDDO	V
Input Capacitance, inputs	C_{IN}			5		pF
Load Capacitance, X1 and X2	C_L	No internal load capacitance		5		pF
Internal Pull-up Resistor	R_{PU}		100	250		kΩ
Internal Pull-down Resistor	R_{PD}		40	250		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDDO = 2.5 V ±5%**, **C_L = 5 pF,** T_A = 0 to +70°C or -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}			24		MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1	0.7	1.5	2.2	ns
Output Fall Time	t_{OF}	80% to 20%, Note 1	0.7	1.5	2.2	ns
Output Impedance	R_O	VO=VDDO/2	33	46	68	Ω
Output Clock Duty Cycle		VDDO/2, Note 1	40	50	60	%
Short Term Jitter		Cycle-to-Cycle		150	250	ps
Long Term Jitter		n=1000			750	ps
Power-up Time	t_{PU}	From minimum VDD to outputs stable		1.5	3	ms
Output Enable Time					10	ns
Output Disable Time					10	ns

Note 1: Measured with a 5 pF load.

AC Electrical Characteristics

Unless stated otherwise, **VDDO = 1.8 V ±0.1 V**,**C_L = 5pF**, T_A = 0 to +70°C or -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}			24		MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1	1.1	2.2	3.3	ns
Output Fall Time	t_{OF}	80% to 20%, Note 1	1.1	2.2	3.3	ns
Output Impedance	R_O	VO=VDDO/2	33	46	68	Ω
Output Clock Duty Cycle		VDDO/2, 27M, Note 1	40	50	60	%
		VDDO/2, Note 1	45	50	55	%
Absolute Clock Period Jitter		Note 1		± 225		ps
Short Term Jitter		Cycle-to-cycle		225	375	ps
Long Term Jitter		n=1000			750	ps
Power-up Time	t_{PU}	From minimum VDD to outputs stable		1.5	3	ms
Output Enable Time					20	ns
Output Disable Time					20	ns

Note 1: Measured with a 5 pF load.

Serial Data Interface

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in the following table.

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'.

The block write and block read protocol is outlined in the table below, followed by the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command code — 8 bit ‘00000000’ stands for block operation	11:18	Command code - 8 bit ‘00000000’ stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte count — 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address — 7 bits
29:36	Data byte 0 — 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 — 8 bits	30:37	Byte count from slave — 8 bits
46	Acknowledge from slave	38	Acknowledge from master
....	.....	39:46	Data byte from slave — 8 bits
....	Data byte (N-1) — 8 bits	47	Acknowledge from master
....	Acknowledge from slave	48:55	Data byte from slave — 8 bits
....	Data byte N — 8 bits	56	Acknowledge from master
....	Acknowledge from slave	....	Data byte N from slave — 8 bits
....	Stop	....	Acknowledge from master
		....	Stop

.

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command code — 8 bit '10000000' stands for byte operation, bits[1:0] of the command code represents the offset of the byte to be accessed	11:18	Command code — 8 bit '10000000' stands for byte operation, bits[1:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master— 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address — 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave — 8 bits
		38	Acknowledge from master
		39	Stop

Table 2

Byte 0: Vendor ID, Revision Code

Bit	@Pup	Name	Description
7	0	Revision Code (MSB)	Revision Code
6	0	Revision Code	Revision Code
5	0	Revision Code	Revision Code
4	1	Revision Code (LSB)	Revision Code
3	0	Vendor ID (MSB)	Vendor ID
2	0	Vendor ID	Vendor ID
1	0	Vendor ID	Vendor ID
0	1	Vendor ID (LSB)	Vendor ID

Byte 1: CPU Clock Control Register

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	1	CPU	Bit 3 =1, CPU = ON, Bit 3 = 0, CPU = OFF,
2	0	CPU	See Table 3 (page 10) for Frequency selection using bits 3, 2 and 1
1	0	CPU	
0	0	CPU	

Byte 2: USB Clock Control Register

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	1	USB Clock	Bit 2 =1, USB = ON, Bit 2 = 0, USB = OFF
1	0	USB Clock	See Table 4 (page 10) for Frequency selection using bits 2 and 1
0	1	USB Clock	

Byte 3: Output Enable and Power down Register

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	1	PLL2	Bit 3 = 1, PLL2 On, Bit3 = 0, PLL2 Off
2	1	PLL1	Bit 2 = 1, PLL1 On, Bit2 = 0, PLL1 Off.
1	1	24.576	Bit 1 =1, 24.576M output enabled Bit 0 = 0, 24.567M output disabled
0	1	3.68M	Bit 0 =1, 3.68M output enabled Bit 0 = 0, 3.68M output disabled

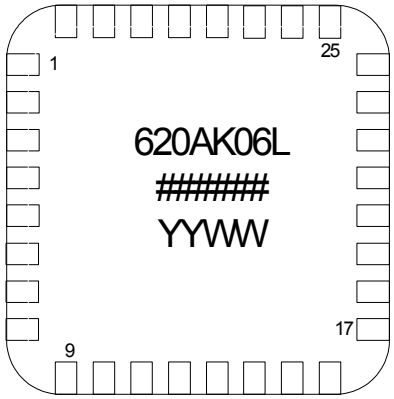
Table 3

Bit 2	Bit 1	Bit 0	CPU Clock (MHz)	
0	0	0	1	Power-up default
0	0	1	2	
0	1	0	4	
0	1	1	6	
1	0	0	8	
1	0	1	10	
1	1	0	12	
1	1	1	13	

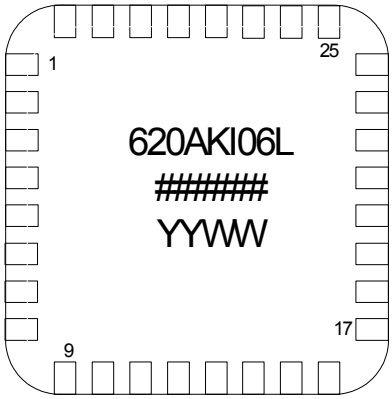
Table 4

Bit 1	Bit 0	USB Clock (MHz)	
0	0	6	
0	1	12	Power-up default
1	0	24	
1	1	Reserved	

Marking Diagram (ICS620AK-06LF)



Marking Diagram (ICS620AKI-06LF)

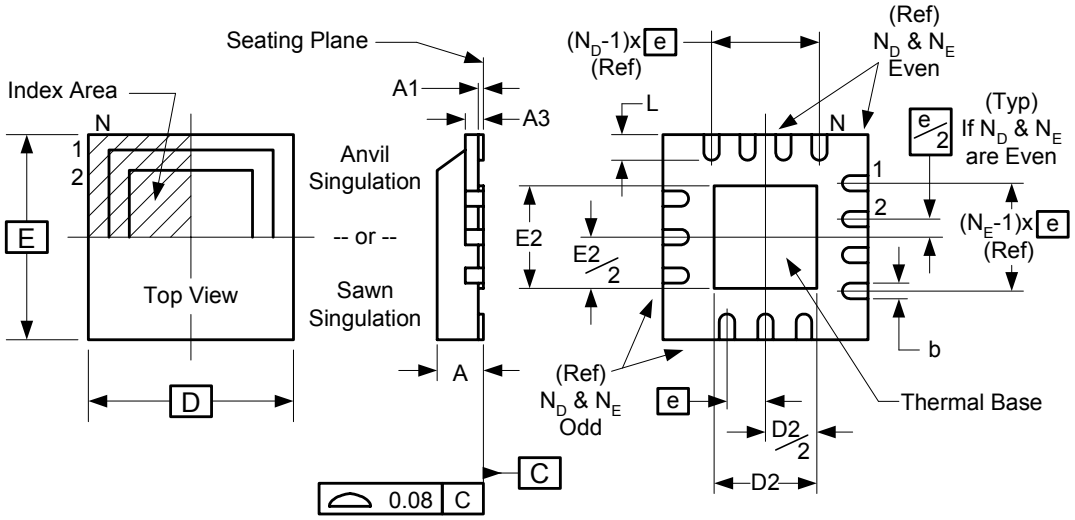


Notes:

1. ###### is the lot code.
2. YYWW is the last two digits of the year and the week number that the part was assembled.
3. “L” denotes RoHS compliant package.
4. “I” denotes industrial temeperature range device
5. Bottom marking: (origin). Origin = country of origin if not USA.

Package Outline and Package Dimensions (32-pin QFN)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	32	
N_D	8	
N_E	8	
D x E BASIC	5.00 x 5.00	
D2	1.25	3.80
E2	1.25	3.80
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS620AK-06LF	see page 10	Tubes	32-pin QFN	0 to +70°C
ICS620AK-06LFT		Tape and Reel	32-pin QFN	0 to +70°C
ICS620AKI-06LF	see page 10	Tubes	32-pin QFN	-40 to +85°C
ICS620AKI-06LFT		Tape and Reel	32-pin QFN	-40 to +85°C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
<product line email>
<product line phone>

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

www.IDT.com