MAX7301

4-Wire-Interfaced, 2.5V to 5.5V, 20-Port and 28-Port I/O Expander

General Description

The MAX7301 compact, serial-interfaced I/O expander (or general-purpose I/O (GPIO) peripheral) provides microprocessors with up to 28 ports. Each port is individually user configurable to either a logic input or logic output.

Each port can be configured either as a push-pull logic output capable of sinking 10mA and sourcing 4.5mA, or a Schmitt logic input with optional internal pullup. Seven ports feature configurable transition detection logic, which generates an interrupt upon change of port logic level. The MAX7301 is controlled through an SPI-compatible 4-wire serial interface.

The MAX7301AAX and MAX7301ATL have 28 ports and are available in 36-pin SSOP and 40-pin TQFN packages, respectively. The MAX7301AAI has 20 ports and is available in a 28-pin SSOP package.

For a 2-wire I^2C-interfaced version, refer to the MAX7300 data sheet.

For a pin-compatible port expander with additional 24mA constant-current LED drive capability, refer to the MAX6957 data sheet.

Applications

- White Goods
- Gaming Machines
- Industrial Controllers
- System Monitoring

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7301AAI+	-40°C to +125°C	28 SSOP
MAX7301AAX+	-40°C to +125°C	36 SSOP
MAX7301ATL+	-40°C to +125°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

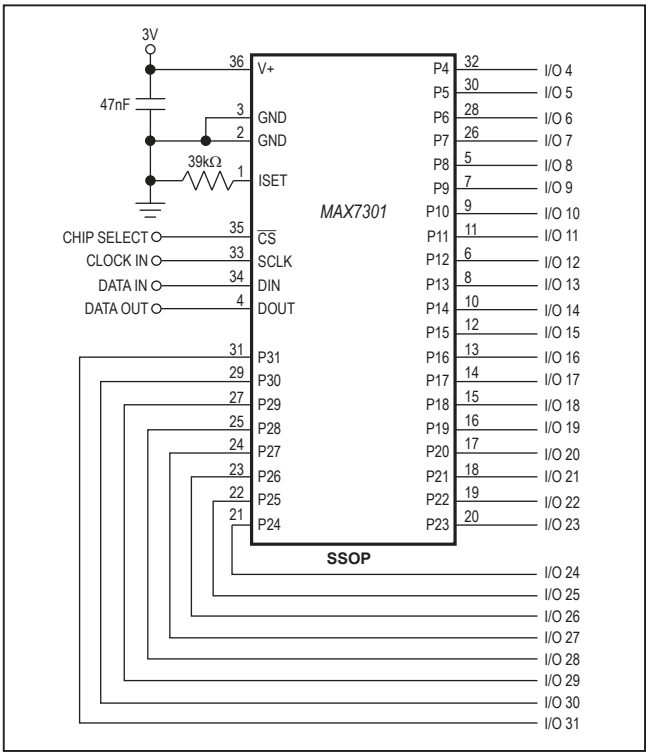
QSPI is a trademark of Motorola, Inc.

MICROWIRE is a registered trademark of National Semiconductor Corp.

Benefits and Features

- Industry-Standard 4-Wire Interface Simplifies Expansion of I/O Ports to Up to 28 I/Os Independent of Microprocessor Architecture
  - High-Speed, 26MHz, SPI-/QSPI™-/MICROWIRE®-Compatible Serial Interface
  - 2.25V to 5.5V Operation
  - 20 or 28 I/O Ports Configurable as Push-Pull Logic Output, Schmitt Logic Input or Schmitt Logic Input with Internal Pullup
  - Logic Transition Detection for Seven I/O Ports
- Low Power Consumption Reduces Power-Supply Requirements
  - 11µA (max) Shutdown Current

Typical Operating Circuit



Pin Configurations appear at end of data sheet.

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Absolute Maximum Ratings

(Voltage with respect to GND.)
V+ .....-0.3V to +6V
All Other Pins .....-0.3V to (V+ + 0.3V)
P4–P31 Current .....±30mA
GND Current 800mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derate 9.5mW/°C above +70°C).....762mW
36-Pin SSOP (derate 11.8mW/°C above +70°C).....941mW
40-Pin TQFN (derate 26.3mW/°C above +70°C)...2963.0mW
Operating Temperature Range
(T_{MIN}, T_{MAX}) ..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(*Typical Operating Circuit*, V+ = 2.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.5		5.5	V
Shutdown Supply Current	ISHDN	All digital inputs at V+ or GND	TA = +25°C		5.5	8	µA
			TA = -40°C to +85°C			10	
			TA = TMIN to TMAX			11	
Operating Supply Current (Output High)	IGPOH	All ports programmed as outputs high, no load, all other inputs at V+ or GND	TA = +25°C		180	230	µA
			TA = -40°C to +85°C			250	
			TA = TMIN to TMAX			270	
Operating Supply Current (Output Low)	IGPOL	All ports programmed as outputs low, no load, all other inputs at V+ or GND	TA = +25°C		170	210	µA
			TA = -40°C to +85°C			230	
			TA = TMIN to TMAX			240	
Operating Supply Current (Input)	IGPI	All ports programmed as inputs without pullup, ports, and all other inputs at V+ or GND	TA = +25°C		110	135	µA
			TA = -40°C to +85°C			140	
			TA = TMIN to TMAX			145	
INPUTS AND OUTPUTS							
Logic High Input Voltage Port Inputs	VIH			0.7 × V+			V
Logic Low Input Voltage Port Inputs	VIL					0.3 × V+	V
Input Leakage Current	IIH, IIL	GPIO inputs without pullup, VPORT = V+ to GND		-100	±1	+100	nA
GPIO Input Internal Pullup to V+	IPU	V+ = 2.5V		12	19	30	µA
		V+ = 5.5V		80	120	180	
Hysteresis Voltage GPIO Inputs	ΔVI				0.3		V
Output High Voltage	VOH	GPIO outputs, ISOURCE = 2mA, TA = -40°C to +85°C		V+ - 0.7			V
		GPIO outputs, ISOURCE = 1mA, TA = TMIN to TMAX (Note 2)		V+ - 0.7			

Electrical Characteristics (continued)

(*Typical Operating Circuit*, V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Sink Current	I_{OL}	V_{PORT} = 0.6V	2	10	18	mA
Output Short-Circuit Current	I_{OLSC}	Port configured output low, shorted to V+	2.75	11	20.00	mA
Input High-Voltage SCLK, DIN, $\overline{CS}$	V_{IH}	V+ ≤ 3.3V	1.6			V
		V+ > 3.3V	2			
Input Low-Voltage SCLK, DIN, $\overline{CS}$	V_{IL}				0.6	V
Input Leakage Current SCLK, DIN, $\overline{CS}$	I_{IH}, I_{IL}		-50		+50	nA
Output High-Voltage DOUT	V_{OH}	I_{SOURCE} = 1.6mA	V+ - 0.5			V
Output Low-Voltage DOUT	V_{OL}	I_{SINK} = 1.6mA			0.4	V

Timing Characteristics (Figure 3)

(V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

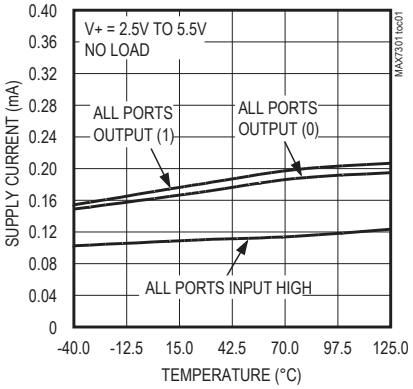
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Clock Period	t_{CP}		38.4			ns
CLK Pulse-Width High	t_{CH}		19			ns
CLK Pulse-Width Low	t_{CL}		19			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		9.5			ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		9.5			ns
DIN Hold Time	t_{DH}		0			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD} = 25pF			21	ns
Minimum $\overline{CS}$ Pulse High	t_{CSW}		19			ns

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.

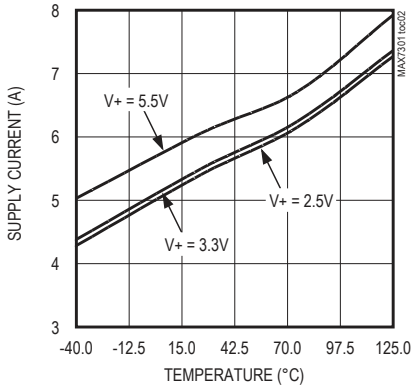
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

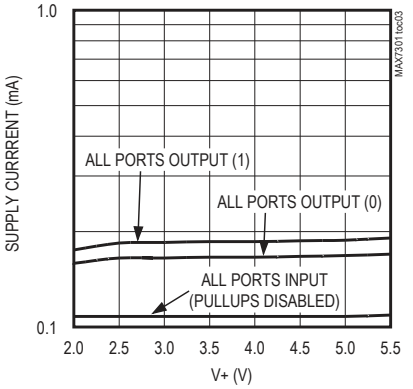
OPERATING SUPPLY CURRENT vs. TEMPERATURE



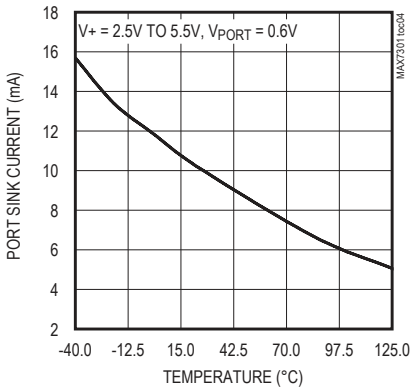
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



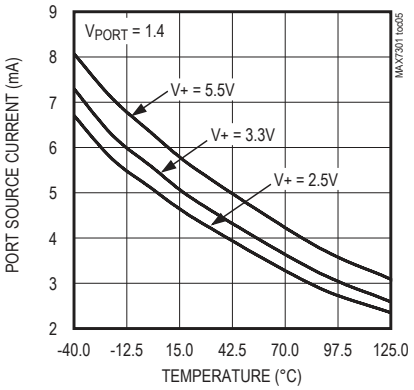
OPERATING SUPPLY CURRENT vs. V+ (OUTPUTS UNLOADED)



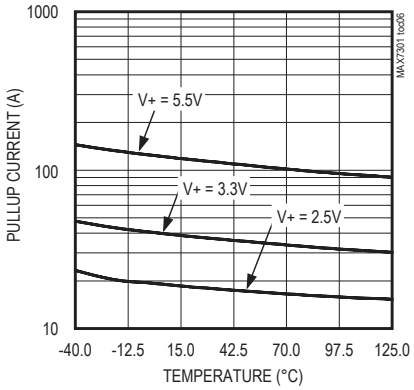
GPO SINK CURRENT vs. TEMPERATURE (OUTPUT = 0)



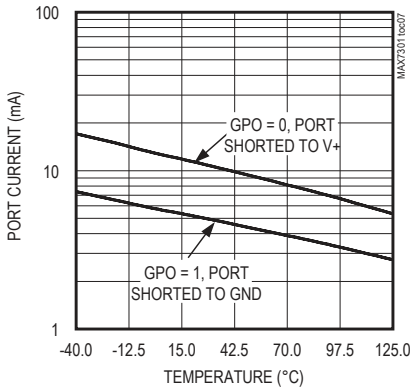
GPO SOURCE CURRENT vs. TEMPERATURE (OUTPUT = 1)



GPI PULLUP CURRENT vs. TEMPERATURE



GPO SHORT-CIRCUIT CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
36 SSOP	28 SSOP	TQFN		
1	1	36	ISET	Bias Current Setting. Connect ISET to GND through a resistor (RISET) value of 39kΩ to 120kΩ.
2, 3	2, 3	37, 38, 39	GND	Ground
4	4	40	DOUT	4-Wire Interface Serial Data Output Port
—	5–24	—	P12–P31	I/O Ports. P12 to P31 can be configured as push-pull outputs, CMOS logic inputs, or CMOS logic inputs with weak pullup resistor.
5–32	—	1–10, 12–19, 21–30	P4–P31	I/O Ports. P4 to P31 can be configured as push-pull outputs, CMOS logic inputs, or CMOS logic inputs with weak pullup resistor.
—	—	11, 20, 31	N.C.	No Connection. Not internally connected.
33	25	32	SCLK	4-Wire Interface Serial Clock Input Port
34	26	33	DIN	4-Wire Interface Serial Data Input Port
35	27	34	$\overline{CS}$	4-Wire Interface Chip-Select Input, Active-Low
36	28	35	V+	Positive Supply Voltage. Bypass V+ to GND with a minimum 0.047µF capacitor.
—	—	—	EP	Exposed Pad on Package Underside. Connect to GND.

Detailed Description

The MAX7301 GPIO peripheral provides up to 28 I/O ports, P4 to P31, controlled through an SPI-compatible serial interface. The ports can be configured to any combination of logic inputs and logic outputs, and default to logic inputs on power-up.

Figure 1 is the MAX7301 functional diagram. Any I/O port can be configured as a push-pull output (sinking 10mA, sourcing 4.5mA), or a Schmitt-trigger logic input. Each input has an individually selectable internal pullup resistor. Additionally, transition detection allows seven ports (P24 through P30) to be monitored in any maskable combination for changes in their logic status. A detected transition is flagged through an interrupt pin (port P31).

The port configuration registers set the 28 ports, P4 to P31, individually as GPIO. A pair of bits in registers 0x09 through 0x0F sets each port's configuration (Tables 1 and 2).

The 36-pin MAX7301AAX and 40-pin MAX7301ATL have 28 ports, P4 to P31. The 28-pin MAX7301AAI is offered in 20 ports, P12 to P31. The eight unused ports should be configured as outputs on power-up by writing 0x55 to registers 0x09 and 0x0A. If this is not done, the eight unused ports remain as floating inputs and quiescent supply current rises, although there is no damage to the part.

Register Control of I/O Ports Across Multiple Drivers

The MAX7301 offers 20 or 28 I/O ports, depending on package choice.

Two addressing methods are available. Any single port (bit) can be written (set/cleared) at once; or, any sequence of eight ports can be written (set/cleared) in any combination at once. There are no boundaries; it is equally acceptable to write P0 through P7, P1 through P8, or P31 through P38 (P32 through P38 are nonexistent, so the instructions to these bits are ignored).

Shutdown

When the MAX7301 is in shutdown mode, all ports are forced to inputs, and the pullup current sources are turned off. Data in the port and control registers remain unaltered so port configuration and output levels are restored when the MAX7301 is taken out of shutdown. The display driver can still be programmed while in shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at GND or V+ potential. Shutdown mode is exited by setting the S bit in the configuration register (Table 6).

Table 1. Port Configuration Map

REGISTER	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Port Configuration for P7, P6, P5, P4	0x09	P7		P6		P5		P4	
Port Configuration for P11, P10, P9, P8	0x0A	P11		P10		P9		P8	
Port Configuration for P15, P14, P13, P12	0x0B	P15		P14		P13		P12	
Port Configuration for P19, P18, P17, P16	0x0C	P19		P18		P17		P16	
Port Configuration for P23, P22, P21, P20	0x0D	P23		P22		P21		P20	
Port Configuration for P27, P26, P25, P24	0x0E	P27		P26		P25		P24	
Port Configuration for P31, P30, P29, P28	0x0F	P31		P30		P29		P28	

Table 2. Port Configuration Matrix

MODE	FUNCTION	PORT REGISTER (0x20–0x5F) (0xA0–0xDF)	PIN BEHAVIOR	ADDRESS CODE (HEX)	PORT CONFIGURATION BIT PAIR	
					UPPER	LOWER
DO NOT USE THIS SETTING				0x09 to 0x0F	0	0
Output	GPIO Output	Register bit = 0	Active-low logic output	0x09 to 0x0F	0	1
		Register bit = 1	Active-high logic output			
Input	GPIO Input Without Pullup	Register bit = input logic level	Schmitt logic input	0x09 to 0x0F	1	0
Input	GPIO Input with Pullup		Schmitt logic input with pullup	0x09 to 0x0F	1	1

Serial Interface

The MAX7301 communicates through an SPI-compatible 4-wire serial interface. The interface has three inputs, Clock (SCLK), Chip Select ($\overline{CS}$), and Data In (DIN), and one output, Data Out (DOUT). $\overline{CS}$ must be low to clock data into or out of the device, and DIN must be stable when sampled on the rising edge of SCLK. DOUT provides a copy of the bit that was input 15.5 clocks earlier, or upon a query it outputs internal register data, and is stable on the rising edge of SCLK. **Note that the SPI protocol expects DOUT to be high impedance when the MAX7301 is not being accessed; DOUT on the MAX7301 is never high impedance. Refer to Application Note 1879: *Using Maxim SPI-compatible Display Drivers with other SPI Peripherals* for ways to convert DOUT to tri-state, if required.**

SCLK and DIN may be used to transmit data to other peripherals, so the MAX7301 ignores all activity on SCLK and DIN except between the fall and subsequent rise of $\overline{CS}$.

Control and Operation Using the 4-Wire Interface

Controlling the MAX7301 requires sending a 16-bit word. The first byte, D15 through D8, is the command address (Table 3), and the second byte, D7 through D0, is the data byte (Table 4 through Table 8).

Connecting Multiple MAX7301s to the 4-Wire Bus

Multiple MAX7301s may be daisy-chained by connecting the DOUT of one device to the DIN of the next, and driving SCLK and $\overline{CS}$ lines in parallel (Figure 3). Data at DIN propagates through the internal shift registers and appears at DOUT 15.5 clock cycles later, clocked out on the falling edge of SCLK. When sending commands to multiple MAX7301s, all devices are accessed at the same time. An access requires (16 × n) clock cycles, where n is the number of MAX7301s connected together. To update just one device in a daisy-chain, the user can send the No-Op command (0x00) to the others.

Writing Device Registers

The MAX7301 contains a 16-bit shift register into which DIN data are clocked on the rising edge of SCLK, when $\overline{CS}$ is low. When $\overline{CS}$ is high, transitions on SCLK have no effect. When $\overline{CS}$ goes high, the 16 bits in the Shift register are parallel loaded into a 16-bit latch. The 16 bits in the latch are then decoded and executed.

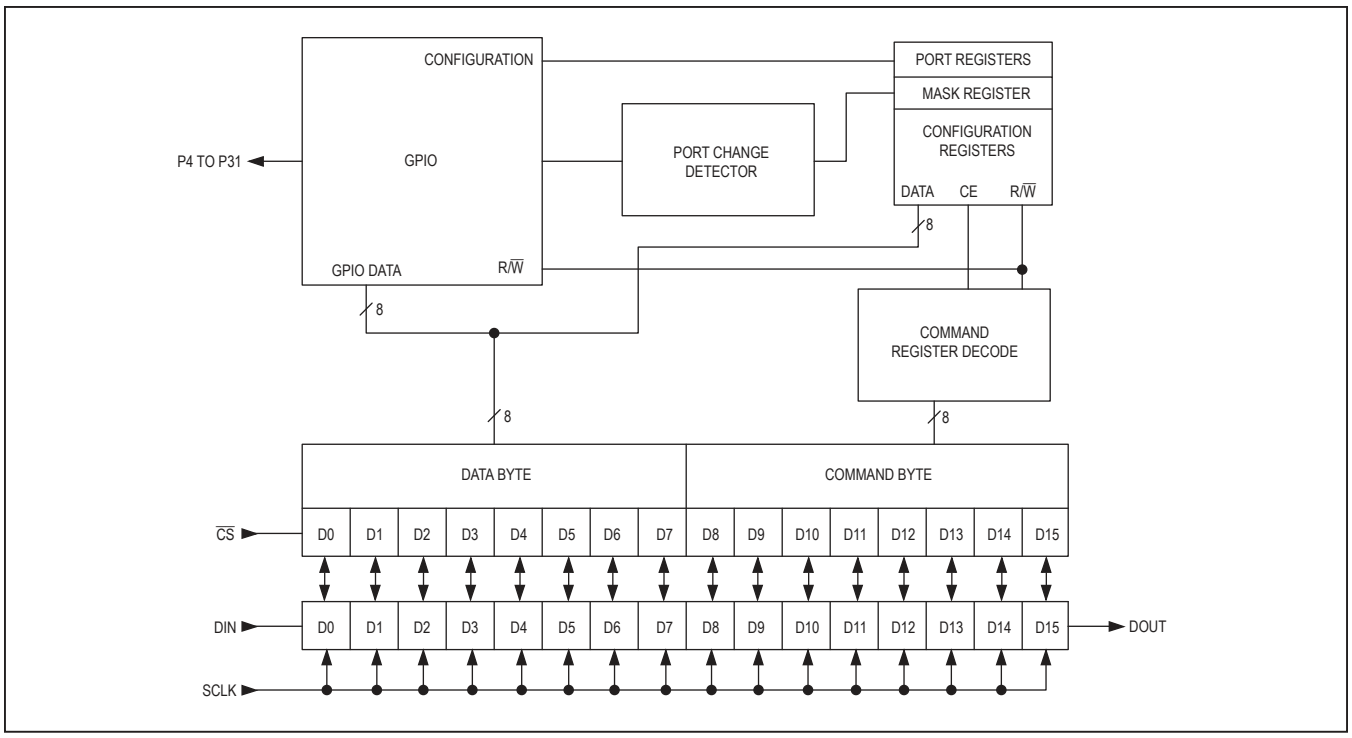


Figure 1. MAX7301 Functional Diagram

The MAX7301 is written to using the following sequence:

1) Take SCLK low.
2) Take $\overline{CS}$ low. This enables the internal 16-bit shift register.
3) Clock 16 bits of data into DIN—D15 first, D0 last—observing the setup and hold times (bit D15 is low, indicating a write command).
4) Take $\overline{CS}$ high (either while SCLK is still high after clocking in the last data bit, or after taking SCLK low).
5) Take SCLK low (if not already low).

Figure 4 shows a write operation when 16 bits are transmitted.

It is acceptable to clock more than 16 bits into the MAX7301 between taking $\overline{CS}$ low and taking $\overline{CS}$ high again. In this case, only the last 16 bits clocked into the MAX7301 are retained.

Reading Device Registers

Any register data within the MAX7301 may be read by sending a logic high to bit D15. The sequence is:

1) Take SCLK low.
2) Take $\overline{CS}$ low (this enables the internal 16-bit Shift register).
3) Clock 16 bits of data into DIN—D15 first to D0 last. D15 is high, indicating a read command and bits D14 through D8 containing the address of the register to be read. Bits D7–D0 contain dummy data, which is discarded.
4) Take $\overline{CS}$ high (either while SCLK is still high after clocking in the last data bit, or after taking SCLK low), positions D7 through D0 in the Shift register are now loaded with the register data addressed by bits D14 through D8.
5) Take SCLK low (if not already low).
6) Issue another read or write command (which can be a No-Op), and examine the bit stream at DOUT; the second 8 bits are the contents of the register addressed by bits D14 through D8 in step 3.

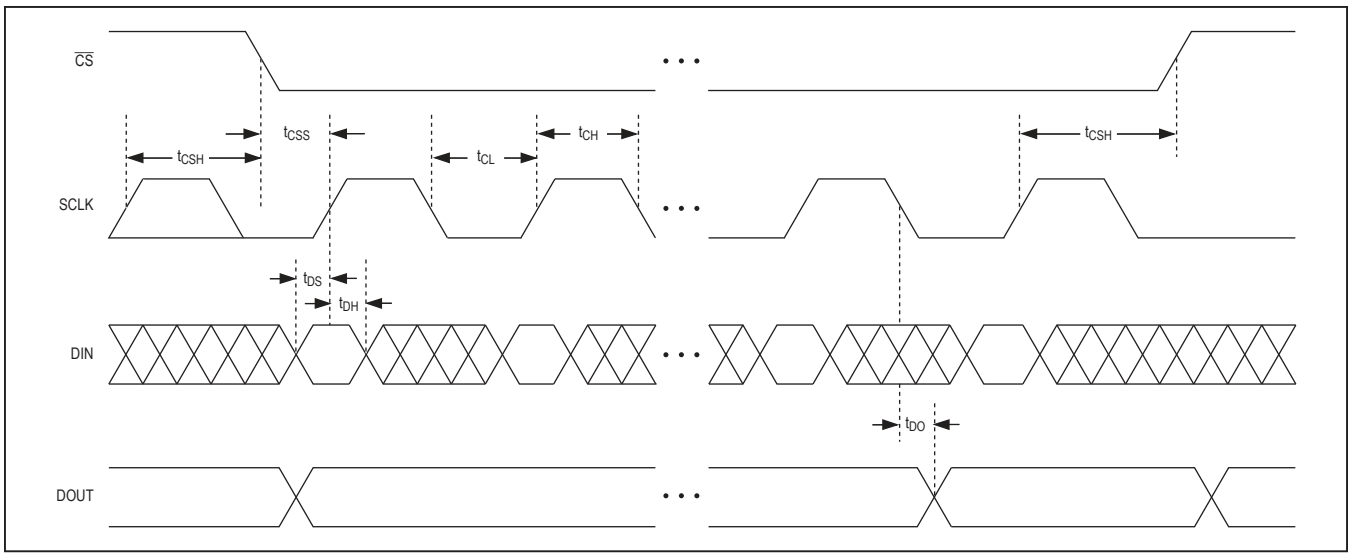


Figure 2. 4-Wire Interface

Initial Power-Up

On initial power-up, all control registers are reset, and the MAX7301 enters shutdown mode (Table 4).

Transition (Port Data Change) Detection

Port transition detection allows any combination of the seven ports P24–P30 to be continuously monitored for changes in their logic status (Figure 5). A detected change is flagged on port P31, which is used as an active-high interrupt output (INT). Note that the MAX7301 does not identify which specific port(s) caused the interrupt, but provides an alert that one or more port levels have changed.

The mask register contains 7 mask bits that select which of the seven ports, P24–P30 are to be monitored (Table 8). Set the appropriate mask bit to enable that port for transition detect. Clear the mask bit if transitions on that port are to be ignored. Transition detection works regardless of whether the port being monitored is set to input or output, but generally it is not particularly useful to enable transition detection for outputs.

Port P31 must be configured as an output in order to work as the interrupt output INT when transition detection is used. Port P31 is set as output by writing bit D7 = 0 and bit D6 = 1 to the port configuration register (Table 1).

To use transition detection, first set up the mask register and configure port P31 as an output, as described above. Then enable transition detection by setting the M bit in the configuration register (Table 7). Whenever the configuration register is written with the M bit set, the MAX7301 updates an internal 7-bit snapshot register, which holds the comparison copy of the logic states of ports P24 through P30. The update action occurs regardless of the previous state of the M bit, so that it is not necessary to clear the M bit and then set it again to update the snapshot register.

When the configuration register is written with the M bit set, transition detection is enabled and remains enabled until either the configuration register is written with the M bit clear, or a transition is detected. The INT output port P31 goes low, if it was not already low.

Once transition detection is enabled, the MAX7301 continuously compares the snapshot register against the changing states of P24 through P31. If a change on any of the monitored ports is detected, even for a short time (like a pulse), INT output port P31 is latched high. The INT output is not cleared if more changes occur or if the data pattern returns to its original snapshot condition. The only way to clear INT is to access (read or write) the transition detection mask register (Table 8).

Transition detection is a one-shot event. When INT has been cleared after responding to a transition event, transition detection is automatically disabled, even though the M bit in the configuration register remains set (unless cleared by the user). Reenable transition detection by writing the configuration register with the M bit set, to take a new snapshot of the seven ports P24 to P30.

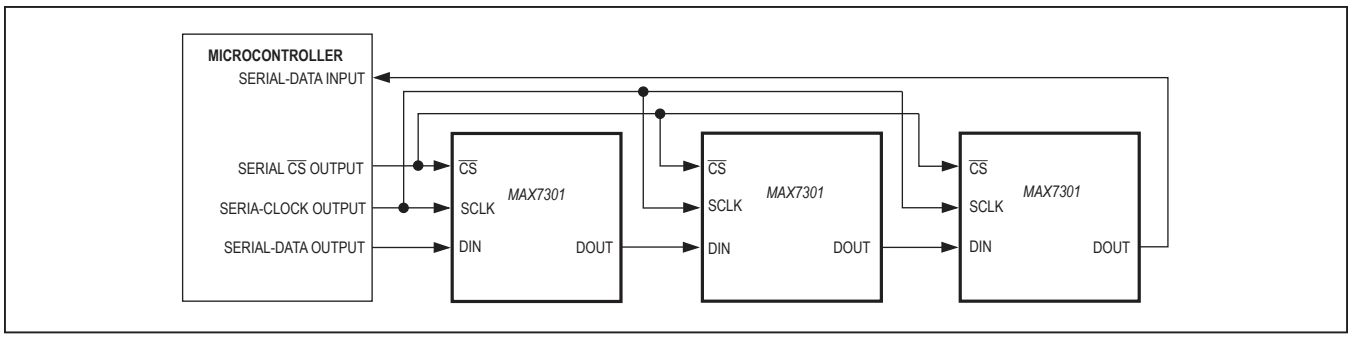


Figure 3. Daisy-Chain Arrangement for Controlling Multiple MAX7301s

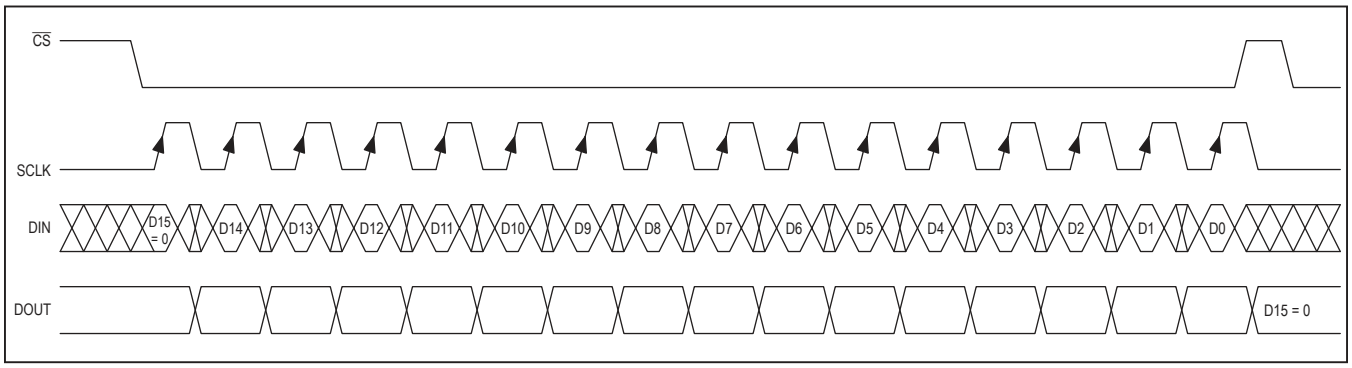


Figure 4. Transmission of a 16-Bit Write to the MAX7301

External Component R_{ISET}

The MAX7301 uses an external resistor, R_{ISET}, to set internal biasing. Use a resistor value of 39kΩ.

Applications Information

Low-Voltage Operation

The MAX7301 operates down to 2V supply voltage (although the sourcing and sinking currents are not guaranteed), providing that the MAX7301 is powered up initially to at least 2.5V to trigger the device's internal reset, and also that the serial interface is constrained to 10Mbps.

SPI Routing Considerations

The MAX7301's SPI interface is guaranteed to operate at 26Mbps on a 2.5V supply, and on a 5V supply typically operates at 50Mbps. This means that transmission line issues should be considered when the interface connections are longer than 100mm, particularly with higher supply voltages. Ringing manifests itself as communication issues, often intermittent, typically due to double clocking due to ringing at the SCLK input. Fit a 1kΩ to 10kΩ parallel termination resistor to either GND or V+ at the DIN, SCLK, and $\overline{CS}$ input to damp ringing for moderately long interface runs. Use line-impedance matching terminations when making connections between boards.

PCB Layout Considerations

For the TQFN version, connect the underside exposed pad to GND. Ensure that all the MAX7301 GND connections are used. A ground plane is not necessary, but may be useful to reduce supply impedance if the MAX7301 outputs are to be heavily loaded. Keep the track length from the ISET pin to the R_{ISET} resistor as short as possible, and take the GND end of the resistor either to the ground plane or directly to the ground pins.

Power-Supply Considerations

The MAX7301 operates with power-supply voltages of 2.5V to 5.5V. Bypass the power supply to GND with a 0.047µF capacitor as close to the device as possible. Add a 1µF capacitor if the MAX7301 is far away from the board's input bulk decoupling capacitor.

Chip Information

PROCESS: CMOS

Table 3. Register Address Map

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
No-Op	R/$\overline{W}$	0	0	0	0	0	0	0	0x00
Configuration	R/$\overline{W}$	0	0	0	0	1	0	0	0x04
Transition Detect Mask	R/$\overline{W}$	0	0	0	0	1	1	0	0x06
Factory Reserved. Do not write to this.	R/$\overline{W}$	0	0	0	0	1	1	1	0x07
Port Configuration P7, P6, P5, P4	R/$\overline{W}$	0	0	0	1	0	0	1	0x09
Port Configuration P11, P10, P9, P8	R/$\overline{W}$	0	0	0	1	0	1	0	0x0A
Port Configuration P15, P14, P13, P12	R/$\overline{W}$	0	0	0	1	0	1	1	0x0B
Port Configuration P19, P18, P17, P16	R/$\overline{W}$	0	0	0	1	1	0	0	0x0C
Port Configuration P23, P22, P21, P20	R/$\overline{W}$	0	0	0	1	1	0	1	0x0D
Port Configuration P27, P26, P25, P24	R/$\overline{W}$	0	0	0	1	1	1	0	0x0E
Port Configuration P31, P30, P29, P28	R/$\overline{W}$	0	0	0	1	1	1	1	0x0F
Port 0 only (virtual port, no action)	R/$\overline{W}$	0	1	0	0	0	0	0	0x20
Port 1 only (virtual port, no action)	R/$\overline{W}$	0	1	0	0	0	0	1	0x21
Port 2 only (virtual port, no action)	R/$\overline{W}$	0	1	0	0	0	1	0	0x22
Port 3 only (virtual port, no action)	R/$\overline{W}$	0	1	0	0	0	1	1	0x23
Port 4 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	0	1	0	0	0x24
Port 5 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	0	1	0	1	0x25
Port 6 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	0	1	1	0	0x26
Port 7 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	0	1	1	1	0x27
Port 8 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	1	0	0	0	0x28
Port 9 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	1	0	0	1	0x29
Port 10 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	1	0	1	0	0x2A
Port 11 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	1	0	1	1	0x2B
Port 12 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	1	1	0	0	0x2C
Port 13 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	1	1	0	1	0x2D
Port 14 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	1	1	1	0	0x2E
Port 15 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	0	1	1	1	1	0x2F
Port 16 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	0	0	0	0	0x30
Port 17 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	0	0	0	1	0x31
Port 18 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	0	0	1	0	0x32
Port 19 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	0	0	1	1	0x33
Port 20 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	0	1	0	0	0x34
Port 21 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	0	1	0	1	0x35
Port 22 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	0	1	1	0	0x36
Port 23 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	0	1	1	1	0x37
Port 24 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	1	0	0	0	0x38
Port 25 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	1	0	0	1	0x39

Table 3. Register Address Map (continued)

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
Port 26 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	1	0	1	0	0x3A
Port 27 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	1	0	1	1	0x3B
Port 28 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	1	1	0	0	0x3C
Port 29 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	1	1	0	1	0x3D
Port 30 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	1	1	1	0	0x3E
Port 31 only (data bit D0. D7–D1 read as 0)	R/$\overline{W}$	0	1	1	1	1	1	1	0x3F
4 ports 4–7 (data bits D0–D3. D4–D7 read as 0)	R/$\overline{W}$	1	0	0	0	0	0	0	0x40
5 ports 4–8 (data bits D0–D4. D5–D7 read as 0)	R/$\overline{W}$	1	0	0	0	0	0	1	0x41
6 ports 4–9 (data bits D0–D5. D6–D7 read as 0)	R/$\overline{W}$	1	0	0	0	0	1	0	0x42
7 ports 4–10 (data bits D0–D6. D7 reads as 0)	R/$\overline{W}$	1	0	0	0	0	1	1	0x43
8 ports 4–11 (data bits D0–D7)	R/$\overline{W}$	1	0	0	0	1	0	0	0x44
8 ports 5–12 (data bits D0–D7)	R/$\overline{W}$	1	0	0	0	1	0	1	0x45
8 ports 6–13 (data bits D0–D7)	R/$\overline{W}$	1	0	0	0	1	1	0	0x46
8 ports 7–14 (data bits D0–D7)	R/$\overline{W}$	1	0	0	0	1	1	1	0x47
8 ports 8–15 (data bits D0–D7)	R/$\overline{W}$	1	0	0	1	0	0	0	0x48
8 ports 9–16 (data bits D0–D7)	R/$\overline{W}$	1	0	0	1	0	0	1	0x49
8 ports 10–17 (data bits D0–D7)	R/$\overline{W}$	1	0	0	1	0	1	0	0x4A
8 ports 11–18 (data bits D0–D7)	R/$\overline{W}$	1	0	0	1	0	1	1	0x4B
8 ports 12–19 (data bits D0–D7)	R/$\overline{W}$	1	0	0	1	1	0	0	0x4C
8 ports 13–20 (data bits D0–D7)	R/$\overline{W}$	1	0	0	1	1	0	1	0x4D
8 ports 14–21 (data bits D0–D7)	R/$\overline{W}$	1	0	0	1	1	1	0	0x4E
8 ports 15–22 (data bits D0–D7)	R/$\overline{W}$	1	0	0	1	1	1	1	0x4F
8 ports 16–23 (data bits D0–D7)	R/$\overline{W}$	1	0	1	0	0	0	0	0x50
8 ports 17–24 (data bits D0–D7)	R/$\overline{W}$	1	0	1	0	0	0	1	0x51
8 ports 18–25 (data bits D0–D7)	R/$\overline{W}$	1	0	1	0	0	1	0	0x52
8 ports 19–26 (data bits D0–D7)	R/$\overline{W}$	1	0	1	0	0	1	1	0x53
8 ports 20–27 (data bits D0–D7)	R/$\overline{W}$	1	0	1	0	1	0	0	0x54
8 ports 21–28 (data bits D0–D7)	R/$\overline{W}$	1	0	1	0	1	0	1	0x55
8 ports 22–29 (data bits D0–D7)	R/$\overline{W}$	1	0	1	0	1	1	0	0x56
8 ports 23–30 (data bits D0–D7)	R/$\overline{W}$	1	0	1	0	1	1	1	0x57
8 ports 24–31 (data bits D0–D7)	R/$\overline{W}$	1	0	1	1	0	0	0	0x58
7 ports 25–31 (data bits D0–D6. D7 reads as 0)	R/$\overline{W}$	1	0	1	1	0	0	1	0x59
6 ports 26–31 (data bits D0–D5. D6–D7 read as 0)	R/$\overline{W}$	1	0	1	1	0	1	0	0x5A
5 ports 27–31 (data bits D0–D4. D5–D7 read as 0)	R/$\overline{W}$	1	0	1	1	0	1	1	0x5B
4 ports 28–31 (data bits D0–D3. D4–D7 read as 0)	R/$\overline{W}$	1	0	1	1	1	0	0	0x5C
3 ports 29–31 (data bits D0–D2. D3–D7 read as 0)	R/$\overline{W}$	1	0	1	1	1	0	1	0x5D
2 ports 30–31 (data bits D0–D1. D2–D7 read as 0)	R/$\overline{W}$	1	0	1	1	1	1	0	0x5E
1 port 31 only (data bit D0. D1–D7 read as 0)	R/$\overline{W}$	1	0	1	1	1	1	1	0x5F

Note: *Unused bits read as 0.*

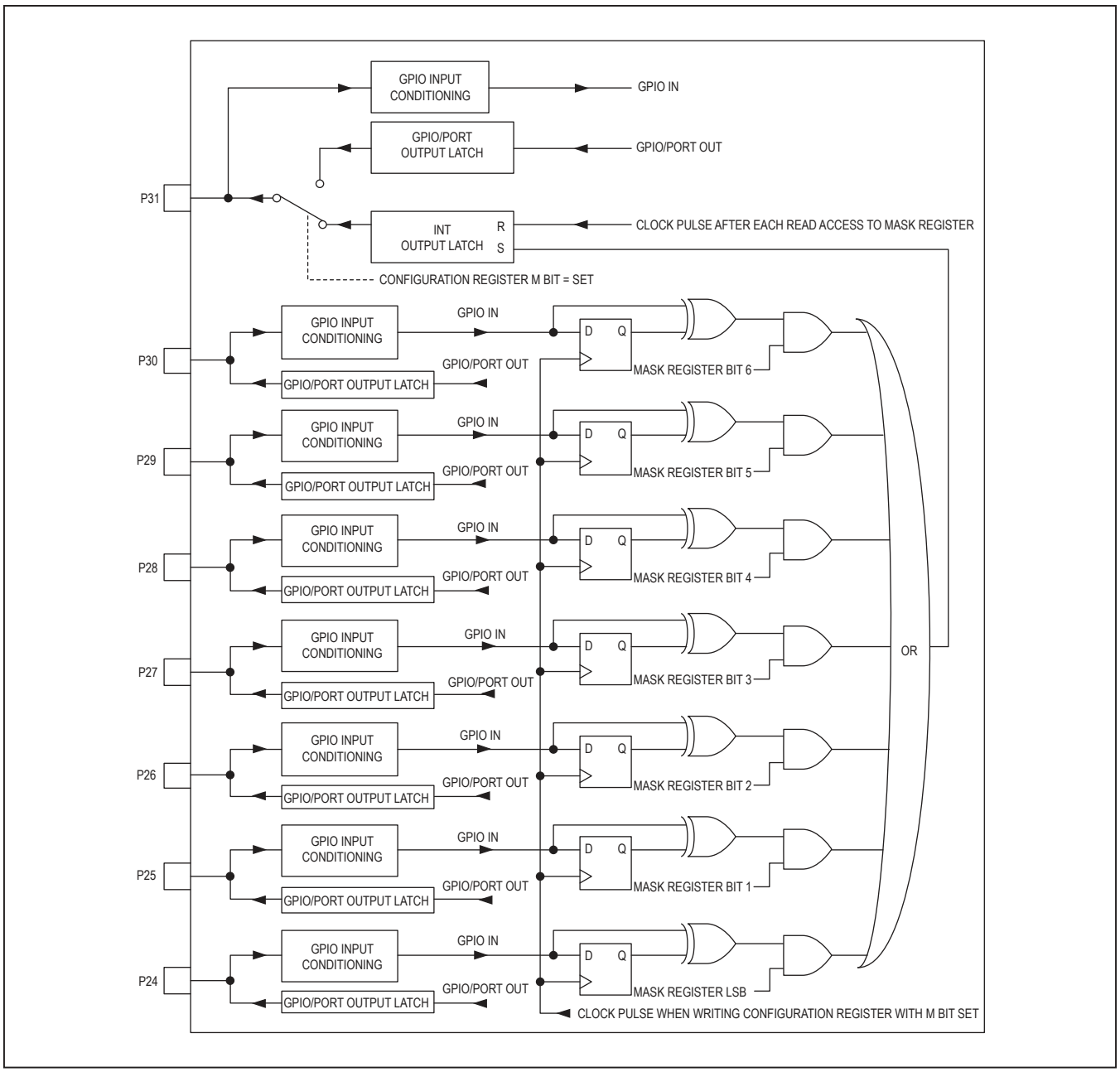


Figure 5. Maskable GPIO Ports P24 Through P31

Table 4. Power-Up Configuration

REGISTER FUNCTION	POWER-UP CONDITION	ADDRESS CODE (HEX)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Port Register Bits 4 to 31	GPIO Output Low	0x24 to 0x3F	X	X	X	X	X	X	X	0
Configuration Register	Shutdown Enabled Transition Detection Disabled	0x04	0	0	X	X	X	X	X	0
Input Mask Register	All Clear (Masked Off)	0x06	X	0	0	0	0	0	0	0
Port Configuration	P7, P6, P5, P4: GPIO Inputs Without Pullup	0x09	1	0	1	0	1	0	1	0
Port Configuration	P11, P10, P9, P8: GPIO Inputs Without Pullup	0x0A	1	0	1	0	1	0	1	0
Port Configuration	P15, P14, P13, P12: GPIO Inputs Without Pullup	0x0B	1	0	1	0	1	0	1	0
Port Configuration	P19, P18, P17, P16: GPIO Inputs Without Pullup	0x0C	1	0	1	0	1	0	1	0
Port Configuration	P23, P22, P21, P20: GPIO Inputs Without Pullup	0x0D	1	0	1	0	1	0	1	0
Port Configuration	P27, P26, P25, P24: GPIO Inputs Without Pullup	0x0E	1	0	1	0	1	0	1	0
Port Configuration	P31, P30, P29, P28: GPIO Inputs Without Pullup	0x0F	1	0	1	0	1	0	1	0

X = Unused bits; if read, zero results.

Table 5. Configuration Register Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Configuration Register	0x04	M	0	X	X	X	X	X	S

Table 6. Shutdown Control (S Data Bit D0) Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown	0x04	M	0	X	X	X	X	X	0
Normal Operation	0x04	M	0	X	X	X	X	X	1

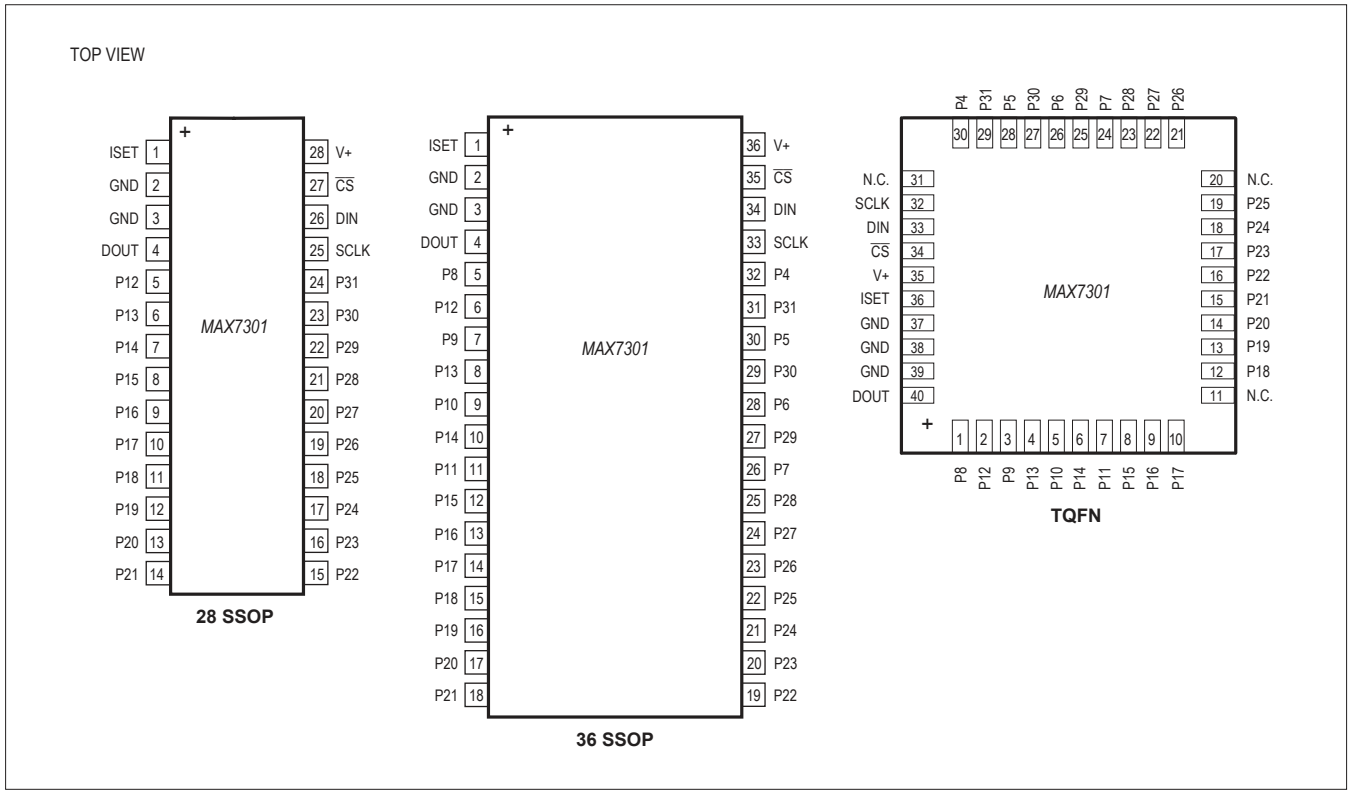
Table 7. Transition Detection Control (M Data Bit D7) Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Disabled	0x04	0	0	X	X	X	X	X	S
Enabled	0x04	1	0	X	X	X	X	X	S

Table 8. Transition Detection Mask Register

FUNCTION	REGISTER ADDRESS (HEX)	READ/ WRITE	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Mask Register	0x06	Read	0	Port 30 mask	Port 29 mask	Port 28 mask	Port 27 mask	Port 26 mask	Port 25 mask	Port 24 mask
		Write	Unchanged							

Pin Configurations



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
28 SSOP	A28+1	**21-0056**	**90-0095**
36 SSOP	A36+4	**21-0040**	**90-0098**
40 TQFN-EP	T4066+5	**21-0141**	**90-0055**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/02	Initial Release	—
1	10/02	Updated *General Description*, *Detailed Description*, *Initial Power-Up* section, Table 3 and Table 8	1, 5, 7, 8, 11, 14, 15
2	2/03	Corrected input leakage current	2
3	11/03	Updated Table 2, Table 3, Figure 5, *Serial Interface*, *Reading Device Registers*, *Transition (Port Data Change) Detection* sections. Added *SPI Routing Configuration* and *PCB Layout Considerations* sections. Added the 36 SSOP package outline	1, 5–12, 17
4	5/04	Various corrections to data sheet	5, 9, 15, 16
5	2/06	Removed MAX7301AGL and ANI package, added MAX7301ATL+ package	1, 2, 5, 9, 15, 17
6	4/06	Updated *Absolute Maximum Ratings*, corrected *Pin Configuration* and package outlines	2, 5, 15, 16, 17
7	7/14	Removed automotive reference from data sheet	1
8	5/15	Updated *Benefits and Features* section	1
9	8/19	Updated *Reading Device Registers* section	7
10	8/20	Updated *Shutdown* section	5

