DS36954 Quad Differential Bus Transceiver

Check for Samples: DS36954

FEATURES

- **Pinout for SCSI Interface**
- **Compact 20-Pin PLCC or SOIC Package**
- **Meets EIA-485 Standard for Multipoint Bus Transmission**
- **Greater than 60 mA Source/Sink Currents**
- **Thermal Shutdown Protection**
- **Glitch-Free Driver Outputs on Power Up and Down**

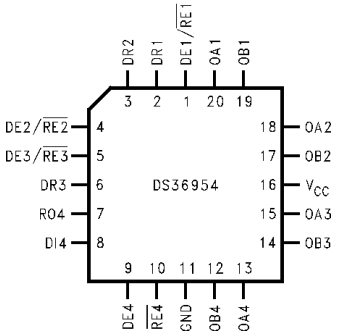
DESCRIPTION

The DS36954 is a low power, quad EIA-485 differential bus transceiver especially suited for high speed, parallel, multipoint, I/O bus applications. A compact 20-pin surface mount PLCC or SOIC package provides high transceiver integration and a very small PC board footprint.

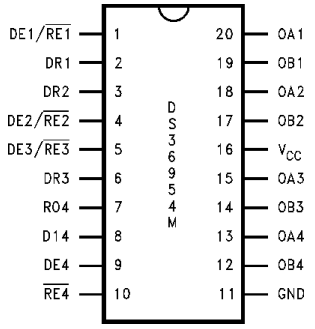
Propagation delay skew between devices is specified to aid in parallel interface designs—limits on maximum and minimum delay times are verified.

Five devices can implement a complete SCSI initiator or target interface. Three transceivers in a package are pinned out for data bus connections. The fourth transceiver, with the flexibility provided by its individual enables, can serve as a control bus transceiver.

Connection Diagram

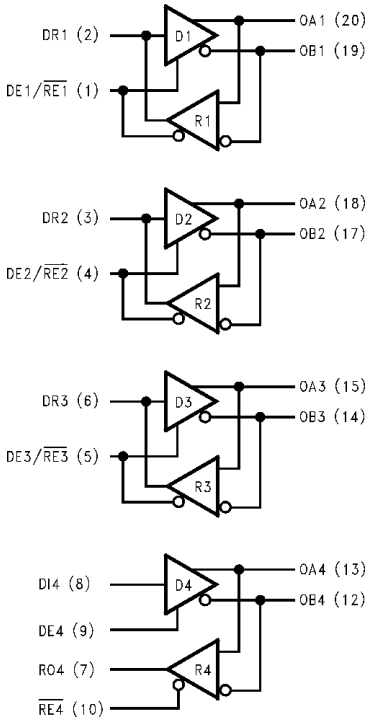


See Package Number FN (S-PQCC-J20)



See Package Number DW (R-PDSO-G20)

Logic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage	7V
Control Input Voltage	V_{CC} + 0.5V
Driver Input Voltage	V_{CC} + 0.5V
Driver Output Voltage/Receiver Input Voltage	−10V to +15V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ +25°C	
FN Package	1.73W
DW Package	1.73W
Derate FN Package	13.9 mW/°C above +25°C
Derate DW Package	13.7 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 Sec.)	260°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instrument Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temperature (T_A)	0	+70	°C

Electrical Characteristics (1)(2)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_{ODL}	Differential Driver Output Voltage (Full Load)	I_L = 60 mA		1.5	1.9		V
		V_{CM} = 0V					
V_{OD}	Differential Driver Output Voltage (Termination Load)	R_L = 100Ω (EIA-422)		2.0	2.25		V
		R_L = 54Ω (EIA-485)		1.5	2.0		V
ΔIVODI	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R_L = 54 or 100Ω (3)(*Figure 1*) (EIA-422/485)				0.2	V
V_{OC}	Driver Common Mode Output Voltage (4)	R_L = 54Ω (*Figure 1*) (EIA-485)				3.0	V
ΔIVOCI	Change in Magnitude of Common Mode Output Voltage	(3)(*Figure 1*) (EIA-422/485)				0.2	V
V_{OH}	Output Voltage High	I_{OH} = −55 mA		2.7	3.2		V
V_{OL}	Output Voltage Low	I_{OL} = 55 mA			1.4	1.7	V
V_{IH}	Input Voltage High			2.0			V
V_{IL}	Input Voltage Low					0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
(2) All typicals are given for V_{CC} = 5V and T_A = 25°C.
(3) Δ IVODI and Δ IVOCI are changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes state.
(4) In EIA Standards EIA-422 and EIA-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS} .

Electrical Characteristics [1][2] (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	Input High Current	V_{IN} = 2.4V [5]				20	µA
I_{IL}	Input Low Current	V_{IN} = 0.4V [5]				−20	µA
I_{OSC}	Driver Short-Circuit Output Current [6]	V_O = −7V (EIA-485)			−130	−250	mA
		V_O = 0V (EIA-422)			−90	−150	mA
		V_O = +12V (EIA-485)			130	250	mA
RECEIVER CHARACTERISTICS							
I_{OSR}	Short Circuit Output Current	V_O = 0V [6]		−15	−28	−75	mA
I_{OZ}	TRI-STATE Output Current	V_O = 0.4V to 2.4V				20	µA
V_{OH}	Output Voltage High	V_{ID} = 0.2V, I_{OH} = 0.4 mA		2.4	3.0		V
V_{OL}	Output Voltage Low	V_{ID} = −0.2V, I_{OL} = 4 mA			0.35	0.5	V
V_{TH}	Differential Input High Threshold Voltage	V_O = V_{OH}, I_O = −0.4 mA (EIA-422/485)			0.03	0.2	V
V_{TL}	Differential Input Low Threshold Voltage [7]	V_O = V_{OL}, I_O = 4.0 mA (EIA-422/485)		−0.20	−0.03		V
V_{HST}	Hysteresis [8]	V_{CM} = 0V		35	60		mV
DRIVER AND RECEIVER CHARACTERISTICS							
V_{IH}	Enable Input Voltage High			2.0			V
V_{IL}	Enable Input Voltage Low					0.8	V
V_{CL}	Enable Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
I_{IN}	Line Input Current [9]	Other Input = 0V DE/$\overline{RE}$ = 0.8V DE4 = 0.8V	V_I = +12V		0.5	1.0	mA
			V_I = −7V		−0.45	−0.8	mA
I_{ING}	Line Input Current [9]	Other Input = 0V DE/$\overline{RE}$ and DE4 = 2V V_{CC} = 3.0V T_A = +25°C	V_I = +12V			1.0	mA
			V_I = −7V			−0.8	mA
I_{IH}	Enable Input Current High	V_{IN} = 2.4V DE/$\overline{RE}$	V_{CC} = 3.0V		1	40	µA
			V_{CC} = 4.75V		1		µA
			V_{CC} = 5.25V		1	40	µA
		V_{IN} = 2.4V DE4 or $\overline{RE4}$	V_{CC} = 3.0V		1	20	µA
			V_{CC} = 5.25V		1	20	µA
I_{IL}	Enable Input Current Low	V_{IN} = 0.8V DE/$\overline{RE}$	V_{CC} = 3.0V		−6	−40	µA
			V_{CC} = 4.75V		−12		µA
			V_{CC} = 5.25V		−14	−40	µA
		V_{IN} = 0.8V DE4 or $\overline{RE4}$	V_{CC} = 3.0V		−3	−20	µA
			V_{CC} = 5.25V		−7	−20	µA
I_{CCD}	Supply Current [10]	No Load, DE/$\overline{RE}$ and DE4 = 2.0V			75	90	mA
I_{CCR}	Supply Current [10]	No Load, DE/$\overline{RE}$ and $\overline{RE4}$ = 0.8V			50	70	mA

(5) I_{IH} and I_{IL} include driver input current and receiver TRI-STATE leakage current on DR(1–3).
(6) Short one output at a time.
(7) Threshold parameter limits specified as an algebraic value rather than by magnitude.
(8) Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.
(9) I_{IN} includes the receiver input current and driver TRI-STATE leakage current.
(10) Total package supply current.

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER SINGLE-ENDED CHARACTERISTICS							
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω	(Figure 6)		35	40	ns
t_{PZL}	Output Enable Time to Low Level		(Figure 8)		25	40	ns
t_{PHZ}	Output Disable Time to High Level		(Figure 6)		15	25	ns
t_{PLZ}	Output Disable Time to Low Level		(Figure 8)		35	40	ns
DRIVER DIFFERENTIAL CHARACTERISTICS							
t_r, t_f	Rise and Fall Time	R_L = 54Ω C_L = 50 pF C_D = 15 pF (Figure 3 Figure 4 (1))			13	16	ns
t_{PLHD}	Differential Propagation			9	15	19	ns
t_{PHLD}	Delays (2)			9	12	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Diff. Skew				3	6	ns
RECEIVER CHARACTERISTICS							
t_{PLHD}	Differential Propagation Delays	C_L = 15 pF V_{CM} = 2.0V (Figure 10)		9	14	19	ns
t_{PHLD}				9	13	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Diff. Receiver Skew				1	3	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF (Figure 15)			15	22	ns
t_{PZL}	Output Enable Time to Low Level				20	30	ns
t_{PHZ}	Output Disable Time from High Level				20	30	ns
t_{PLZ}	Output Disable Time from Low Level				17	25	ns

(1) Propagation Delay Timing for Calculations of Driver Differential Propagation Delays
(2) Differential propagation delays are calculated from single-ended propagation delays measured from driver input to the 20% and 80% levels on the driver outputs (Figure 16) .

PARAMETER MEASUREMENT INFORMATION

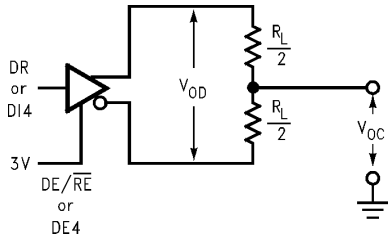


Figure 1. Driver V_{OD} and V_{OC} (3)

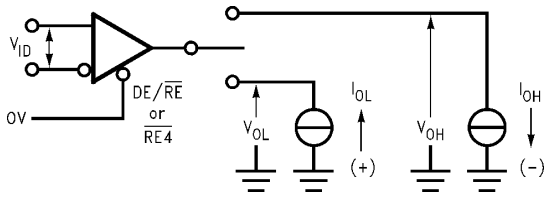
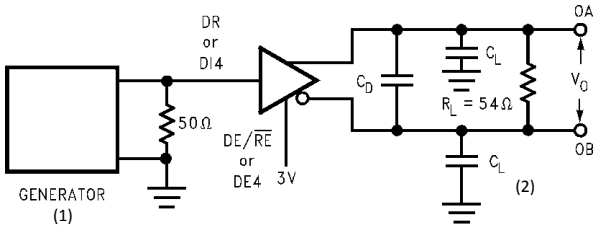


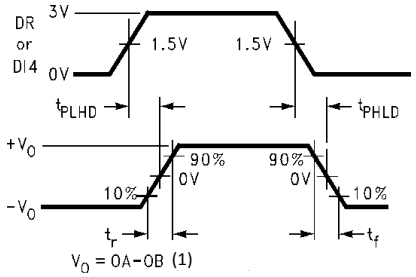
Figure 2. Receiver V_{OH} and V_{OL}



(1) The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, trand tf < 6.0 ns, ZO = 50Ω

(2) C_L includes probe and stray capacitance.

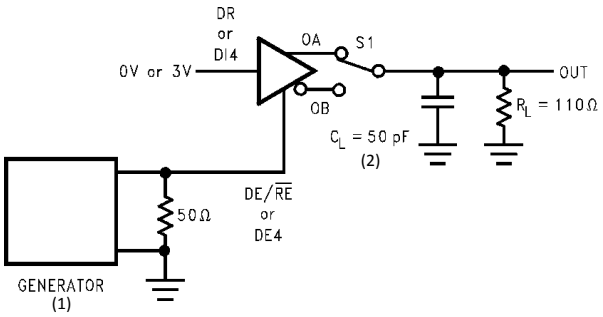
Figure 3. Driver Differential Propagation Delay Load Circuit



(1) Differential propagation delays are calculated from single-ended propagation delays measured from driver input to the 20% and 80% levels on the driver outputs (Figure 16).

Figure 4. Driver Differential Propagation Delays and Transition Times

(3) C_L includes probe and stray capacitance.



S1 to OA for DI = 3V
S1 to OB for DI = 0V

(1) The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, trand tf < 6.0 ns, ZO = 50Ω.

(2) C_L includes probe and stray capacitance.

Figure 5.

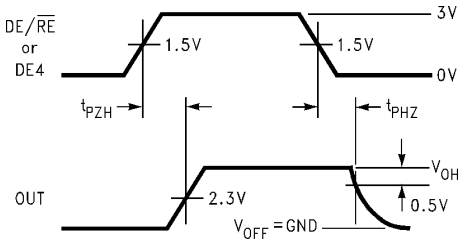
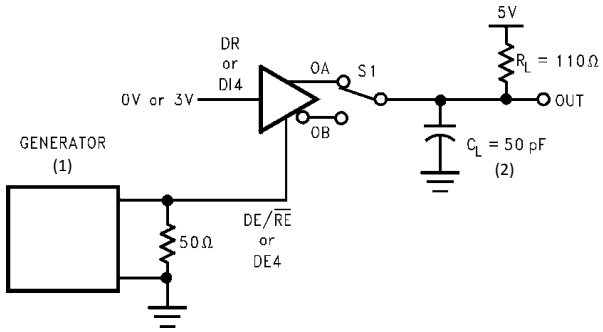


Figure 6. Driver Enable and Disable Timing (t_{PZH}, t_{PHZ})



S1 to OA for DI = 0V
S1 to OB for DI = 3V

(1) The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, trand tf < 6.0 ns, ZO = 50Ω.

(2) C_L includes probe and stray capacitance.

Figure 7.

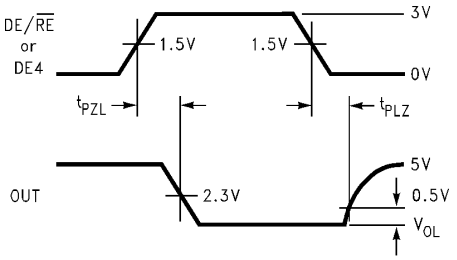
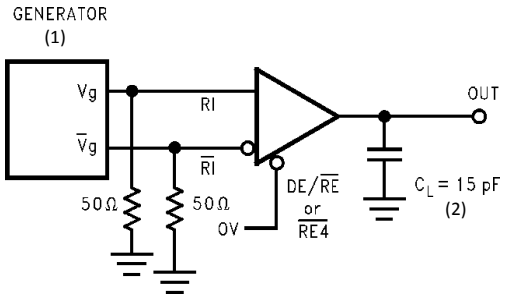


Figure 8. Driver Enable and Disable Timing (t_{PZL}, t_{PLZ})



(1) The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, trand tf < 6.0 ns, ZO = 50Ω.

(2) C_L includes probe and stray capacitance.

Figure 9.

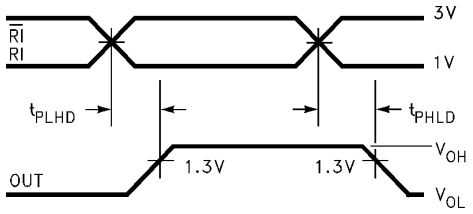
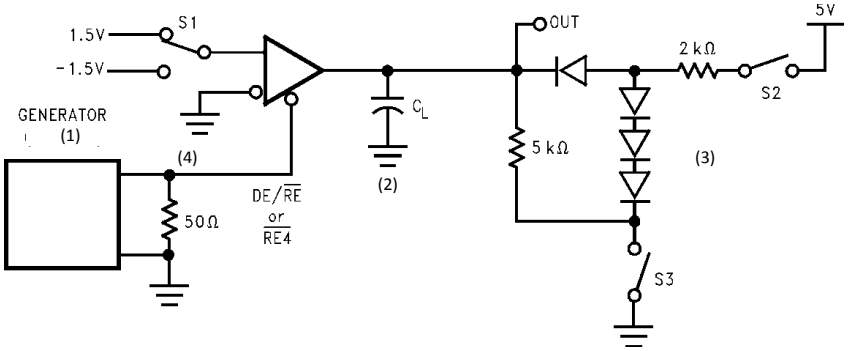


Figure 10. Receiver Differential Propagation Delay Timing



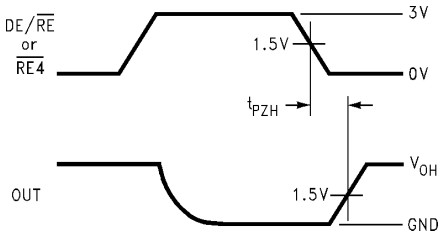
(1) The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, trand tf < 6.0 ns, ZO = 50Ω.

(2) C_L includes probe and stray capacitance.

(3) Diodes are 1N916 or equivalent.

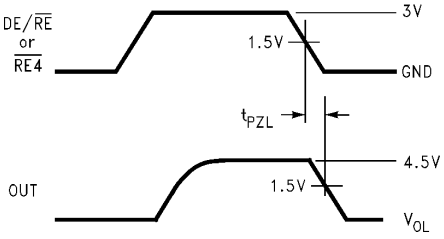
(4) On transceivers 1–3 the driver is loaded with receiver input conditions when DE/RE is high. Do not exceed the package power dissipation limit when testing.

Figure 11.



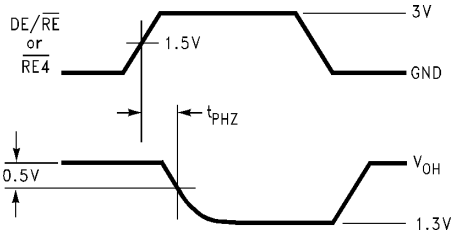
S1 1.5V
S2 Open
S3 Closed

Figure 12.



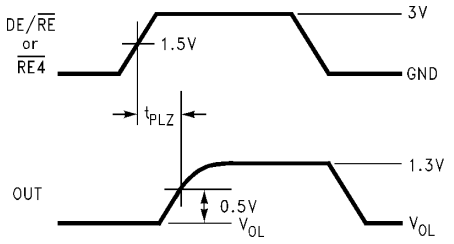
S1 −1.5V
S2 Closed
C3 Open

Figure 13.



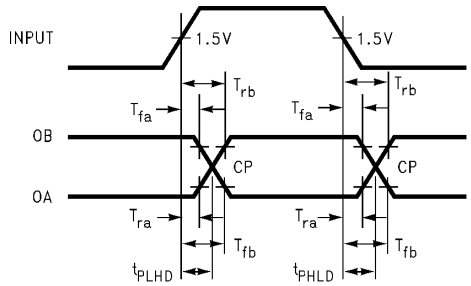
S1 1.5V
S2 Closed
C3 Closed

Figure 14.



S1 −1.5V
S2 Closed
C3 Closed

Figure 15. Receiver Enable and Disable Timing



$$T_{CP} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$$

T_{ra}, T_{rb}, T_{fa} and T_{fb} are propagation delay measurements to the 20% and 80% levels.
T_{CP} = Crossing Point

Figure 16. Propagation Delay Timing for Calculations of Driver Differential Propagation Delays

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS36954M	NRND	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	DS36954 M	
DS36954M/NOPB	ACTIVE	SOIC	DW	20	36	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	DS36954 M	Samples
DS36954MX/NOPB	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	DS36954 M	Samples
DS36954VX	NRND	PLCC	FN	20		TBD	Call TI	Call TI	0 to 70	DS36954V	
DS36954VX/NOPB	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2A-250C-4 WEEK	0 to 70	DS36954V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

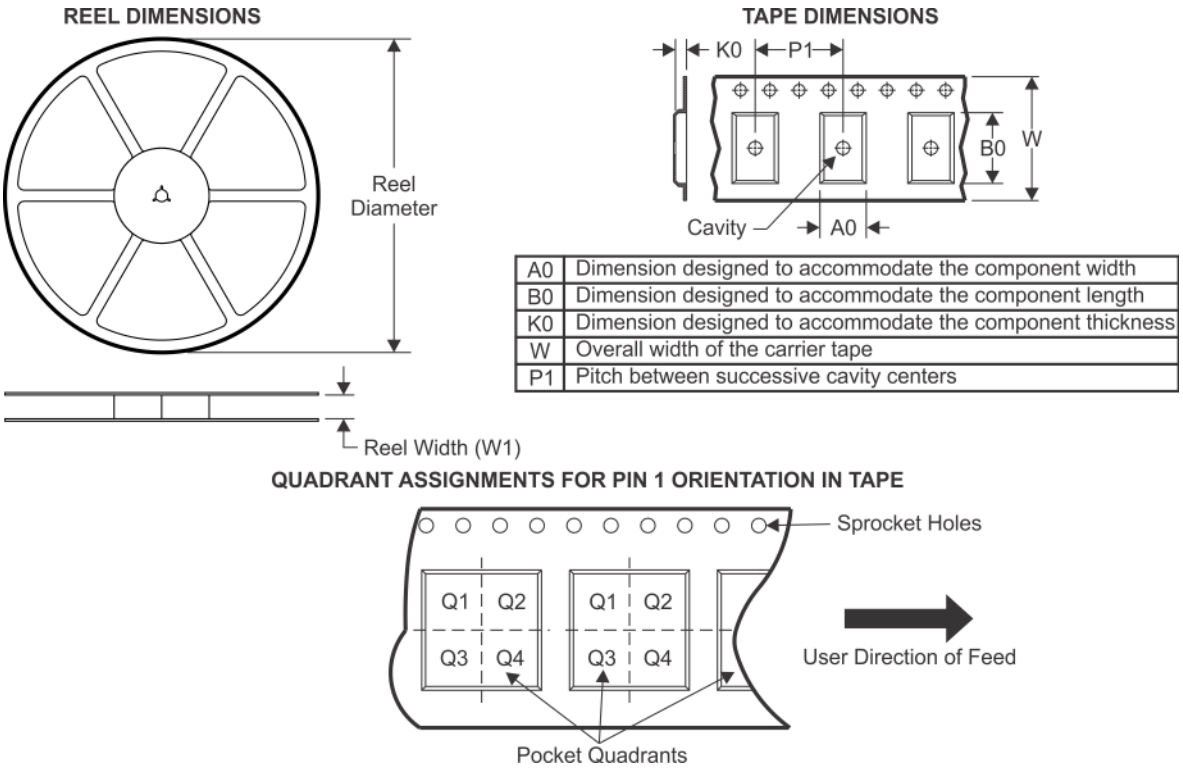
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

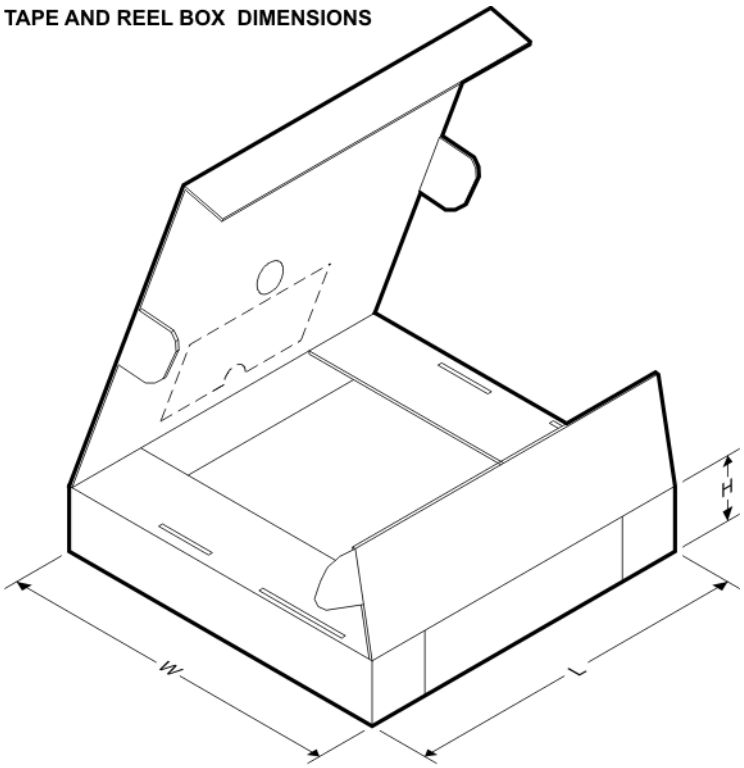


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS36954MX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

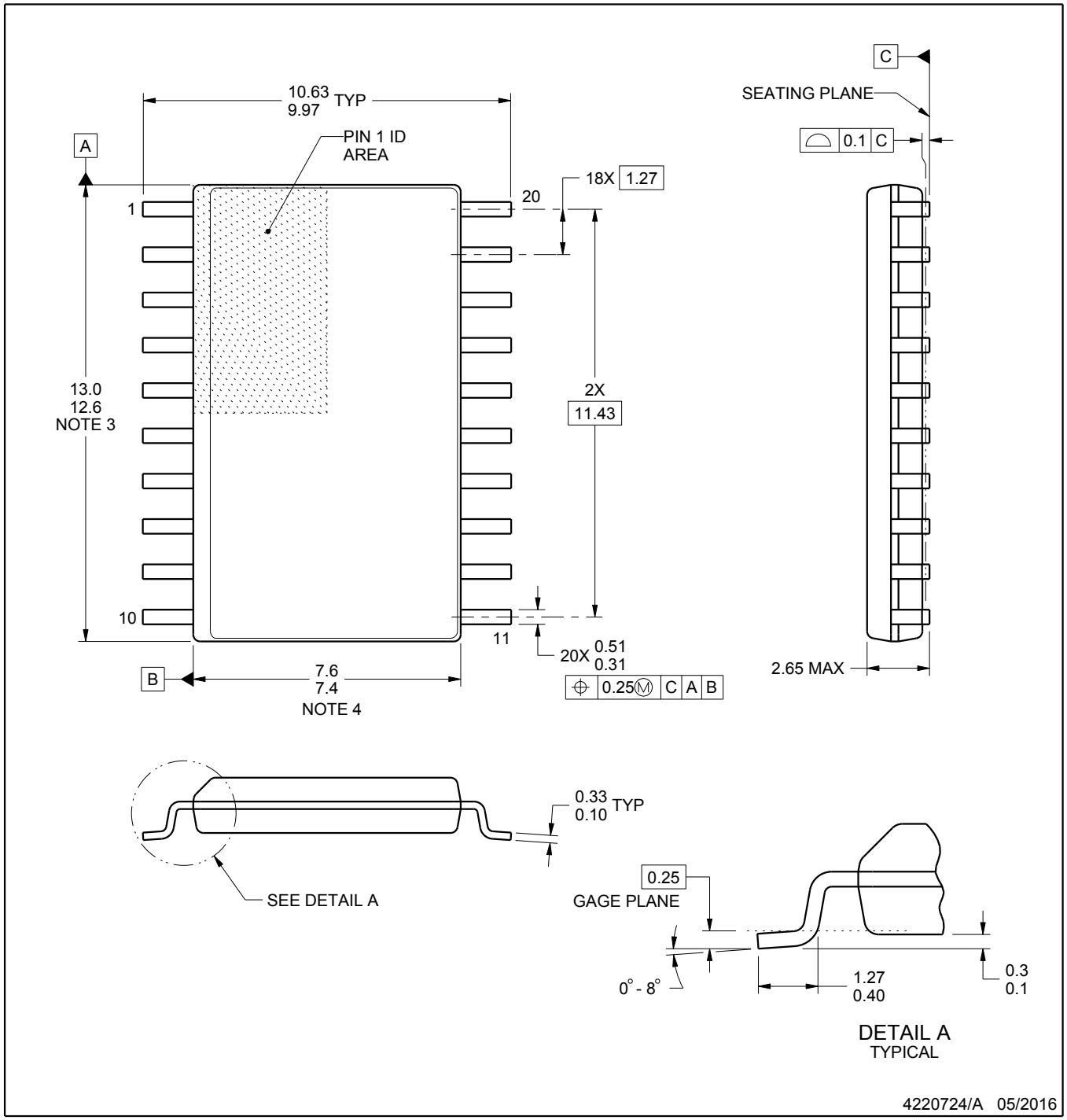
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS36954MX/NOPB	SOIC	DW	20	1000	367.0	367.0	45.0

PACKAGE OUTLINE

DW0020A

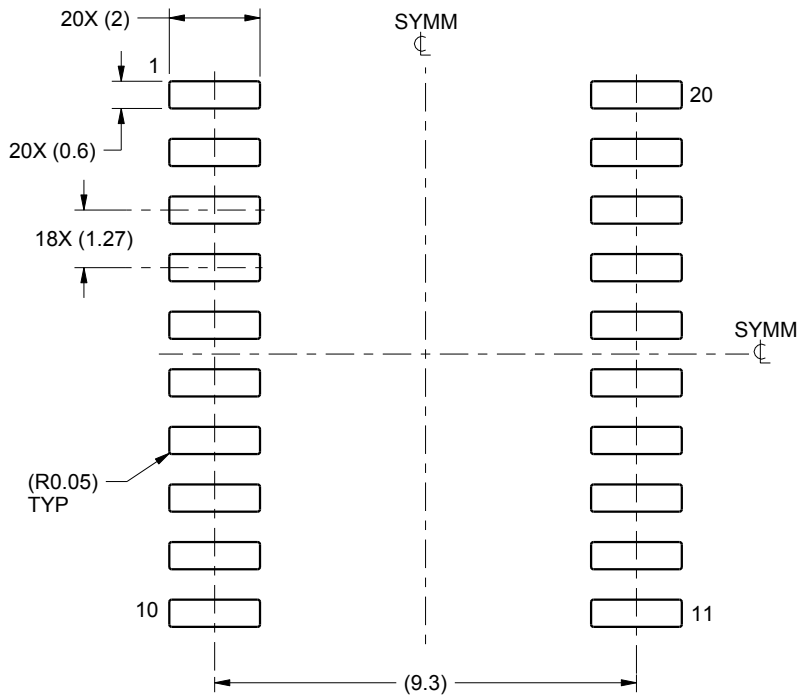
SOIC - 2.65 mm max height

SOIC

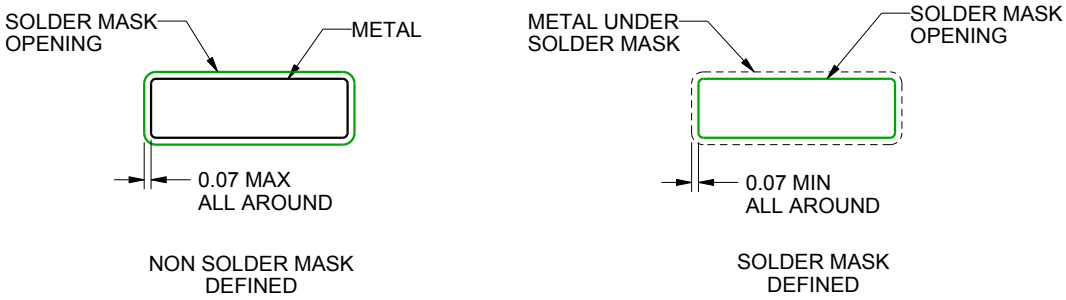


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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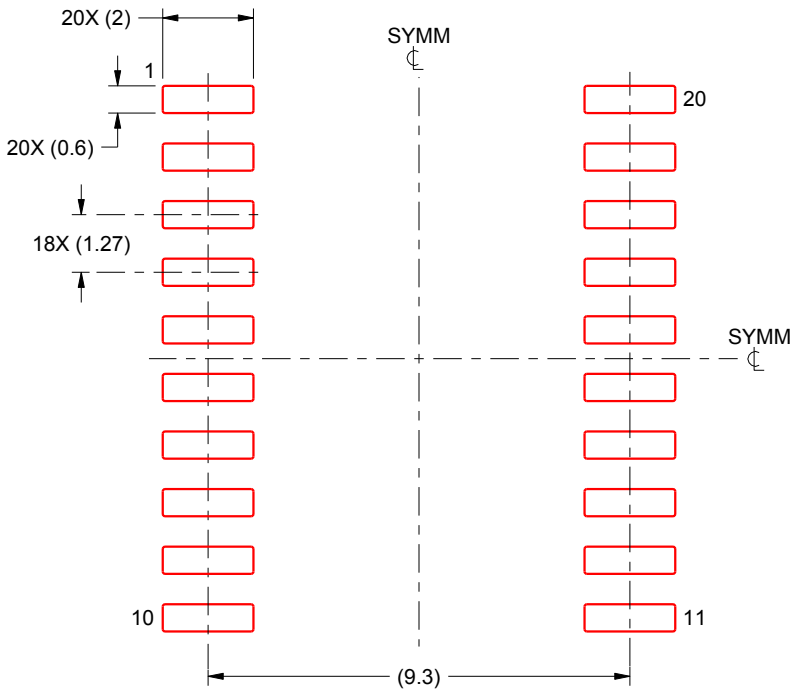
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

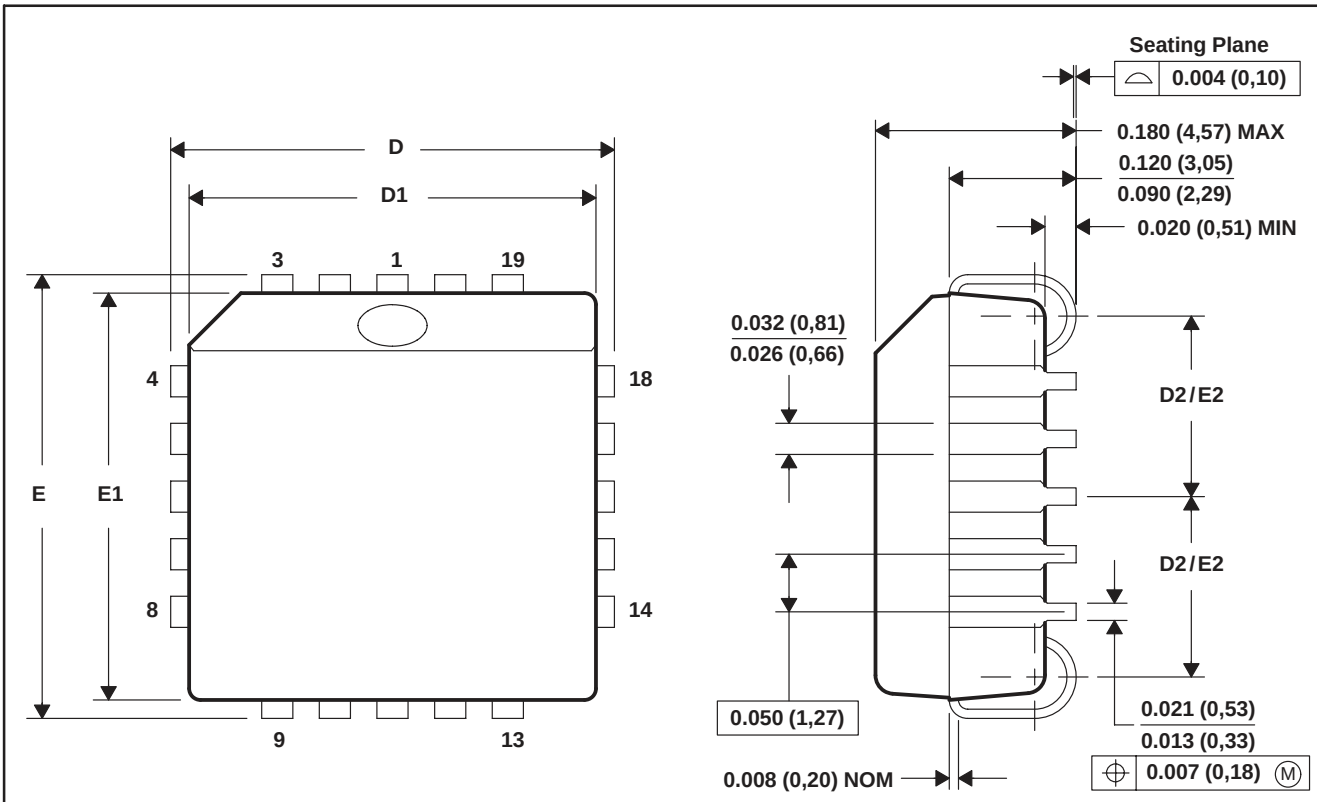
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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