

Features

- Industry Standard Architecture
 - Low-cost Easy-to-use Software Tools
- High-speed, Electrically Erasable Programmable Logic Devices
- CMOS and TTL Compatible Inputs and Outputs
 - Input and I/O Pull-up Resistors
- Advanced Flash Technology
 - Reprogrammable
 - 100% Tested
- High-reliability CMOS Process
 - 20 year Data Retention
 - 100 Erase/Write Cycles
 - 2,000V ESD Protection
 - 200mA Latchup Immunity
- Full Military Temperature Ranges
- Dual-in-line and Surface Mount Packages in Standard Pinouts
- PCI Compliant

Figure 0-1. Logic Diagram

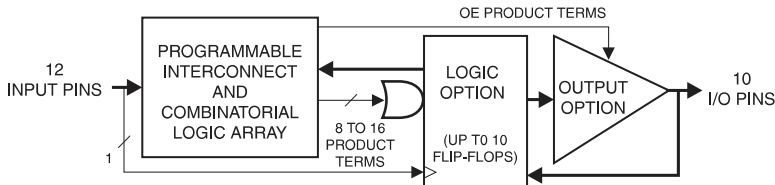
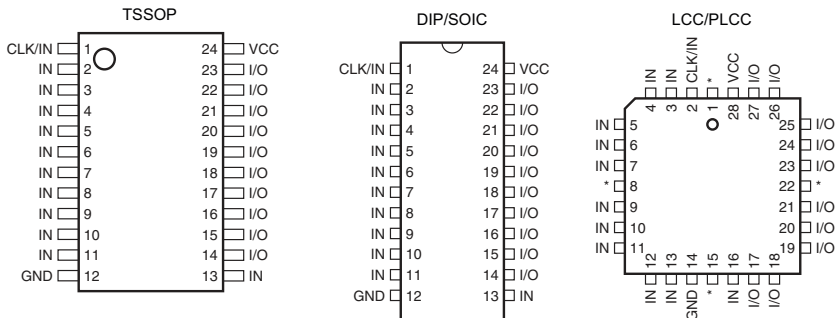


Figure 0-2. Pin Configurations

All Pinouts Top View

| Pin Name | Function |
|-----------------|------------------------|
| CLK | Clock |
| IN | Logic Inputs |
| I/O | Bidirectional Buffers |
| * | No Internal Connection |
| V _{CC} | +5V Supply |



High-performance Electrically Erasable Programmable Logic Device

Atmel ATF22V10B



1. Description

The Atmel® ATF22V10B is a high-performance CMOS (electrically erasable) programmable logic device (PLD) which utilizes the Atmel proven electrically erasable Flash memory technology. Speeds down to 7.5ns and power dissipation as low as 10mA are offered. All speed ranges are specified over the full $5V \pm 10\%$ range for military and industrial temperature ranges, and $5V \pm 5\%$ for commercial temperature ranges.

Several low-power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

2. Absolute Maximum Ratings*

| | |
|---|--------------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V ⁽¹⁾ |
| Voltage on Input Pins with Respect to Ground During Programming | -2.0V to +14.0V ⁽¹⁾ |
| Programming Voltage with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to 7.0V for pulses of less than 20ns.

3. DC and AC Operating Conditions

| | Commercial | Industrial | Military |
|-----------------------|-------------------------|---------------------------|-------------------------|
| Operating Temperature | 0°C - 70°C (Ambient) | -40°C - 85°C (Ambient) | -55°C - 125°C (Case) |
| V_{CC} Power Supply | $5V \pm 5\%$ | $5V \pm 10\%$ | $5V \pm 10\%$ |

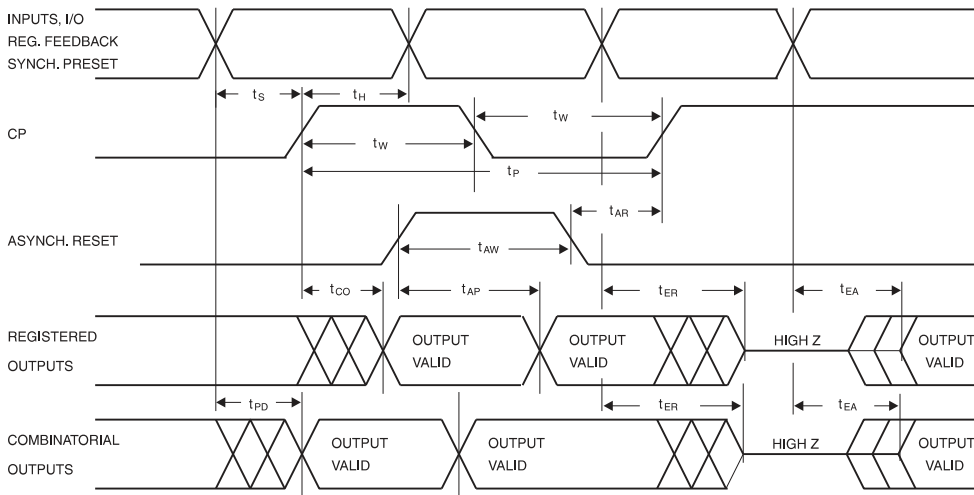
Note: 1. The shaded devices are obsolete

3.1 DC Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units | |
|----------------|-----------------------------------|---|--------------------------|------------|-----------------|---------------|----|
| I_{IL} | Input or I/O Low Leakage Current | $0 \leq V_{IN} \leq V_{IL} \text{ (Max)}$ | | -35 | -100 | μA | |
| I_{IH} | Input or I/O High Leakage Current | $3.5 \leq V_{IN} \leq V_{CC}$ | | | 10 | μA | |
| I_{CC} | Power Supply Current, Standby | $V_{CC} = \text{Max}, V_{IN} = \text{Max}, \text{Outputs Open}$ | B-7 | Com. | 85 | 120 | mA |
| | | | | Ind., Mil. | 85 | 140 | mA |
| I_{CC} | Power Supply Current, Standby | $V_{CC} = \text{Max}, V_{IN} = \text{Max}, \text{Outputs Open}$ | B-10 | Com./Ind. | 85/85 | 120/140 | mA |
| | | | | Mil. | 85 | 140 | mA |
| | | | B-15 | Com./Ind. | 65/65 | 90/115 | mA |
| | | | | Mil. | 65 | 115 | mA |
| | | | B-25 | Com. | 65 | 90 | mA |
| | | | | Ind., Mil. | 65 | 115 | mA |
| | | | BQ-15 | Com. | 35 | 55 | mA |
| | | | BQL-20, -25 | Com. | 5 | 10 | mA |
| Ind., Mil. | 5 | 15 | | mA | | | |
| I_{CC2} | Clocked Power Supply Current | $V_{CC} = \text{Max}, \text{Outputs Open}, f = 15\text{MHz}$ | B-7 | Com. | 90 | 120 | mA |
| | | | | Mil., Ind. | 90 | 145 | mA |
| | | | B-10 | Com./Ind. | 90/90 | 120/145 | mA |
| | | | | Mil. | 90 | 150 | mA |
| | | | B-15 | Com./Ind. | 65/65 | 90/120 | mA |
| | | | | Mil. | 65 | 150 | mA |
| | | | B-25 | Com. | 65 | 90 | mA |
| | | | | Ind., Mil. | 65 | 120 | mA |
| | | | BQ-15 | Com. | 40 | 60 | mA |
| | | | BQL-20, -25 | Com. | 20 | 50 | mA |
| Ind., Mil. | 20 | 70 | | mA | | | |
| $I_{OS}^{(1)}$ | Output Short Circuit Current | $V_{OUT} = 0.5\text{V}$ | | | -130 | mA | |
| V_{IL} | Input Low Voltage | | -0.5 | | 0.8 | V | |
| V_{IH} | Input High Voltage | | 2.0 | | $V_{CC} + 0.75$ | V | |
| V_{OL} | Output Low Voltage | $V_{IN} = V_{IH} \text{ or } V_{IL}, V_{CC} = \text{Min}$ | $I_{OL} = 16\text{mA}$ | Com., Ind. | | 0.5 | V |
| | | | $I_{OL} = 12\text{mA}$ | Mil. | | 0.5 | V |
| V_{OH} | Output High Voltage | $V_{IN} = V_{IH} \text{ or } V_{IL}, V_{CC} = \text{Min}$ | $I_{OH} = -4.0\text{mA}$ | 2.4 | | V | |

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec
 2. The shaded devices are obsolete

4. AC Waveforms⁽¹⁾



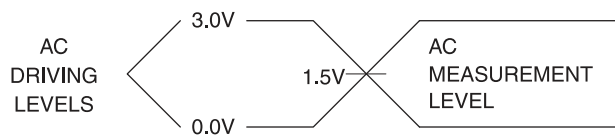
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified

5. AC Characteristics⁽¹⁾

| Symbol | Parameter | -10 | | -15 | | Units |
|-----------|--|-----|-----|------|-----|-------|
| | | Min | Max | Min | Max | |
| t_{PD} | Input or Feedback to Combinatorial Output | 3 | 10 | 3 | 15 | ns |
| t_{CO} | Clock to Output | 2 | 6.5 | 2 | 8 | ns |
| t_{CF} | Clock to Feedback | | 2.5 | | 2.5 | ns |
| t_S | Input or Feedback Setup Time | 4.5 | | 10 | | ns |
| t_H | Hold Time | 0 | | 0 | | ns |
| f_{MAX} | External Feedback $1/(t_S + t_{CO})$ | 90 | | 55.5 | | MHz |
| | Internal Feedback $1/(t_S + t_{CF})$ | 142 | | 69 | | MHz |
| | No Feedback $1/(t_{WH} + t_{WL})$ | 142 | | 83.3 | | MHz |
| t_W | Clock Width (t_{WL} and t_{WH}) | 3.5 | | 6 | | ns |
| t_{EA} | Input or I/O to Output Enable | 3 | 10 | 3 | 15 | ns |
| t_{ER} | Input or I/O to Output Disable | 3 | 9 | 3 | 15 | ns |
| t_{AP} | Input or I/O to Asynchronous Reset of Register | 3 | 12 | 3 | 20 | ns |
| t_{AW} | Asynchronous Reset Width | 8 | | 15 | | ns |
| t_{AR} | Asynchronous Reset Recovery Time | 6 | | 10 | | ns |
| t_{SP} | Setup Time, Synchronous Preset | 6 | | 10 | | ns |
| t_{SPR} | Synchronous Preset to Clock Recovery Time | 8 | | 10 | | ns |

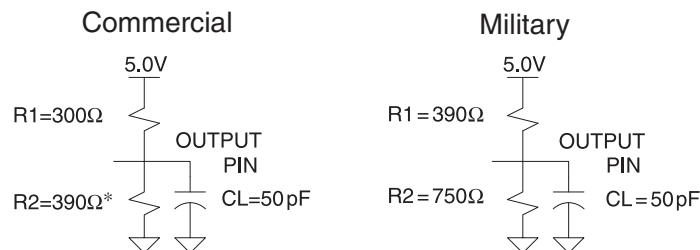
Notes: 1. See ordering information for valid part numbers

6. Input Test Waveforms and Measurement Levels



$t_R, t_F < 3ns$

7. Output Test Loads



* All except -7 which is R2 = 300Ω

8. Pin Capacitance

$f = 1MHz, T = 25^{\circ}C^{(1)}$

| | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 5 | 8 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 6 | 8 | pF | $V_{OUT} = 0V$ |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested

9. Power-up Reset

The registers in the Atmel® ATF22V10B are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high
3. The clock must remain stable during t_{PR}

10. Preload of Registered Outputs

The Atmel® ATF22V10B registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Figure 10-1.

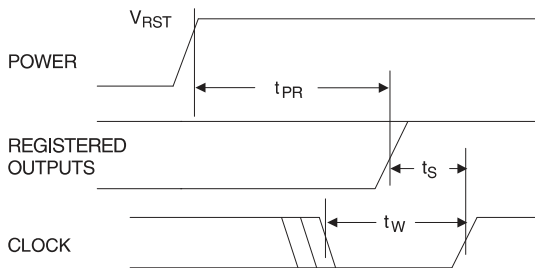


Table 10-1.

| Parameter | Description | Typ | Max | Units |
|-----------|------------------------|-----|-------|-------|
| t_{PR} | Power-up Reset Time | 600 | 1,000 | ns |
| V_{RST} | Power-up Reset Voltage | 3.8 | 4.5 | V |

11. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22V10B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

12. Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

13. Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware and Software Support* for information on software/programming.

14. Input and I/O Pull-ups

All Atmel® ATF22V10B family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to V_{CC} . This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

Figure 14-1. Input Diagram

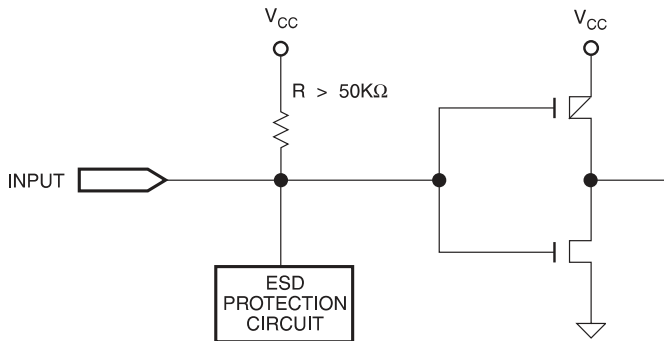


Figure 14-2. I/O Diagram

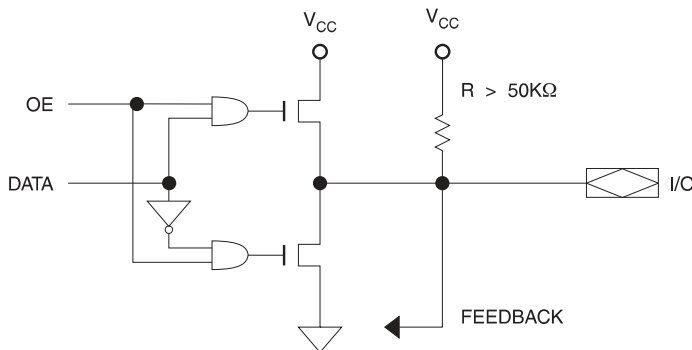
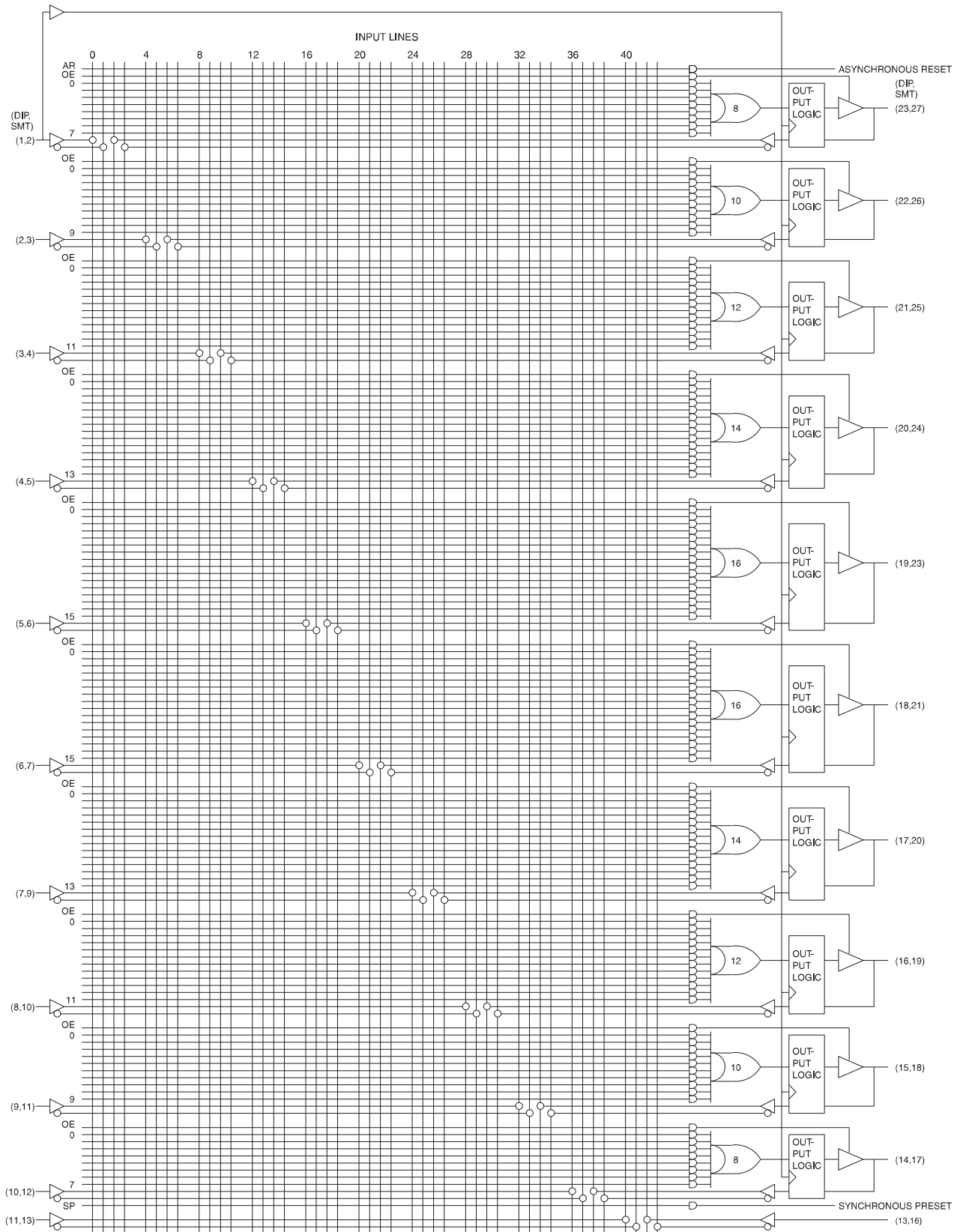
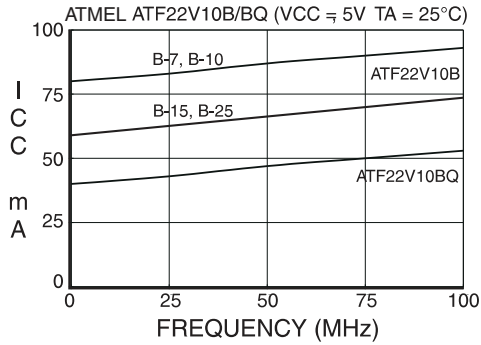


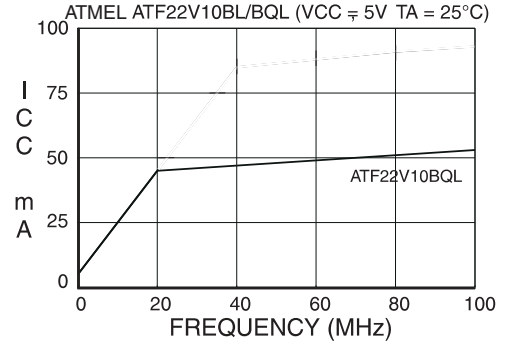
Figure 14-3. Functional Logic Diagram Atmel ATF22V10B



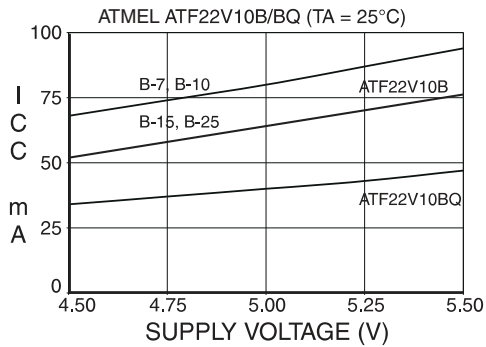
SUPPLY CURRENT vs. INPUT FREQUENCY



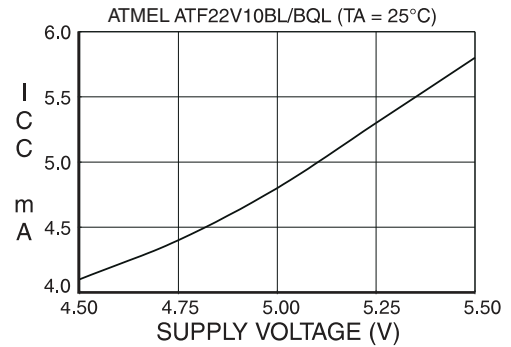
SUPPLY CURRENT vs. INPUT FREQUENCY



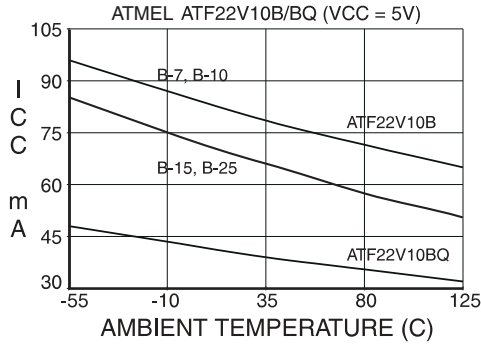
SUPPLY CURRENT vs. SUPPLY VOLTAGE



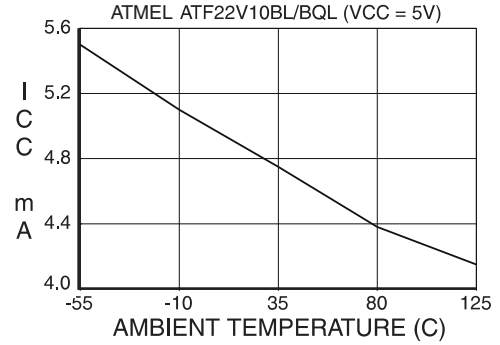
SUPPLY CURRENT vs. SUPPLY VOLTAGE



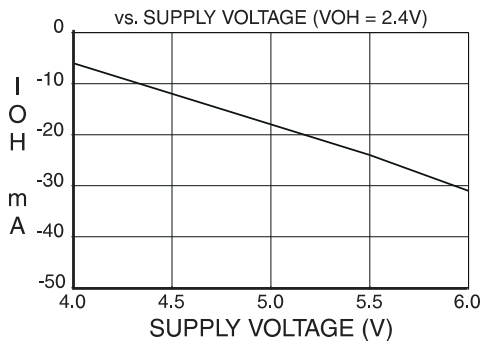
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



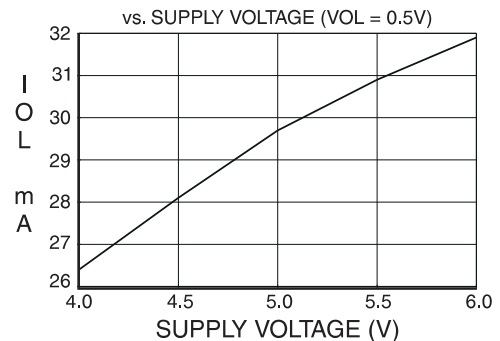
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

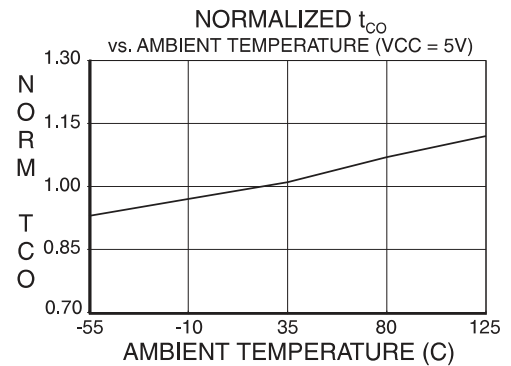
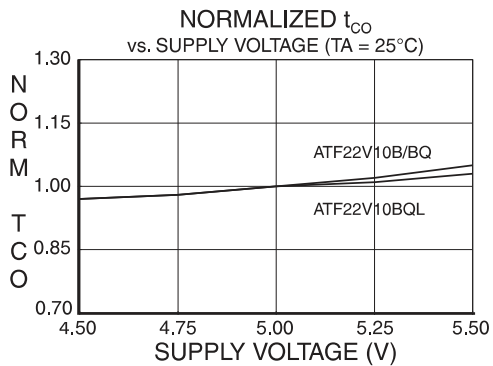
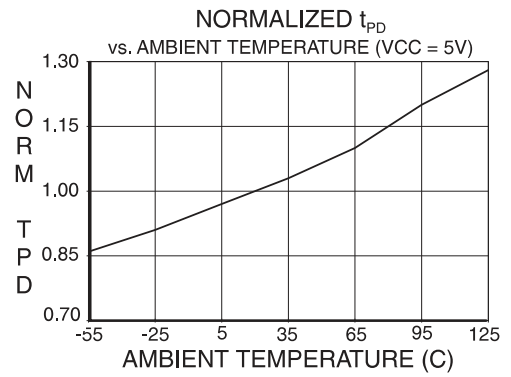
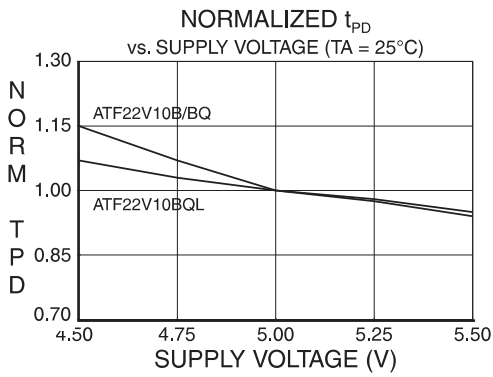
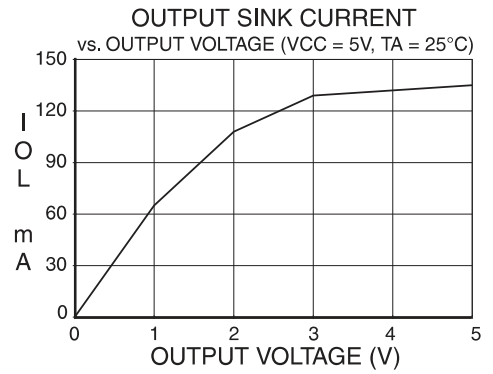
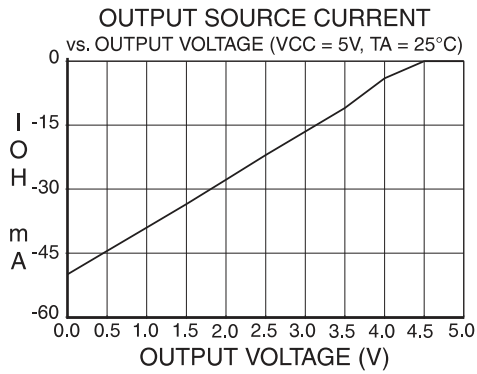
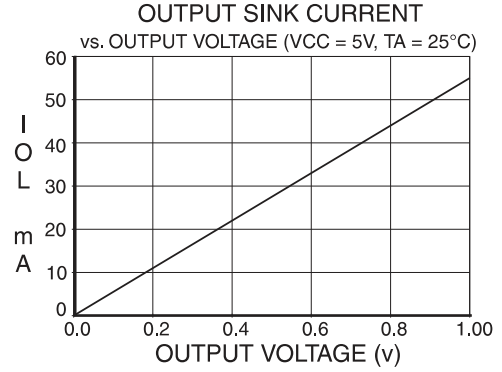
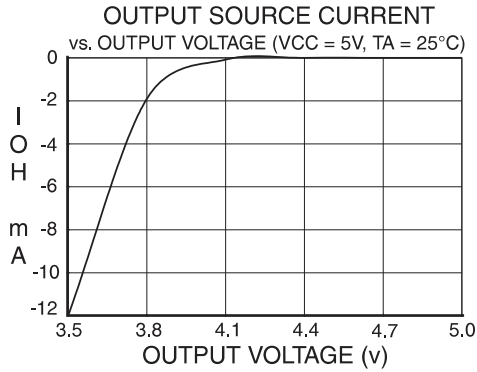


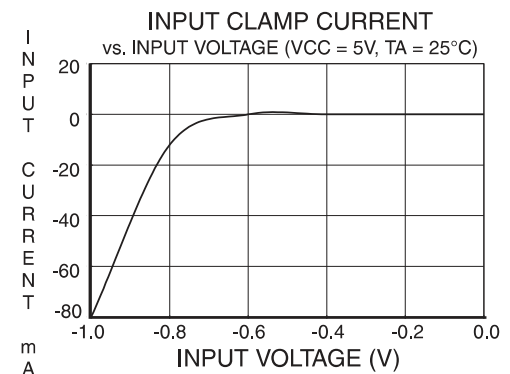
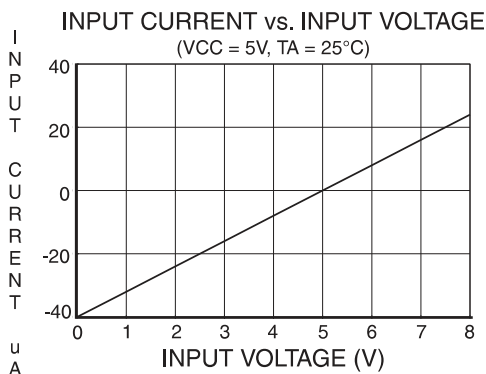
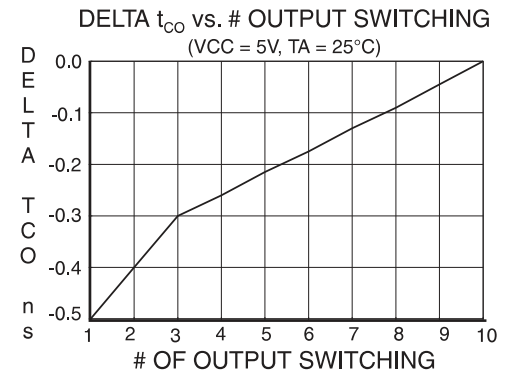
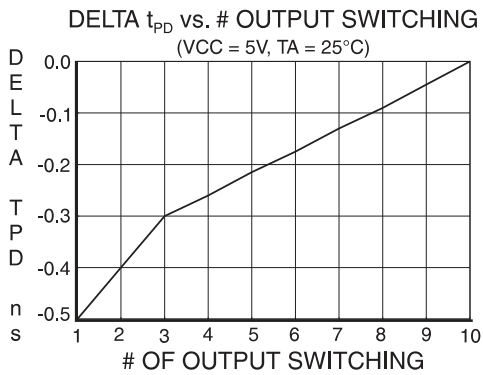
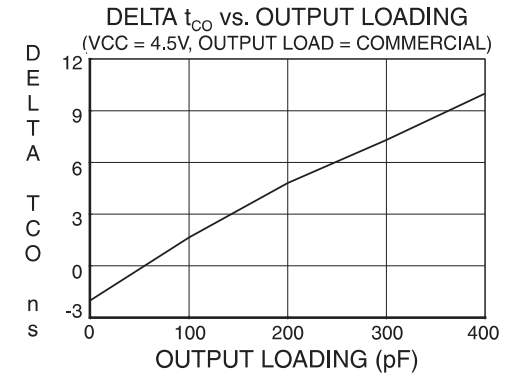
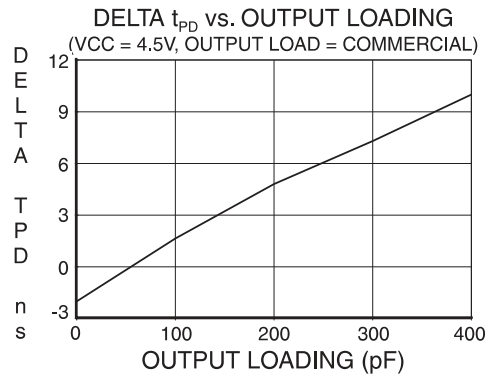
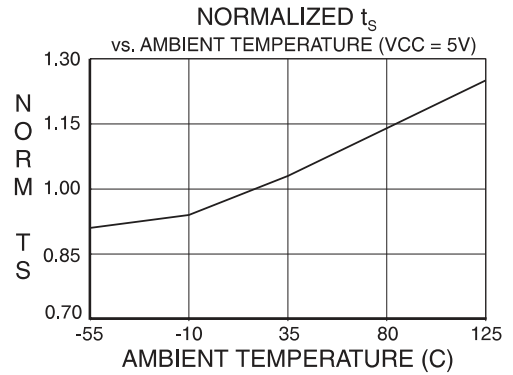
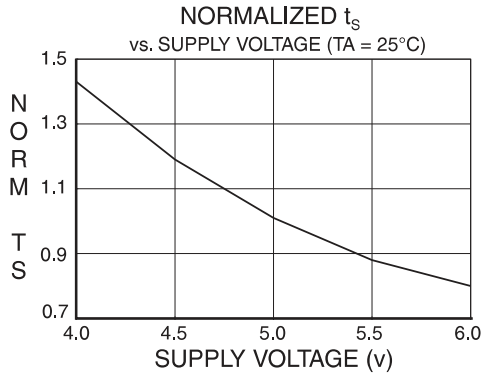
OUTPUT SOURCE CURRENT



OUTPUT SINK CURRENT







15. Ordering Information

15.1 Atmel ATF22V10B⁽²⁾ Ordering Detail

| t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | Ordering Code | Package | Operation Range |
|---------------|------------|---------------|--|-------------|---|
| 10 | 4.5 | 6.5 | ATF22V10B-10GM/883 ATF22V10B-10NM/883 | 24D3 28L | Military/883C (-55°C to 125°C) Class B, Fully Compliant |
| | | | 5962-89841 06LA 5962-89841 063X | 24D3 28L | Military (-55°C to 125°C) Class B, Fully Compliant |
| 15 | 10 | 8 | ATF22V10B-15GM/883 ATF22V10B-15NM/883 | 24D3 28L | Military/883C (-55°C to 125°C) Class B, Fully Compliant |
| | | | 5962-89841 03LA 5962-89841 033X | 24D3 28L | Military (-55°C to 125°C) Class B, Fully Compliant |

15.2 Atmel ATF22V10BQ(L)^(1,2) Ordering Detail

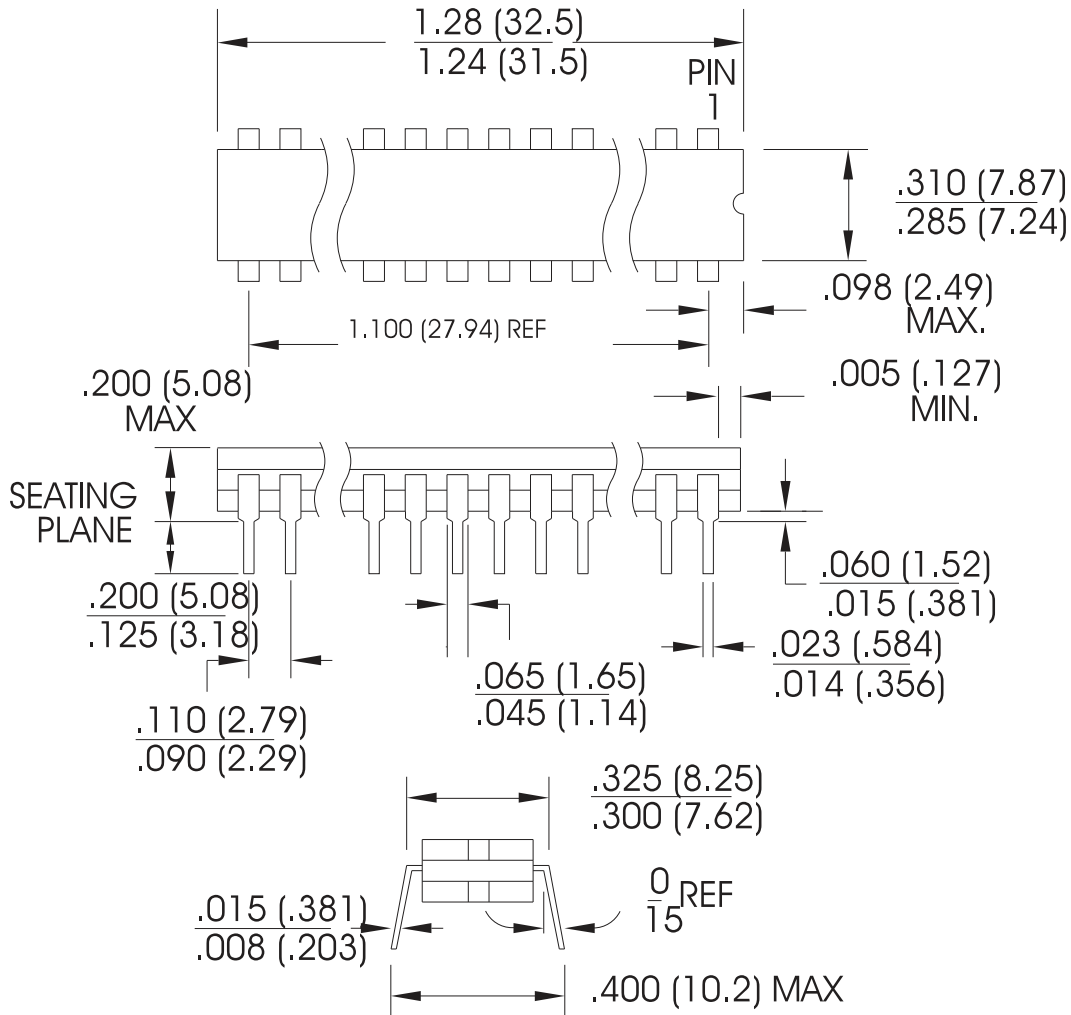
| t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | Ordering Code | Package | Operation Range |
|---------------|------------|---------------|--|-------------|---|
| 20 | 14 | 12 | ATF22V10BQL-20GM/883 ATF22V10BQL-20NM/883 | 24D3 28L | Military/883C (-55°C to 125°C) Class B, Fully Compliant |
| | | | 5962-89841 14 LA 5962-89841 14 3X | 24D3 28L | Military (-55°C to 125°C) Class B, Fully Compliant |
| 25 | 15 | 15 | ATF22V10BQL-25GM/883 ATF22V10BQL-25NM/883 | 24D3 28L | Military/883C (-55°C to 125°C) Class B, Fully Compliant |
| | | | 5962-89841 13 LA 5962-89841 13 3X | 24D3 28L | Military (-55°C to 125°C) Class B, Fully Compliant |

- Notes: 1. The shaded devices are obsolete
2. Please see DSCC DWG for military parts

16. Packaging Information

24D3

24D3, 24-lead, 0.300" Wide. Non-windowed,
 Ceramic Dual Inline Package (Cerdip)
 Dimensions in Millimeters and (Inches)*
 MIL-STD-1835 D-9 CONFIG A (Glass Sealed)



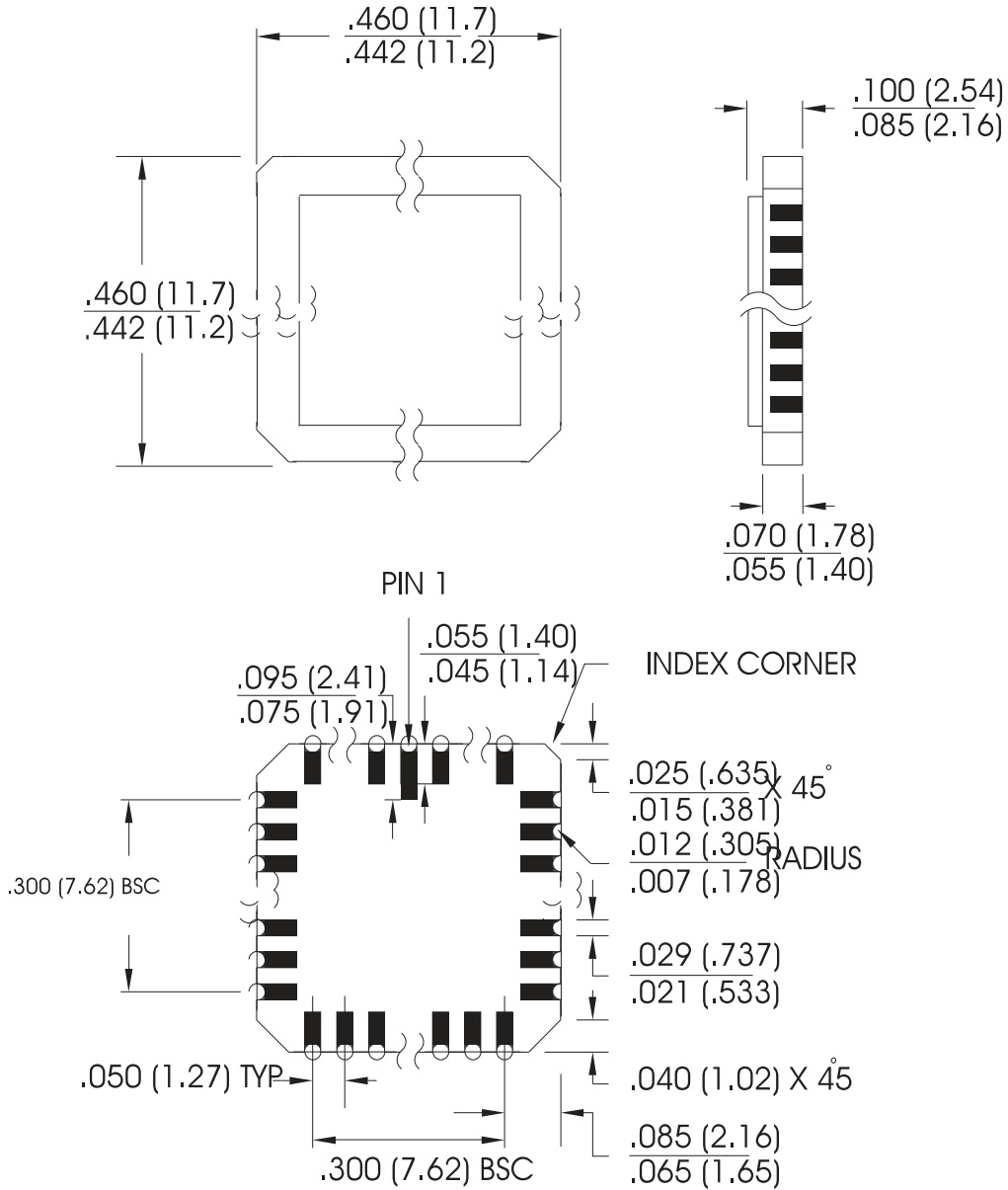
*Controlling dimension: Inches

REV. A 04/11/2001

28L

28L, 28-pad, Non-windowed, Ceramic lid, Leadless Chip Carrier (LCC)

Dimensions in Millimeters and (Inches)*
MIL-STD-1835 C-4



*Controlling dimension: Inches

17. Revision History

| Doc. Rev. | Date | Comments |
|-----------|---------|---|
| 0250M | 07/2010 | Removed all commercial and industrial grade leaded part offerings |



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