TC7126/A

3-1/2 Digit Analog-to-Digital Converters

Features:

- Internal Reference with Low Temperature Drift:
  - TC7126: 80ppm/°C, Typical
  - TC7126A: 35ppm/°C, Typical
- Zero Reading with Zero Input
- Low Noise: 15µV_{P-P}
- High Resolution: 0.05%
- Low Input Leakage Current: 1pA Typ., 10pA Max.
- Precision Null Detectors with True Polarity at Zero
- High-Impedance Differential Input
- Convenient 9V Battery Operation with Low-Power Dissipation: 500µW Typ., 900µW Max.

Applications:

- Thermometry
- Bridge Readouts: Strain Gauges, Load Cells, Null Detectors
- Digital Meters and Panel Meters:
  - Voltage/Current/Ohms/Power, pH
- Digital Scales, Process Monitors

Device Selection Table

Package Code	Package	Temperature Range
CPL	40-Pin PDIP	0°C to +70°C
IPL	40-Pin PDIP (TC7126 Only)	-25°C to +85°C
CKW	44-Pin PQFP	0°C to +70°C
CLW	44-Pin PLCC	0°C to +70°C

General Description:

The TC7126A is a 3-1/2 digit CMOS Analog-to-Digital Converter (ADC) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, digit and polarity drivers, voltage reference, and clock circuit are integrated on-chip. The TC7126A directly drives a Liquid Crystal Display (LCD), and includes a backplane driver.

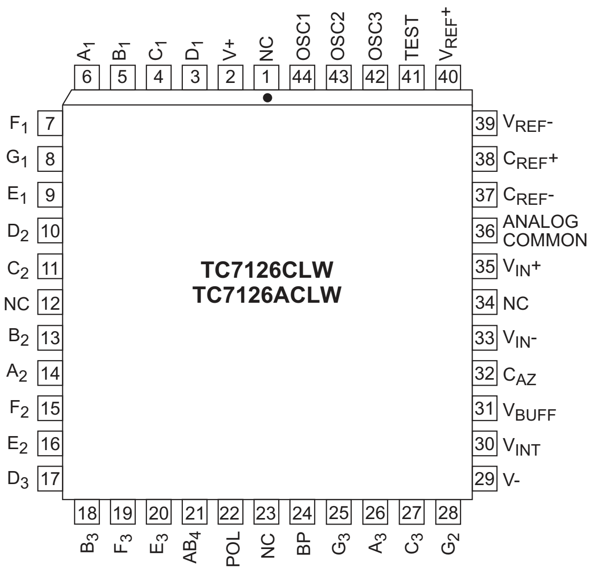
A low-cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TC7126A's extremely low-power drain and 9V battery operation make it ideal for portable applications.

The TC7126A reduces linearity error to less than 1 count. Rollover error (the difference in readings for equal magnitude, but opposite polarity input signals) is below ±1 count. High-impedance differential inputs offer 1pA leakage current and a $10^{12}\Omega$ input impedance. The 15µV_{P-P} noise performance ensures a "rock solid" reading, and the auto-zero cycle ensures a zero display reading with a 0V input.

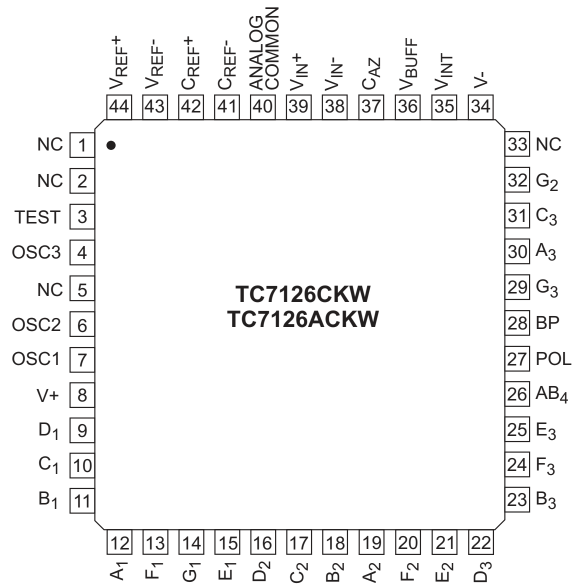
The TC7126A features a precision, low drift internal voltage reference and is functionally identical to the TC7126. A low drift external reference is not normally required with the TC7126A.

Package Type

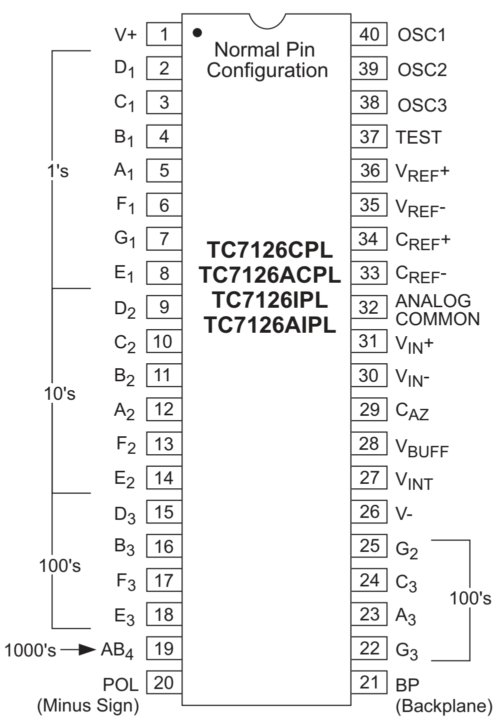
44-Pin PLCC



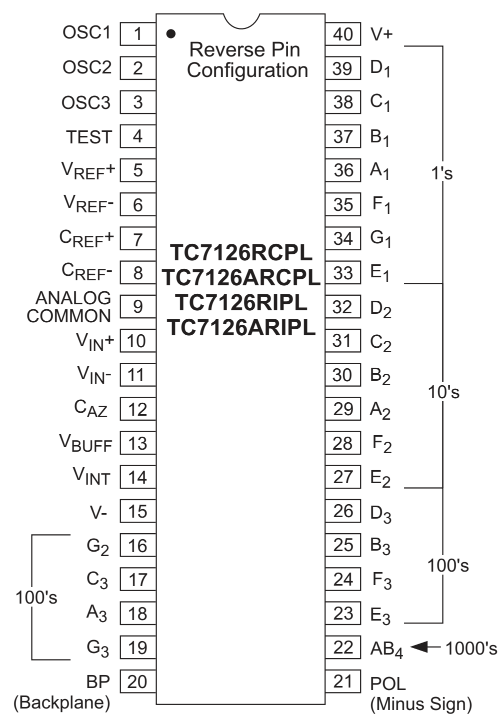
44-Pin PQFP



40-Pin PDIP (Normal)

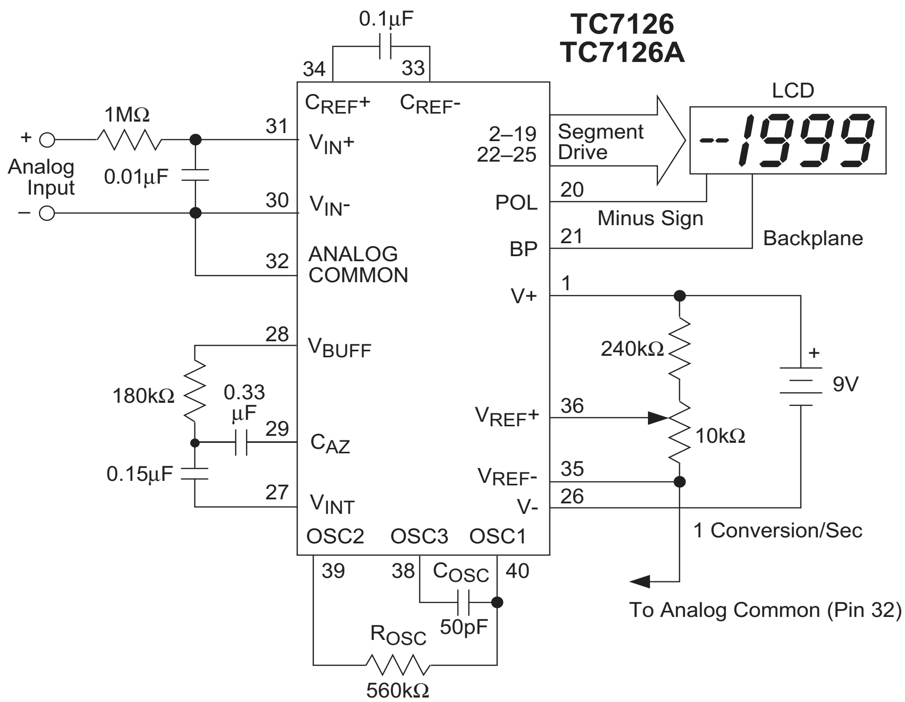


44-Pin PDIP (Reverse)



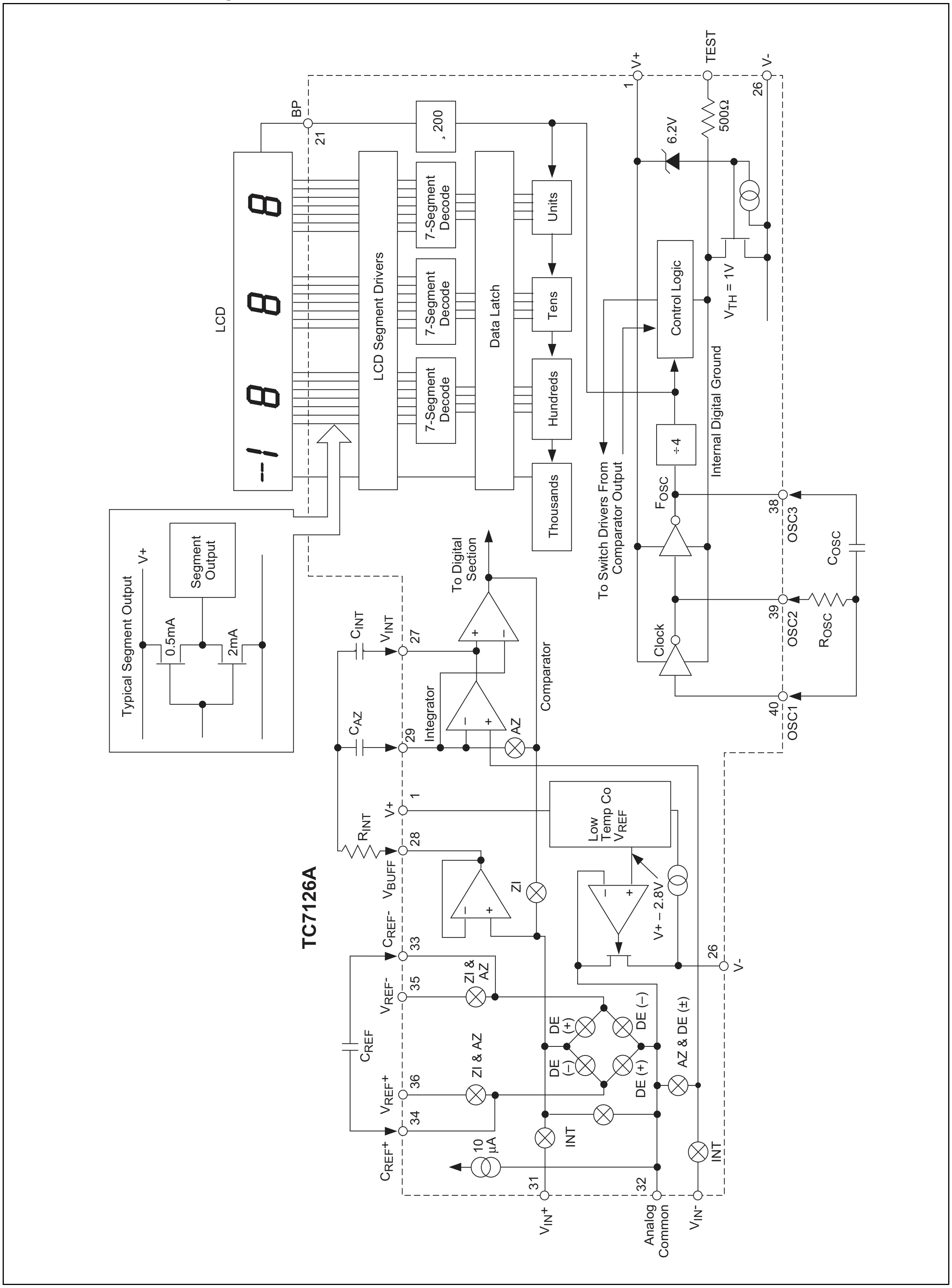
NC = No Internal Connection

Typical Application



Note: Pin numbers refer to 40-pin DIP.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V+ to V-) 15V
Analog Input Voltage (either Input) **(Note 1)** ... V+ to V-
Reference Input Voltage (either Input) .... V+ to V-
Clock Input .... Test to V+
Package Power Dissipation ($T_A \leq 70°C$) **(Note 2)**:

- 44-Pin PQFP 1.00W
- 40-Pin PLCC 1.23W
- 44-Pin PDIP 1.23W

Operating Temperature Range:

- C (Commercial) Devices .... 0°C to +70°C
- I (Industrial) Devices .... -25°C to +85°C

Storage Temperature Range .... -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: TC7126/A ELECTRICAL SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Electrical Characteristics: V_S = +9V, f_{CLK} – 16kHz, and T_A = +25°C, unless otherwise noted.						
Input						
Z_{IR}	Zero Input Reading	-000.0	±000.0	+000.0	Digital Reading	V_{IN} = 0V Full Scale = 200mV
Z_{RD}	Zero Reading Drift	—	0.2	1	μV/°C	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C
	Ratiometric Reading	999	999/1000	1000	Digital Reading	V_{IN} = V_{REF}, V_{REF} = 100mV
NL	Linearity Error	-1	±0.2	1	Count	Full Scale = 200mV or 2V Max Deviation From Best Fit Straight Line
	Rollover Error	-1	±0.2	1	Count	V_{IN}- = V_{IN}+ ≈ 200mV
e_N	Noise	—	15	—	μV_{P-P}	V_{IN} = 0V, Full Scale = 200mV
I_L	Input Leakage Current	—	1	10	pA	V_{IN} = 0V
CMRR	Common Mode Rejection Ratio	—	50	—	μV/V	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200mV
	Scale Factor Temperature Coefficient	—	1	5	ppm/°C	V_{IN} = 199mV, 0°C ≤ T_A ≤ +70°C Ext. Ref. Temp Coeff. = 0ppm/°C
Analog Common						
V_{CTC}	Analog Common Temperature Coefficient	—	—	—	—	250kΩ Between Common and V+
		—	—	—	—	0°C ≤ T_A ≤ +70°C ("C" Devices)
		—	80	—	ppm/°C	TC7126
		—	35	75	ppm/°C	TC7126A
		—	35	100	ppm/°C	-25°C ≤ T_A ≤ +85°C ("I" Device) (TC7126A)

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3: Refer to "Differential Input" discussion.
4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
5: See "Typical Application".
6: During Auto-Zero phase, current is 10-20μA higher. A 48kHz oscillator increases current by 8μA (Typical). Common current is not included.

TABLE 1-1: TC7126/A ELECTRICAL SPECIFICATIONS (CONTINUED)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Electrical Characteristics: V_S = +9V, f_{CLK} – 16kHz, and T_A = +25°C, unless otherwise noted.						
V_C	Analog Common Voltage	2.7	3.05	3.35	V	250kΩ Between Common and V+
LCD Drive						
V_{SD}	LCD Segment Drive Voltage	4	5	6	V_{P-P}	V+ to V- = 9V
V_{BD}	LCD Backplane Drive Voltage	4	5	6	V_{P-P}	V+ to V- = 9V
Power Supply						
I_S	Power Supply Current	—	55	100	μA	V_{IN} = 0V, V+ to V- = 9V **(Note 6)**

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3: Refer to “Differential Input” discussion.
4: Backplane drive is in phase with segment drive for “OFF” segment, 180° out of phase for “ON” segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
5: See “Typical Application”.
6: During Auto-Zero phase, current is 10-20μA higher. A 48kHz oscillator increases current by 8μA (Typical). Common current is not included.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (40-Pin PDIP) Normal	(Reversed)	Symbol	Description
1	(40)	V+	Positive supply voltage.
2	(39)	D_1	Activates the D section of the units display.
3	(38)	C_1	Activates the C section of the units display.
4	(37)	B_1	Activates the B section of the units display.
5	(36)	A_1	Activates the A section of the units display.
6	(35)	F_1	Activates the F section of the units display.
7	(34)	G_1	Activates the G section of the units display.
8	(33)	E_1	Activates the E section of the units display.
9	(32)	D_2	Activates the D section of the tens display.
10	(31)	C_2	Activates the C section of the tens display.
11	(30)	B_2	Activates the B section of the tens display.
12	(29)	A_2	Activates the A section of the tens display.
13	(28)	F_2	Activates the F section of the tens display.
14	(27)	E_2	Activates the E section of the tens display.
15	(26)	D_3	Activates the D section of the hundreds display.
16	(25)	B_3	Activates the B section of the hundreds display.
17	(24)	F_3	Activates the F section of the hundreds display.
18	(23)	E_3	Activates the E section of the hundreds display.
19	(22)	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP	LCD Backplane drive output (TC7106A). Digital Ground (TC7107A).
22	(19)	G_3	Activates the G section of the hundreds display.
23	(18)	A_3	Activates the A section of the hundreds display.
24	(17)	C_3	Activates the C section of the hundreds display.
25	(16)	G_2	Activates the G section of the tens display.
26	(15)	V-	Negative power supply voltage.
27	(14)	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance buildup will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047µF capacitor may be used. The capacitor must have a low dielectric constant to prevent rollover errors. See **Section 6.3 "Integrating Capacitor (CINT)"**, Integrating Capacitor for additional details.
28	(13)	V_{BUFF}	Integration resistor connection. Use a 180kΩ resistor for a 200mV full-scale range and a 1.8MΩ resistor for a 2V full scale range.
29	(12)	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.33µF capacitor for 200mV full scale, and a 0.033µF capacitor for 2V full scale. See **Section 6.1 "Auto-Zero Capacitor (CAZ)"**, Auto-Zero Capacitor for additional details.
30	(11)	V_{IN}-	The analog LOW input is connected to this pin.
31	(10)	V_{IN}+	The analog HIGH input signal is connected to this pin.
32	(9)	ANALOG COMMON	This pin is primarily used to set the Analog Common mode voltage for battery operation, or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See **Section 7.3 "Analog Common (Pin 32)"**, Analog Common for additional details.
33	(8)	C_{REF}-	See Pin 34.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (40-Pin PDIP) Normal	(Reversed)	Symbol	Description
34	(7)	$C_{REF}+$	A 0.1μF capacitor is used in most applications. If a large Common mode voltage exists (for example, the V_{IN}- pin is not at analog common) and a 200mV scale is used, a 1μF capacitor is recommended and will hold the rollover error to 0.5 count.
35	(6)	$V_{REF}-$	See Pin 36.
36	(5)	$V_{REF}+$	The analog input required to generate a full scale output (1999 counts). Place 100mV between Pins 35 and 36 for 199.9mV full scale. Place 1V between Pins 35 and 36 for 2V full scale. See **Section 6.6 "Reference Voltage Selection"**, Reference Voltage for additional information.
37	(4)	TEST	Lamp test. When pulled HIGH (to V+), all segments will be turned on and the display should read `-1888`. It may also be used as a negative supply for externally generated decimal points. See **Section 7.4 "TEST (Pin 37)"**, TEST for additional information.
38	(3)	OSC3	See Pin 40.
39	(2)	OSC2	See Pin 40.
40	(1)	OSC1	Pins 40, 39 and 38 make up the oscillator section. For a 48kHz clock (3 readings, 39 per second), connect Pin 40 to the junction of a 180kΩ resistor and a 50pF capacitor. The 180kΩ resistor is tied to Pin 39 and the 50pF capacitor is tied to Pin 38.

3.0 DETAILED DESCRIPTION

(All Pin Designations Refer to 40-Pin PDIP.)

3.1 Dual Slope Conversion Principles

The TC7126A is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TC7126/A operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (De-integration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}) (see Figure).

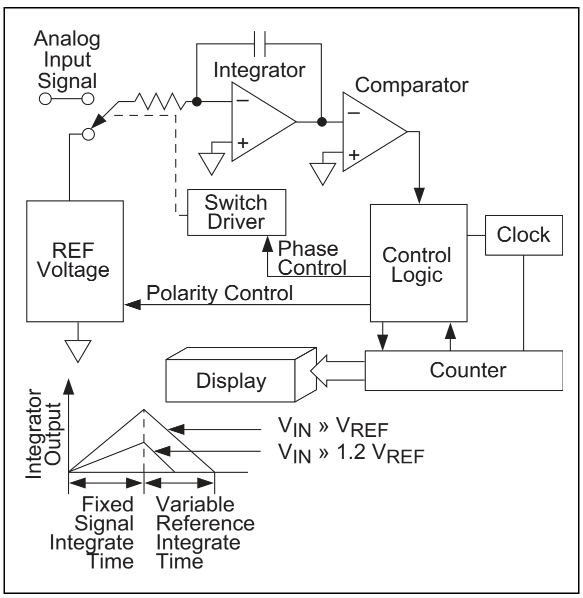


FIGURE 3-1: *Basic Dual Slope Converter*

In a simple dual slope converter, a complete conversion requires the integrator output to “ramp-up” and “ramp-down.”

A simple mathematical equation relates the input signal, reference voltage and integration time:

EQUATION 3-1:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)d_t = \frac{V_R T_{RI}}{RC}$$

Where:

V_R = Reference voltage

T_{SI} = Signal integration time (fixed)

T_{RI} = Reference voltage integration time (variable)

For a constant V_{IN}:

EQUATION 3-2:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated or averaged to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50Hz/60Hz power line period (see Figure 3-2).

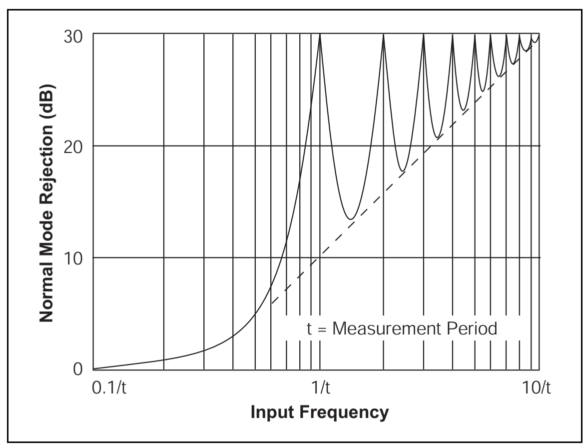


FIGURE 3-2: *Normal Mode Rejection of Dual Slope Converter*

4.0 ANALOG SECTION

In addition to the basic integrate and de-integrate dual slope cycles discussed above, the TC7126A design incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three phases:

1. Auto-Zero phase
2. Signal Integrate phase
3. Reference Integrate phase

4.1 Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically 10µV to 15µV. The auto-zero cycle length is 1000 to 3000 clock periods.

4.2 Signal Integrate Phase

The auto-zero loop is entered and the internal differential inputs connect to $V_{IN}+$ and $V_{IN}-$. The differential input signal is integrated for a fixed time period. The TC7126/A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

EQUATION 4-1:

$$T_{SI} = \frac{4}{F_{OSC}} \times 1000$$

Where: F_{OSC} = external clock frequency.

The differential input voltage must be within the device Common mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, $V_{IN}-$ should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

4.3 Reference Integrate Phase

The third phase is reference integrate or de-integrate. $V_{IN}-$ is internally connected to analog common and $V_{IN}+$ is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

EQUATION 4-2:

$$1000 \frac{V_{IN}}{V_{REF}}$$

5.0 DIGITAL SECTION

The TC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD, including an LCD backplane driver. The backplane frequency is the external clock frequency divided by 800. For 3 conversions per second, the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal, the segment is OFF. An out of phase segment drive signal causes the segment to be ON (visible). This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is ON for negative analog inputs. If $V_{IN}+$ and $V_{IN}-$ are reversed, this indicator reverses.

On the TC7126A, when the TEST pin is pulled to V+, all segments are turned ON and the display reads -1888. During this mode, LCD segments have a constant DC voltage impressed.

Note:	Do not leave the display in this mode for more than several minutes. LCDs may be destroyed if operated with DC levels for extended periods.

The display font and segment drive assignment are shown in Figure 5-1.

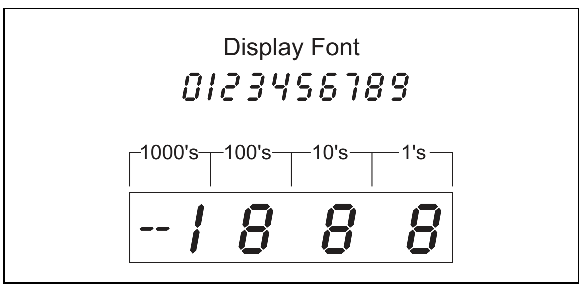


FIGURE 5-1: *Display Font and Segment Assignment*

5.1 System Timing

The oscillator frequency is divided by four prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts (16,000 clock pulses). The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

1. Auto-Zero Phase: 1000 to 3000 counts (4000 to 12,000 clock pulses).

   For signals less than full scale, the auto-zero phase is assigned the unused reference integrate time period.

2. Signal Integrate: 1000 counts (4000 clock pulses).

   This time period is fixed. The integration period is:

EQUATION 5-1:

$$T_{SI} = 4000 \frac{1}{F_{OSC}}$$

Where: F_{OSC} is the externally set clock frequency.

3. Reference Integrate: 0 to 2000 counts (0 to 8000 clock pulses).

The TC7126A is a drop-in replacement for the TC7126 and ICL7126, which offer a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

6.0 COMPONENT VALUE SELECTION

6.1 Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A 0.47µF capacitor is recommended for 200mV full scale applications where 1LSB is 100µV. A 0.033µF capacitor is adequate for 2.0V full scale applications. A mylar type dielectric capacitor is adequate.

6.2 Reference Voltage Capacitor (C_{REF})

The reference voltage, used to ramp the integrator output voltage back to zero during the reference integrate phase, is stored on C_{REF}. A 0.1µF capacitor is acceptable when V_{REF}- is tied to analog common. If a large Common mode voltage exists (V_{REF}- – analog common) and the application requires a 200mV full scale, increase C_{REF} to 1µF. Rollover error will be held to less than 0.5 count. A Mylar type dielectric capacitor is adequate.

6.3 Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TC7126A's superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case, a ±2V full scale integrator output swing is satisfactory. For 3 readings per second (F_{OSC} = 48kHz), a 0.047µF value is suggested. For 1 reading per second, 0.15µF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

EQUATION 6-1:

$$C_{INT} = \frac{(4000)\left(\frac{1}{F_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

F_{OSC} = Clock frequency at Pin 38

V_{FS} = Full scale input voltage

R_{INT} = Integrating resistor

V_{INT} = Desired full scale integrator output swing

At 3 readings per second, a 750Ω resistor should be placed in series with C_{INT}. This increases accuracy by compensating for comparator delay. C_{INT} must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

6.4 Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6µA. The integrator and buffer can supply 1µA drive current with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200mV full scale, R_{INT} is 180kΩ. A 2V full scale requires 1.8MΩ.

Component Value	Nominal Full Scale Voltage	
	200mV	2V
C_{AZ}	0.33µF	0.033µF
R_{INT}	180kΩ	1.8MΩ
C_{INT}	0.047µF	0.047µF

Note: F_{OSC} = 48kHz (3 readings per sec).

6.5 Oscillator Components

C_{OSC} should be 50pF; R_{OSC} is selected from the equation:

EQUATION 6-2:

$$F_{OSC} = \frac{0.45}{RC}$$

For a 48kHz clock (3 conversions per second), R = 180kΩ.

Note that F_{OSC} is 44 to generate the TC7126A's internal clock. The backplane drive signal is derived by dividing F_{OSC} by 800.

To achieve maximum rejection of 60Hz noise pickup, the signal integrate period should be a multiple of 60Hz. Oscillator frequencies of 24kHz, 12kHz, 80kHz, 60kHz, 40kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 20kHz, 100kHz, 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings per second) will reject both 50Hz and 60Hz.

6.6 Reference Voltage Selection

A full scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full Scale Voltage*	V_{REF}
20mV	100mV
2V	1V

Note: $V_{FS} = 2V_{REF}$.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000lb/in^2 is 400mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

The differential reference can also be used where a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}-. The transducer output is connected between V_{IN}+ and analog common.

7.0 DEVICE PIN FUNCTIONAL DESCRIPTION

(Pin Numbers Refer to the 40-Pin PDIP.)

7.1 Differential Signal Inputs V_{IN}+ (Pin 31), V_{IN}- (Pin 30)

The TC7126A is designed with true differential inputs and accepts input signals within the input stage Common mode voltage range (V_{CM}). Typical range is V+ – 1V to V- + 1V. Common mode voltages are removed from the system when the TC7126A operates from a battery or floating power source (isolated from measured system), and V_{IN}- is connected to analog common (V_{COM}) (see Figure 7-2).

In systems where Common mode voltages exist, the TC7126A's 86 dB Common mode rejection ratio minimizes error. Common mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 7-1). For such applications, the integrator output swing can be reduced below the recommended 2V full scale swing. The integrator output will swing within 0.3V of V+ or V- without increased linearity error.

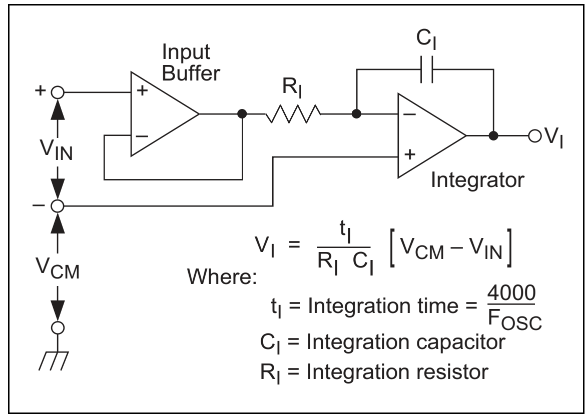


FIGURE 7-1: *Common Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)*

7.2 Differential Reference V_{REF}+ (Pin 36), V_{REF}- (Pin 35)

The reference voltage can be generated anywhere within the V+ to V- power supply range.

To prevent rollover type errors being induced by large Common mode voltages, C_{REF} should be large compared to stray node capacitance.

The TC7126A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage, suitable for use as a reference. The temperature coefficient of analog common is typically 35ppm/°C for the TC7126A and 80 ppm/°C for the TC7126.

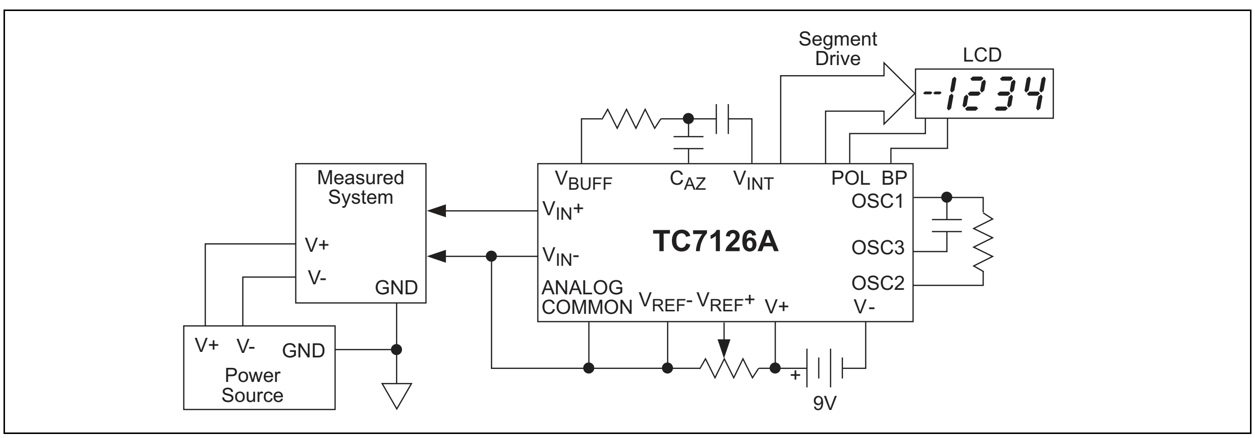


FIGURE 7-2: *Common Mode Voltage Removed in Battery Operation with V_{IN} = Analog Common*

7.3 Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3V below V+. The potential is between 2.7V and 3.35V below V+. Analog common is tied internally to an N-channel FET capable of sinking 100μA. This FET will hold the common line at 3V should an external load attempt to pull the common line toward V+. Analog common source current is limited to 1μA. Therefore, analog common is easily pulled to a more negative voltage (i.e., below V+ – 3V).

The TC7126A connects the internal V_{IN}+ and V_{IN}- inputs to analog common during the auto-zero phase. During the reference integrate phase, V_{IN}- is connected to analog common. If V_{IN}- is not externally connected to analog common, a Common mode voltage exists, but is rejected by the converter's 86dB Common mode rejection ratio. In battery operation, analog common and V_{IN}- are usually connected, removing Common mode voltage concerns. In systems where V_{IN}- is connected to power supply ground or to a given voltage, analog common should be connected to V_{IN}-.

The analog common pin serves to set the analog section reference, or common point. The TC7126A is specifically designed to operate from a battery, or in any measurement system where input signals are not referenced (float) with respect to the TC7126A's power source. The analog common potential of V+ – 3V gives a 7V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15Ω output impedance.

With sufficiently high total supply voltage (V+ – V- > 7V), analog common is a very stable potential with excellent temperature stability (typically 35ppm/°C). This potential can be used to generate the TC7126A's reference voltage. An external voltage reference will be unnecessary in most cases because of the 35ppm/°C temperature coefficient. See **Section 7.5 "TC7126A Internal Voltage Reference"**, TC7126A Internal Voltage Reference discussion.

7.4 TEST (Pin 37)

The TEST pin potential is 5V less than V+. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally generated negative logic supply through a 500Ω resistor. The TEST pin load should be no more than 1mA. See **Section 5.0 "DIGITAL SECTION"**, Digital Section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled HIGH (to V+), all segments plus the minus sign will be activated. DO NOT OPERATE IN THIS MODE FOR MORE THAN SEVERAL MINUTES. With TEST = V+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

7.5 TC7126A Internal Voltage Reference

The TC7126A's analog common voltage temperature stability has been significantly improved (Figure 7-3). The "A" version of the industry standard TC7126 device allows users to upgrade old systems and design new systems, without external voltage references. External R and C values do not need to be changed. Figure 7-4 shows analog common supplying the necessary voltage reference for the TC7126A.

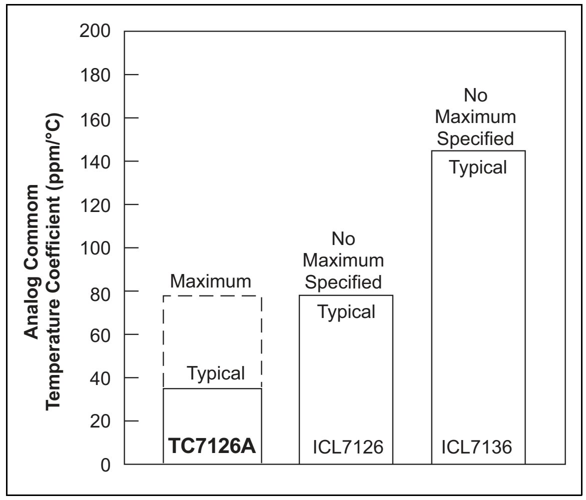


FIGURE 7-3: Analog Common Temp. Coefficient

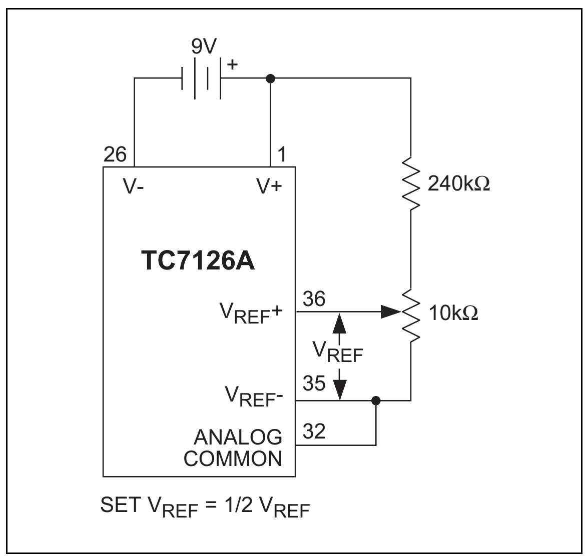


FIGURE 7-4: TC7126A Internal Voltage Reference Connection

8.0 TYPICAL APPLICATIONS

8.1 Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7126A, 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr. Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	720 Palomar Ave. Sunnyvale, CA 94086 408-523-8200	FE 0801 FE 0203
VGI, Inc.	1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St. Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

Note: Contact LCD manufacturer for full product listing/specifications.

8.2 Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added, without adding an additional supply. No more than 1mA should be supplied by the TEST pin; its potential is approximately 5V below V+ (see Figure).

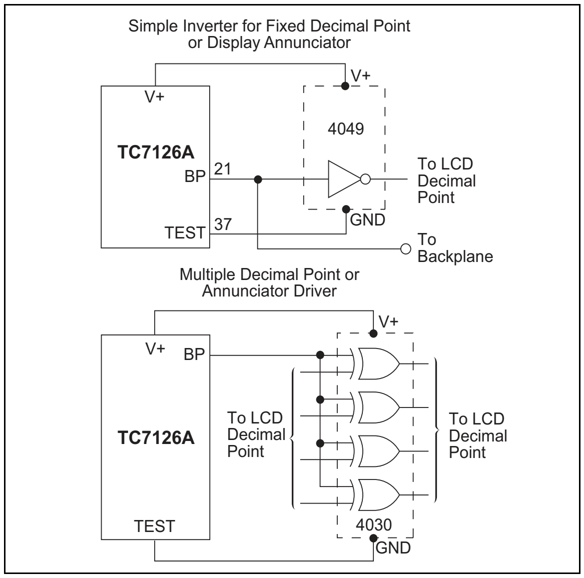


FIGURE 8-1: Decimal Point and Annunciator Drives

8.3 Flat Package

The TC7126 is available in an epoxy 64-pin formed lead package. A test socket for the TC7126ACBQ device is available:

Part Number:	IC 51-42
Manufacturer:	Yamaichi
Distribution:	Nepenthe Distribution 2471 East Bayshore, Ste. 520 Palo Alto, CA 94043 (650) 856-9332

8.4 Ratiometric Resistance Measurements

The TC7126A's true differential input and differential reference make ratiometric reading possible. In a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor is applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

EQUATION 8-1:

$$\text{Displayed (Reading)} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000$$

The display will over range for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$ (see Figure 8-2).

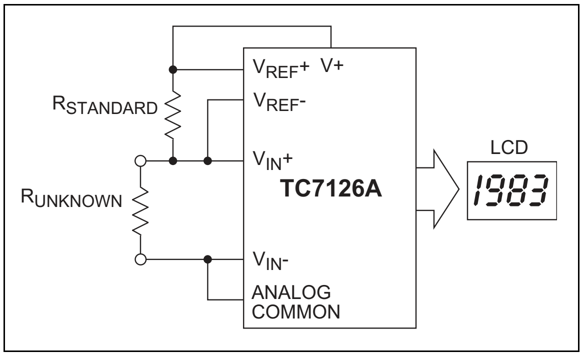


FIGURE 8-2: *Low Parts Count Ratiometric Resistance Measurement*

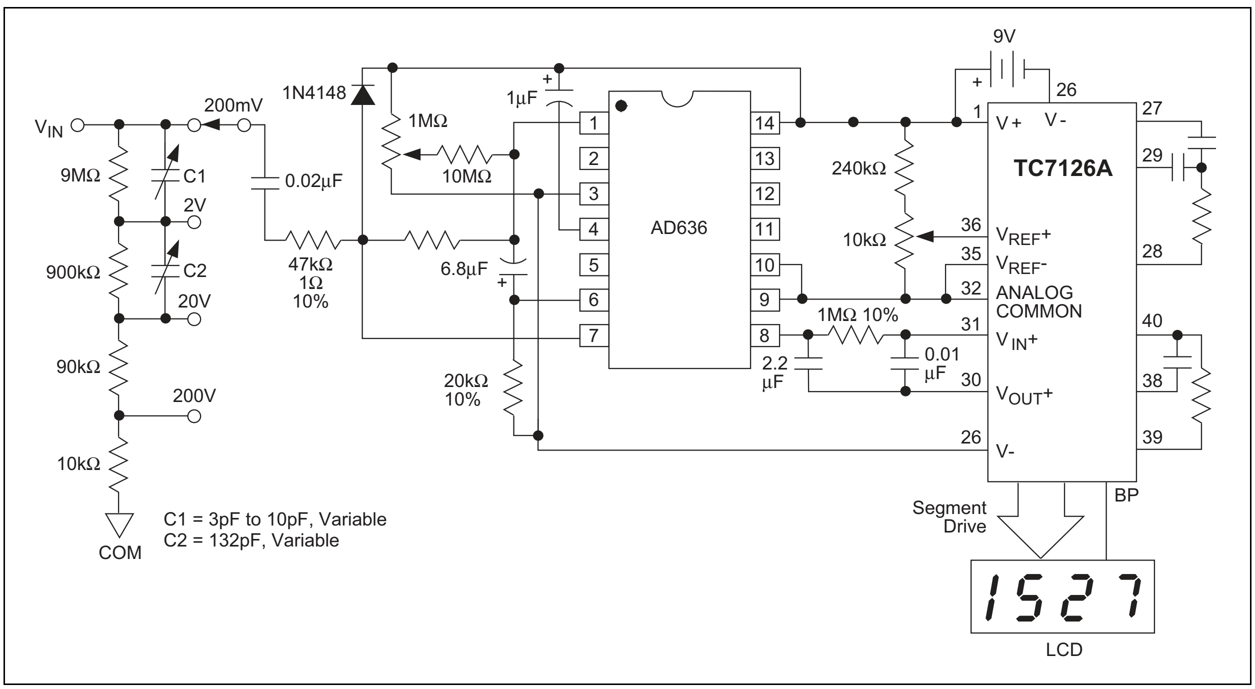


FIGURE 8-3: *3-1/2 Digit True RMS AC DMM*

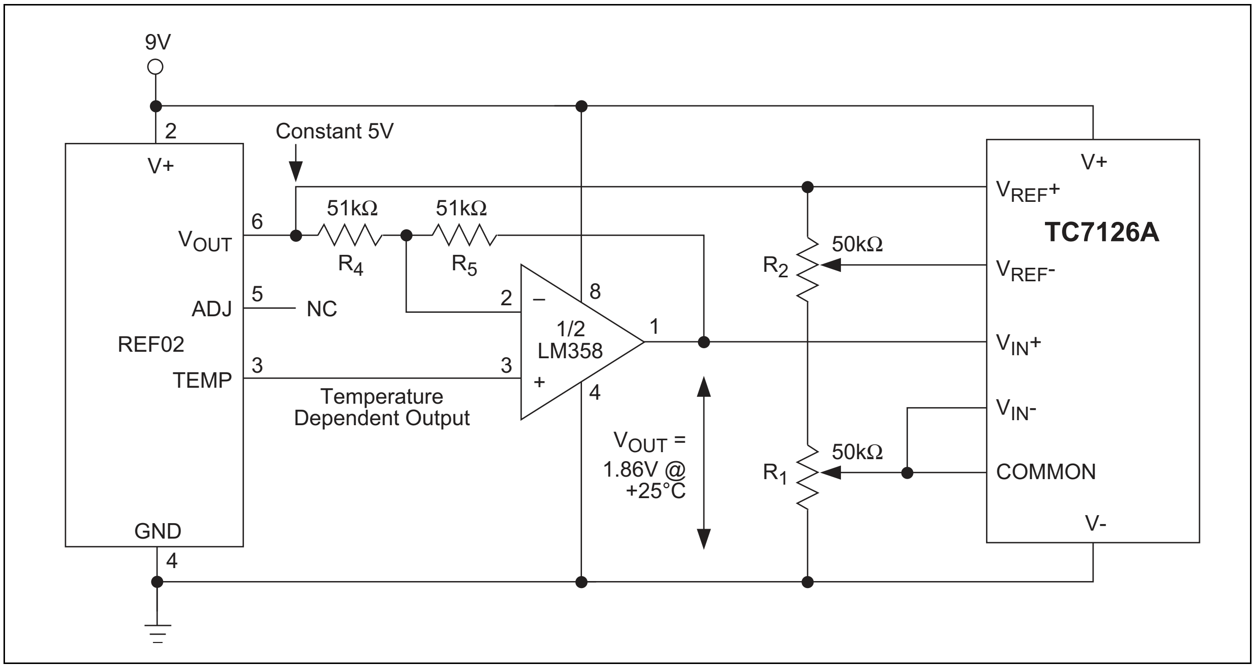


FIGURE 8-4: *Integrated Circuit Temperature Sensor*

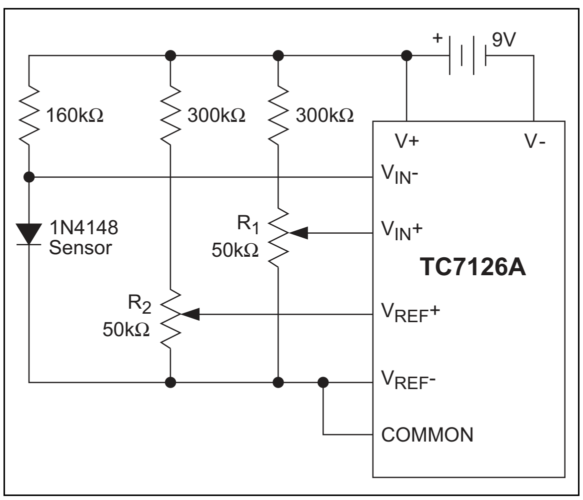


FIGURE 8-5: *Temperature Sensor*

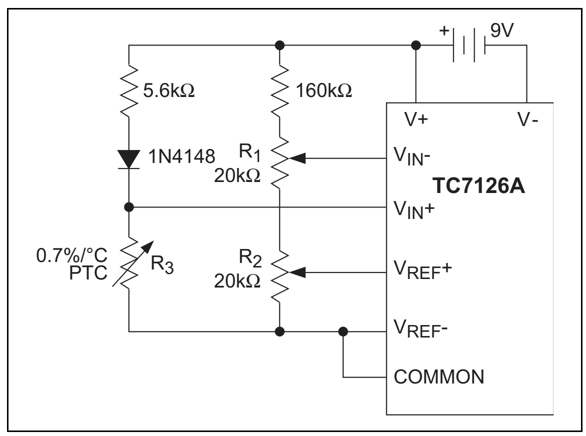


FIGURE 8-6: *Positive Temperature Coefficient Resistor Temperature Sensor*

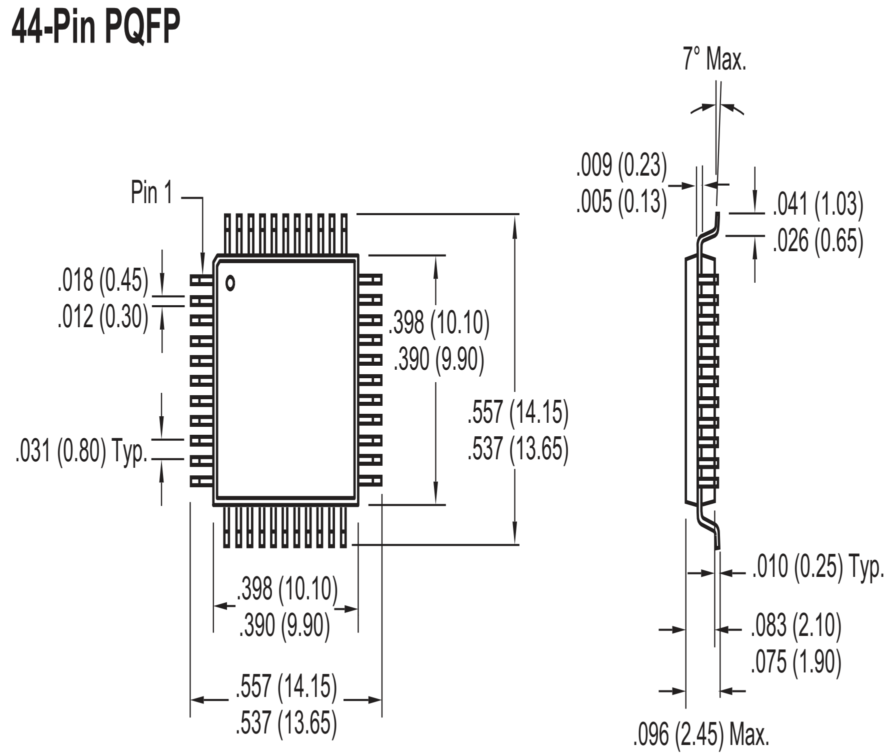
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

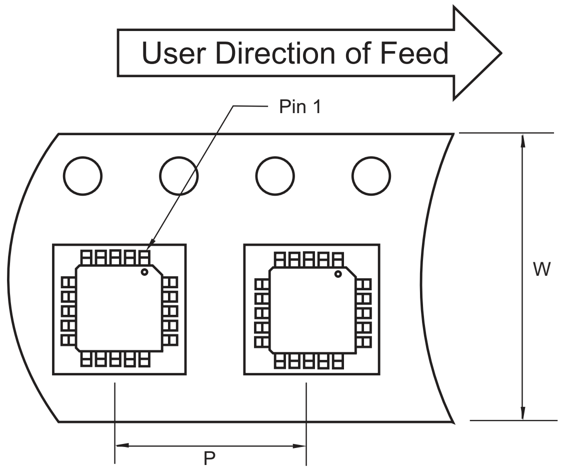
Package marking data not available at this time.

9.2 Taping Form

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Component Taping Orientation for 44-Pin PQFP Devices



Carrier Tape, Number of Components Per Reel and Reel Size

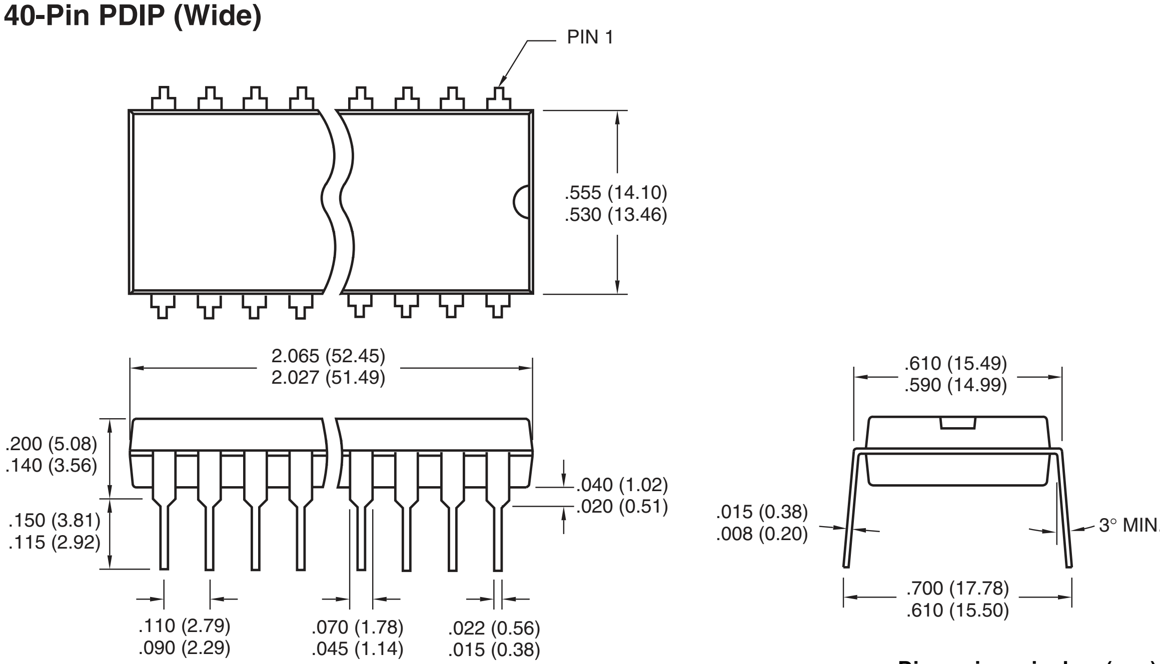
Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PQFP	24 mm	16 mm	500	13 in

Note: Drawing does not represent total number of pins.

9.3 Package Dimensions

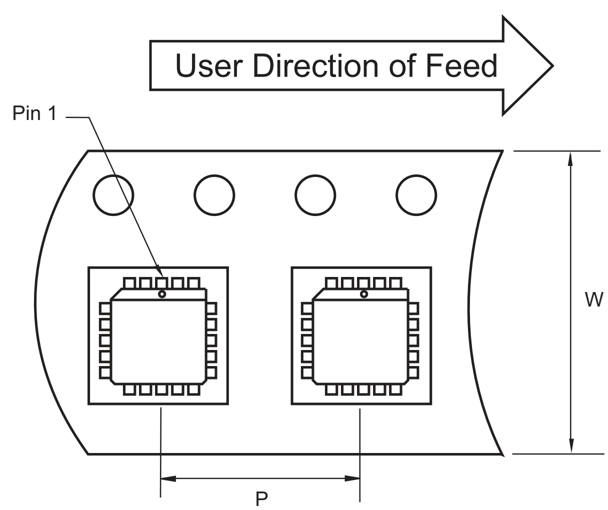
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

40-Pin PDIP (Wide)



Dimensions: inches (mm)

Component Taping Orientation for 44-Pin PLCC Devices



Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PLCC	32 mm	24 mm	500	13 in

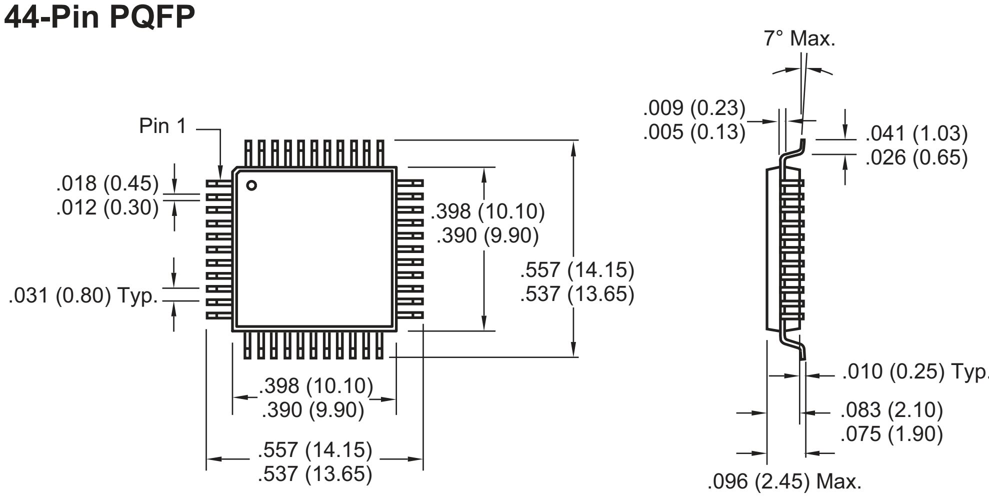
Note: Drawing does not represent total number of pins.

Dimensions: inches (mm)

9.4 Package Dimensions (Continued)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

44-Pin PQFP



Dimensions: inches (mm)

10.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART CODE **TC7126X X XXX**

A or blank*

R (reversed pins) or blank (CPL pkg only)

* "A" parts have an improved reference TC

Package Code (see Device Selection Table)

NOTES:

Note the following details of the code protection feature on Microchip devices:

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