Technical Data

MC44CD02 Version 3.3
27 APR 2006

MC44CD02 Wideband Zero-IF Direct Conversion Receiver

freescale semiconductor

MC44CD02

QFN48-EP Package

Single Chip Wideband Zero-IF Direct Conversion Receiver Front-End IC for Hand Held Portable Convergence Terminals

Ordering Information

Device	Temp Range	Package
MC44CD02FC,R2	-30°C to +85°C	QFN48
NOTE: For tape and reel, add R2 suffix.		

MC44CD02 Data Sheet
Version 3.3

Original Release Date: 18 OCT 2004
Revised: 27 APR 2006

WMSG
EMEA Radio Product Division
Freescale, Inc.

Revision History

Version Number	Revision Date	Description of Changes	
1.0	12/15/2004	Initial version.	
2.0	10/03/2005	Major revision (filtering, WBD, packaging, clock, LOP, I2C)	All pages
3.0	11/28/2005	All sections: typos and general comments updated First public release	All pages
3.1	12/06/2005	Added marking and shipping informations	p 79
3.2	01/19/2006	Corrected typo on pin#31/37 Corrected typo on startup time typical value (parameter 1.7) Modified LO leakage parameter 2.6 in table A.4 into parameter 3.15 in table A.5 Correction of table 4-6 (120k and 470k swapped) Added explanations on how to use the bit PADCTRL (2 write operations required) Changed marking specification (no more DVB-H logo)	All pages
3.3	04/27/2006	Changed parameter 8.2 (LVDS common voltage) Detailed conditions for WBD calibration Added parameter type 5.51 in table A-12 Added parameter type from 8.8 to 8.15 in table A-14	p 73 p 39 p 71 p 73,74

Table Of Content

Section 1 Introduction

1.1 Overview

The MC44CD02 is a Single Chip Wideband Zero-IF Direct Conversion Receiver Front-End IC intended to be associated with an IQ baseband OFDM demodulator and an external LNA (see **Figure 1-1**).

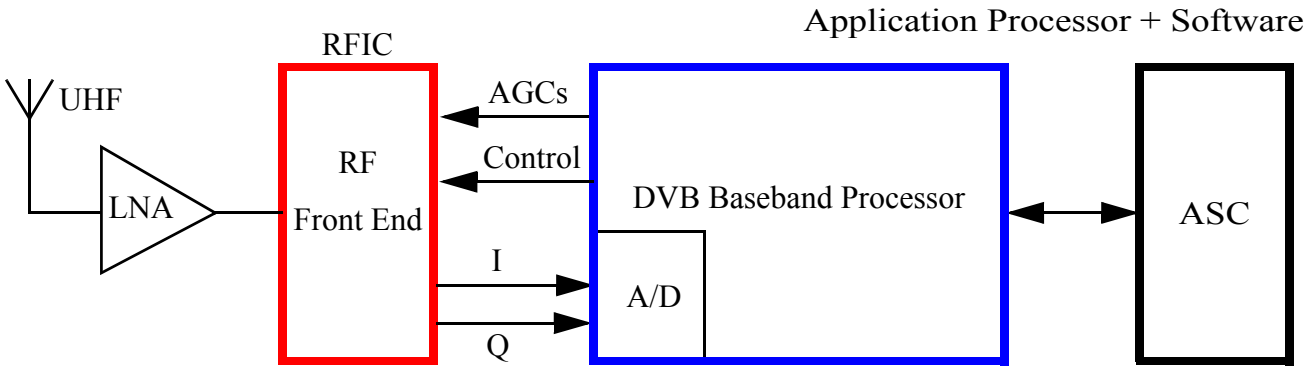

Figure 1-1 Block Diagram of a DVB-H chipset

The MC44CD02 chip is targeted for terminals dedicated in Integrated Cellular Phones (Category 3 for Hand Held Portable Convergence Terminals). This category is described in the EICTA-TAC-MBRAI RF Specification (reference [1]), and exhibits the following attributes:

- Both cellular and DVB-H radios integrated in the terminal.
- Battery powered.
- Moved during reception.
- Low gain integrated antenna.

The system is based on DVB-H standard and shall be capable of correctly demodulating all modes specified in the EN 300 744 specification (reference [2]), except the code rates 5/6 and 7/8.

The MC44CD02 covers the UHF bands IV and V (470-862MHz) and is able to handle 6, 7 or 8 MHz bandwidth channels in this range.

This device is targeted to provide an optimum solution where the power consumption is the major constraint for small battery operated devices.

It is designed using the CDR1BiGCMOS process with the SiGe (HBT) option and electroplated copper inductors.

The MC44CD02 is available in a Lead-free 48 pin QFN package.

1.2 Glossary

AAF
Baseband Anti Aliasing Filter.

ASC
Application Specific Controller, an external processor in charge of computing complex functions in the DVB-H system.

MC44CD02
The code name of the DVB-H RF front-end chip.

DVB-H
Digital Video Broadcast system, optimized for handheld applications. This category is described in the EICTA-TAC-MBRAI RF Specifications.

Deep-Sleep Mode
An operating mode characterized by the ENABLE pin held low leading to a power consumption reduced to a minimum.

EICTA-TAC
European Information, Communications and Consumer Electronics Industry Technology Association Result of the merge of EICTA (European Information and Communications Technology Industry Association and EACEM (European Association of Consumer Electronics Manufacturers).

I2C
Inter IC bus, a bidirectional, serial data transfer protocol.

LPF
Baseband filter sub-module. The filter in charge of providing the I and Q components to the baseband processor during receive.

LVDS
Low Voltage Differential Signaling. LVDS is targeted for general purpose high speed applications requiring very low noise. This technology is defined by the ANSI/TIA/EIA-644 industry standard.

MBRAI
Mobile and Portable DVB-T Radio Access Interface Specification.

MIXER
The I and Q mixer sub-module.

MLP
The Multi-Level pin sub-module is dedicated to the configuration of the chip with regards to the reference clock frequency and the clock output signal shaping.

Normal Mode
An operating mode characterized by the ENABLE pin set, the SCAN_MODE pin cleared and the TSTM bit cleared in the MODE register (address $00).

OFDM
Orthogonal Frequency Division Multiplexing.

OSC
The 36MHz or 26MHz crystal oscillator sub-module.

PLL
Phase Locked Loop sub-module.

PMA
Post Mixer Amplifier sub-module.

Power Down Mode
An operating mode characterized by the ENABLE pin set, the SCAN_MODE pin cleared, the TSTM bit cleared and the PDM bit set in the MODE register (address $00).

RCI
The Radio Control Interface sub-module.

REM
Reference Management (bias support) sub -module. The block in charge of delivering current/voltage references to the rest of the chip

RFLNA
RF Low Noise Amplifier sub-module.

WBD
Wide Band Detector sub-module, providing an estimation of the total power present in the UHF band.

1.3 Features

The MC44CD02 is a Wide Band Zero-IF Direct Conversion Receiver Front-End IC. It receives the RF signal from an associated external LNA that provides a typical gain of about 10dB. Furthermore, this external LNA and its matching network will exhibit a total noise figure NF of 3.5dB maximum. The MC44CD02 provides I and Q terms to the associated baseband demodulator. The device is controlled through an I2C bus and provides interface signals to the baseband processor (RF wide band detector, reference clock). In addition, the MC44CD02 receives control signals for specific functions or features such as the internal LNA and baseband AGC controls.

The device exhibits the following features:

- Low power operation (2.775V, 98mA current drain, i.e. 270mW in normal mode)
- Power down and deep sleep battery saving modes of operation
- Full UHF range operation (470 to 862MHz)
- Multi standard RF operation (6, 7 and 8MHz bandwidth channels)
- Low external components count
- I2C bus controlled
- Integrated low phase noise PLL with 4GHz VCO and quadrature generator for precise I and Q local oscillator generation
- 166.67kHz synthesizer step size
- Integrated RF low noise amplifier (LNA) with gain control and differential inputs
- Integrated balanced I and Q down mixers
- Integrated post mixer amplifiers (PMA)
- Integrated I and Q baseband 8th order inverse Chebyshev low pass filters and amplifiers with gain controlIntegrated I and Q baseband 4th order Butterworth anti-aliasing (AAF) filter, with 6MHz 3dB cut-off frequency.Integrated filter tracking loop to cover the 6, 7 and 8MHz channel bandwidths, the AAF filter, and all process variations
- Integrated wide band RF power detector with output signal to the baseband demodulator
- 36MHz or 26MHz crystal oscillator with clock outputs (either custom LVDS or single-ended) toward the baseband demodulator
- A general purpose digital output which can possibly be used to control the gain of an external low noise amplifier
- Lead free QFN48 7x7, 0.5mm pitch exposed pad package

1.4 Modes of Operation

This circuit supports three modes of operation.

- Normal - The device operates normally.
- Power Down - The device is turned OFF except for the crystal oscillator and associated reference clock buffers which are kept active. The integrated superfilter providing the supply to the VCO is also kept ON for PLL start-up purposes.
- Deep Sleep - The device is fully disabled and the power consumption is reduced to a minimum.

1.5 Block Diagram

Following depicts the block diagram of the MC44CD02 chip and several external components. The receive path starts with an external LNA located very close to the UHF antenna which can also be equipped with a filter in charge for example to block the GSM interferers. Possibly the external LNA exhibits a switchable gain under control of the LOP pin. A UHF balun in charge of the single-ended to differential conversion as well as impedance transformation (50Ω to 200Ω) is connected to the two differential RF inputs (RF_IN, RF_INB).

The RF section of the MC44CD02 is comprised of an internal Low Noise Amplifier (LNA) with AGC, a set of quadrature mixers and an integrated 4GHz VCO controlled by a PLL.

The LNA with AGC is provided to cover the UHF bands IV and V (470-862 MHz). It drives the quadrature mixers that convert the RF signal to baseband quadrature I and Q. The output of the mixer connects directly to the post-mixer amplifier (PMA). Integrated capacitors are used to provide a primary low frequency filtering pole at the mixer output.

The local oscillator (LO) signal is provided by a fully integrated VCO running at four times the desired frequency that drives a divide-by-4 quadrature generator. A bank of three VCOs with sub-bands is actually used in conjunction with an automatic band switching system in order to cover the whole UHF IV and V bands with sufficient gain control. The frequency synthesis is made by means of an integer mode PLL with 1/6 MHz reference frequency. The VCO supply voltage is provided by an on-chip low noise voltage regulator (“super-filter”).

The baseband section comprises two separate I and Q paths, each containing a post mixer amplifier PMA with a register controlled gain adjustment capability, a multiple channel programmable filter (8th order inverse Chebyshev) with AGC stages, an anti-aliasing filter (4th order Butterworth), and an output buffer. The baseband signal path has 9 filtering poles distributed between mixer pole (1 pole) and the channel filter poles (8 poles) for channel filtering, and 4 additional poles for anti-aliasing.

An integrated 36 or 26 MHz crystal oscillator provides the reference clock to the baseband demodulator.

The IC is controlled through an Inter IC (I2C) bus.

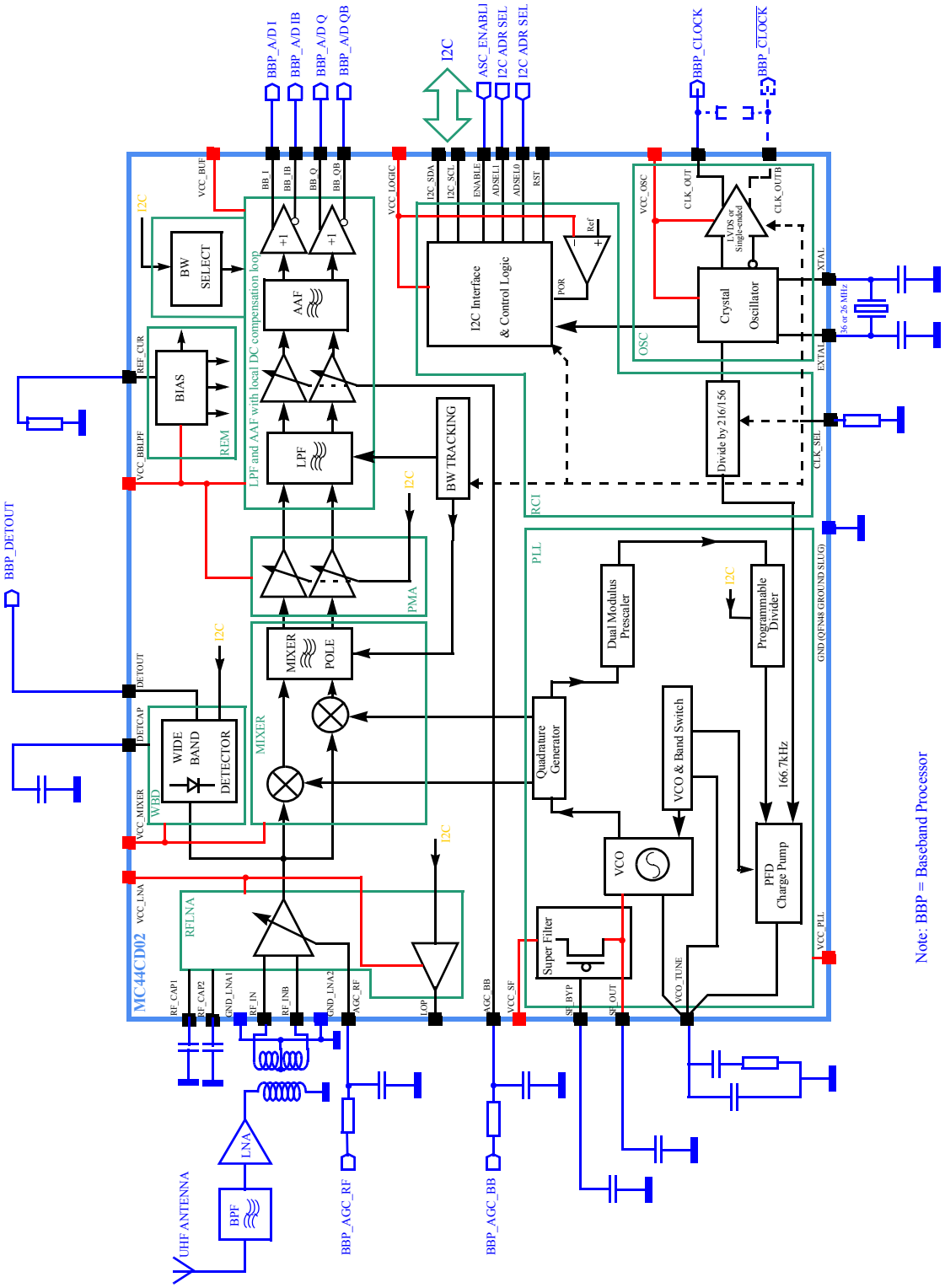

Figure 1-2 Simplified Block Diagram of the MC44CD02 Chip

Section 2 Pin Description

2.1 MC44CD02 Pin Assignment & Package

The MC44CD02 chip is mounted in a Quad Flat Pack No-Lead (QFN) 48 pin package with exposed die pad (QFN-EP version). This exposed flag (“slug”) permits an improved ground connection. This housing exhibits a 7x7 mm^2 footprint and uses a 0.5mm pitch.

WARNING

Most of the internal ground pins as well as the substrate of the IC are connected to the exposed pad. The exposed pad must be grounded in the application.

The MC44CD02 pin assignment in the QFN48 package is shown in **Figure 2-1**.

Pins declared as «NC - Not connected» have no corresponding internal connection, and thus are submitted to no constraint at application level.

Pins declared as «RESERVED» are dedicated to test analysis and must be left floating at application level.

The reset pin 18 (RST), when not used, can be left uncommited as it makes use of an internal pull-down resistor.

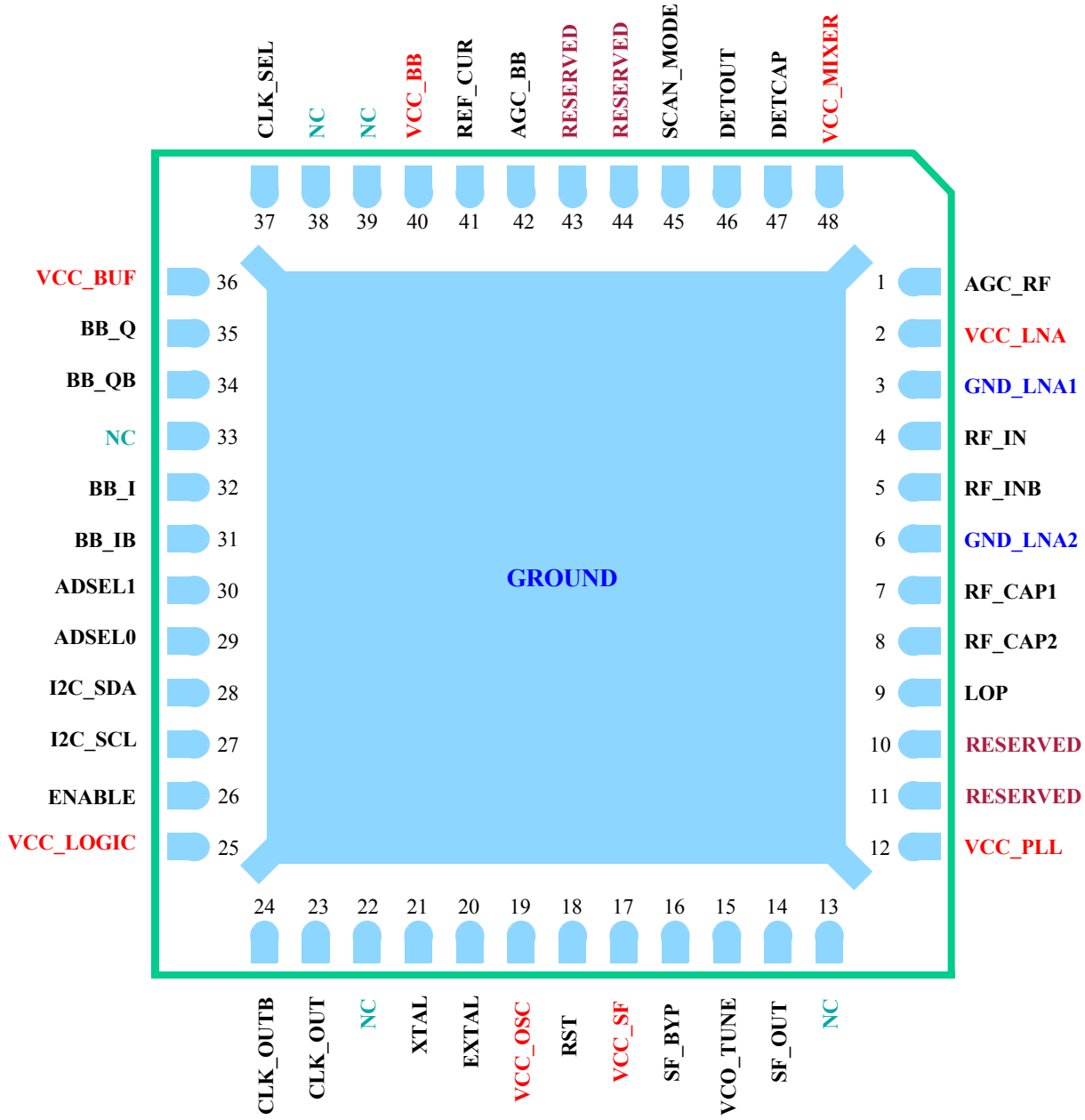

Figure 2-1 MC44CD02 QFN48 Package Bottom View Showing The Ground Slug

2.2 MC44CD02 Pin List

Following **Table 2-2** summarizes the description of every pin bonded in the QFN48 production package.

Table 2-2 MC44CD02 QFN48 Pin List

Pin Number	Pin Name	Pin Description	Nature	Type
1	AGC_RF	RF LNA AGC control voltage	I	Analog
2	VCC_LNA	LNA power supply	P	Supply
3	GND_LNA1	LNA ground (1)	P	Supply
4	RF_IN	RF input	I	Analog
5	RF_INB	RF $\overline{\text{input}}$	I	Analog
6	GND_LNA2	LNA ground (2)	P	Supply
7	RF_CAP1	RFAGC decoupling capacitor pin	C	Analog
8	RF_CAP2	RFAGC decoupling capacitor pin	C	Analog
9	LOP	Logical Output Port	O	Digital
10	RESERVED	Reserved	R	Test
11	RESERVED	Reserved	R	Test
12	VCC_PLL	PLL part supply	P	Supply
13	NC	Not connected	NC	Open
14	SF_OUT	Super Filter output voltage	C	Analog
15	VCO_TUNE	VCO tuning voltage	I/O	Analog
16	SF_BYP	Super Filter bypass capacitor	C	Analog
17	VCC_SF	Super Filter supply	P	Supply
18	RST	Reset	I	Digital
19	VCC_OSC	Crystal oscillator supply	P	Supply
20	EXTAL	Crystal oscillator input	I	Analog
21	XTAL	Crystal oscillator output	O	Analog
22	NC	Not connected	NC	Open
23	CLK_OUT	Reference clock buffered output	O	Digital
24	CLK_OUTB	Reference clock buffered $\overline{\text{output}}$	O	Digital
25	VCC_LOGIC	Control logic supply	P	Supply
26	ENABLE	Enable control pin for deep slep mode	I	Digital
27	I2C_SCL	I2C clock	I	Digital
28	I2C_SDA	I2C data	I/O	Digital
29	ADSEL0	I2C physical address selection bit 0	I	Digital

Table 2-2 MC44CD02 QFN48 Pin List

Pin Number	Pin Name	Pin Description	Nature	Type
30	ADSEL1	I2C physical address selection bit 1	I	Digiital
31	BB_IB	I baseband $\overline{\text{output}}$ signal	O	Analog
32	BB_I	I baseband output signal	O	Analog
33	NC	Not connected	NC	Open
34	BB_QB	Q baseband $\overline{\text{output}}$ signal	O	Analog
35	BB_Q	Q baseband output signal	O	Analog
36	VCC_BUF	Baseband buffers supply	P	Supply
37	CLK_SEL	Multi-level pin for Reference clock and Clock output Configuration	I	Analog
38	NC	Not connected	NC	Open
39	NC	Not Connected	NC	Open
40	VCC_BB	Baseband filter supply	P	Supply
41	REF_CUR	Reference current	C	Analog
42	AGC_BB	Baseband AGC control voltage	I	Analog
43	RESERVED	Reserved	R	Test
44	RESERVED	Reserved	R	Test
45	SCAN_MODE	Scan chain mode entry	I	Digital
46	DETOUT	Wideband detector output	O	Analog
47	DETCAP	Wideband detector integration capacitor	C	Analog
48	VCC_MIXER	Mixer supply	P	Supply
EXPOSED FLAG	GND	General Ground	P	Supply

Table 2-3 Pin Nature Description

Nature	Description
I	Input
O	Output
I/O	Input/Output
P	Power (VCC or GND)
R	Reserved
NC	Internally not connected
C	Passive Components (loop filters, filtering or storage capacitor)

Section 3 I2C Communication And Registers

3.1 Overview

This section describes MC44CD02's memory map and registers accessible through the I2C interface. The full control of the chip is accomplished via the 2-wires I2C-bus used as either slave-receiver or slave-transmitter. The MC44CD02 chip is fully compliant with the I2C-bus specification standard version 2.1. Up to 400kbit/s bus speed can be used in accordance with the I2C Fast-Mode specifications. The I2C interface stage is electrically 1.8V and 2.7V compliant.

The I2C interface of MC44CD02 cannot be used in deep-sleep mode. The address made of seven bits out of which the five most significant bits are set to 11000 as per the I2C requirements. Through a monitoring of the state of the pins ADSEL0 and ADSEL1, it is possible to modify the actual device I2C address out of four possible choices to accommodate systems where more than one MC44CD02 chip sits in the same bus (for antenna diversity reasons in mobile applications for example). The device address as a function of the ADSEL0 and ADSEL1 pins in case of both read and write operations is indicated in **Table 3-1**.

Table 3-1 MC44CD02's I2C Device Address vs. ADSEL1 & ADSEL0 Pins State

A6	A5	A4	A3	A2	A1 = ADSEL1	A0 = ADSEL0	R/$\overline{W}$	I2C Device Address
1	1	0	0	0	0	0	0	$C0
1	1	0	0	0	0	0	1	$C1
1	1	0	0	0	0	1	0	$C2
1	1	0	0	0	0	1	1	$C3
1	1	0	0	0	1	0	0	$C4
1	1	0	0	0	1	0	1	$C5
1	1	0	0	0	1	1	0	$C6
1	1	0	0	0	1	1	1	$C7

The MC44CD02 device supports the sub-addressing in order to speed up the write access of the register map. The read operation conforms to classical I2C practices. **Figure 3-2** depicts the write and read messages.

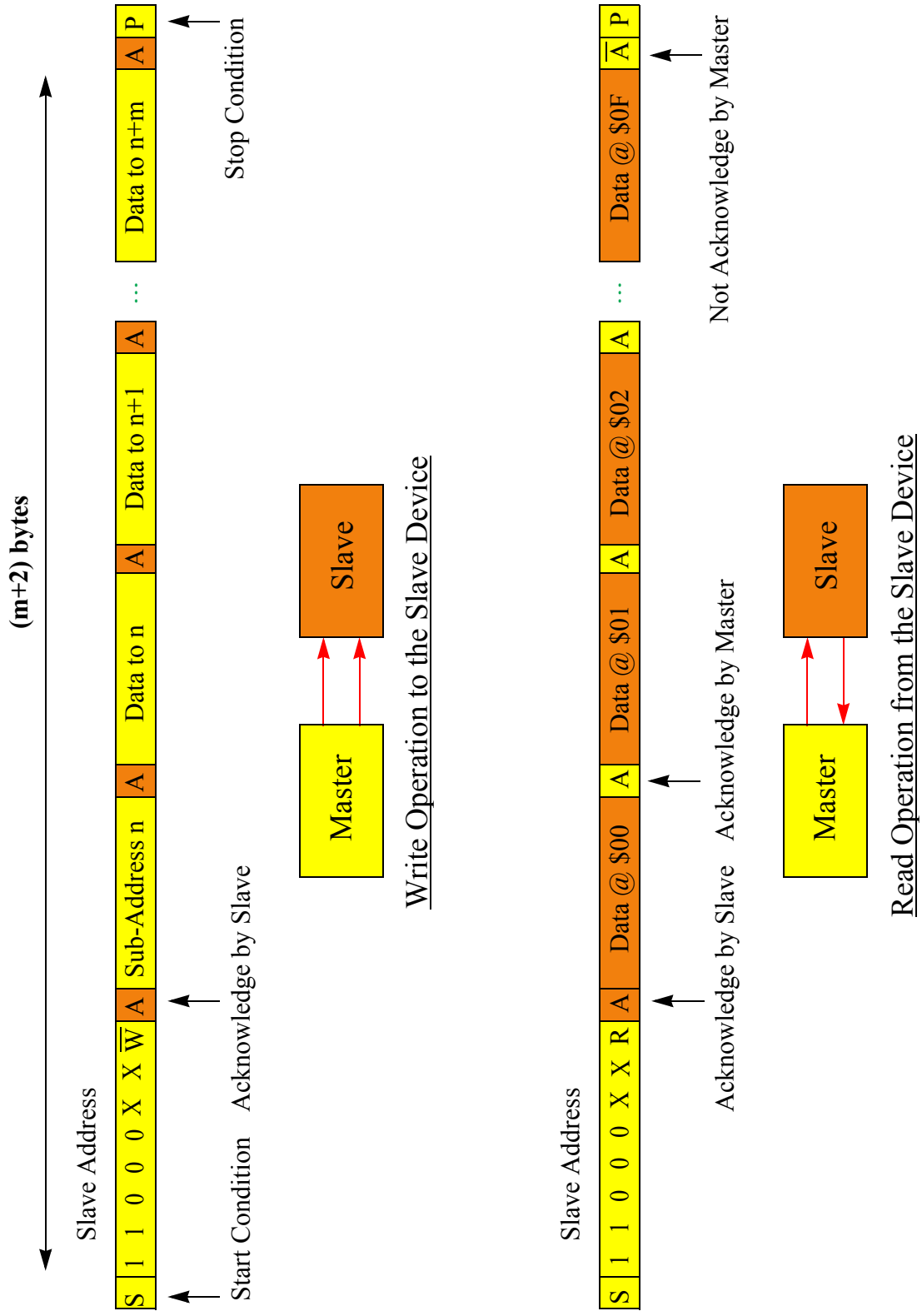

Figure 3-2 I2C Write & Read Operations

3.2 Memory Map

MC44CD02 contains a set of 16 registers in the $00 to $0F address space. The user registers constitute the bottom of the registers addressable space while test registers are placed at the higher sub-addresses. A summary of these registers is given in **Table 3-3** while their accessibility in normal mode is detailed in section **3.3**.

Table 3-3 MC44CD02 Register Map

Register Name	Register Address	Description	Reset Value
MODE	$00	Mode Register	$00
PLLR1	$01	PLL Control Register #1	$0F
PLLR2	$02	PLL Control Register #2	$9C
WBDCR1	$03	Wide Band Detector Control Register #1	$00
WBDCR2	$04	Wide Band Detector Control Register #2	$00
LNAOSCR	$05	Low Noise Amplifier & Oscillator Control Register	$20
MISCR	$06	Miscellaneous Control Register	$00
MDTST1	$07	Reserved	$00
MDTST2	$08	Reserved	$00
LPFTST	$09	Reserved	$00
PLLTST1	$0A	Reserved	$00
PLLTST2	$0B	Reserved	$0D
RFTST	$0C	Reserved	$00
TLTST	$0D	Reserved	$00
VTBSTA	$0E	Reserved	$00
TLSTA	$0F	Reserved	$00

3.3 Register Descriptions

3.3.1 MODE — Mode Register

The MODE register dictates MC44CD02's operating mode.

Register address $00

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PDM	PLLBI	TSTM
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-4 MC44CD02 Mode Register (MODE)

Bits 2-0 of the MODE register are readable and writable anytime. Bits 7-3 cannot be written and always read "0".

PDM — Power Down Mode.

If the ENABLE pin is held high, this bit permits to place the MC44CD02 chip in power down mode with only the oscillator core and associated output clock drivers activated. This feature is used in case of time slice operation where the receiving of the DVB-H signals is pulsed with a low duty cycle to save power consumption. The ENABLE pin has precedence over the PDM control bit, which means that whenever the ENABLE pin is held low, the PDM bit state is cleared and the part placed in deep sleep mode.

1 = MC44CD02 chip is in power down mode if the ENABLE pin is asserted.
0 = MC44CD02 chip is in normal mode if the ENABLE pin is asserted.

PLLBI — PLL Band Change Inhibit.

This bit permits to freeze the PLL VCO and associated sub-band in its current operating configuration. This feature is useful to rapidly regain lock after the circuit has been placed in a power saving mode.

1 = Band lock activated.
0 = Band lock de-activated (automatic VCO and sub-band searching is possible).

TSTM — Analog Test Mode.

The setting of the TSTM bit places the chip in test mode.

1 = Test mode is activated.
0 = Test mode is not activated.

Asserting the TSTM bit by itself does not produce any modification to MC44CD02's operation, it simply enables test functions to be activated and test outputs to be possibly observed. The reset values of the test bits are read at 0 in normal mode.

3.3.2 PLLR1 — PLL Control Register #1

The PLLR1 register contains the ref clock bit along with the five most significant bits of the programmable divider

Register address $01

	7	6	5	4	3	2	1	0
R	0	0	REFCLK	PD12	PD11	PD10	PD9	PD8
W								
Reset:	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 3-5 PLL Control Register #1 (PLLR1)

In all mode, bits 5-0 of the PLLR1 register are readable and writable anytime. Bits 7-6 cannot be written and always read “0”.

REFCLK— Sets the chip in line with the chosen reference clock frequency (either 36MHz or 26MHz reference clock).

Only active when the I2C bit PADCTRL (reg $05) is set to 1 (otherwise, as PADCTRL=0, the reference clock frequency is controlled by the multi-level pin#37 CLK_SEL).

1 = 26MHz

0 = 36MHz

PD12-8 — Programmable Divider MSBs.

These five bits are complemented by the 8 bits of the PLLR2 register to form the 13 bits used to define the programmable divider ratio, part of the PLL feedback divider. A sequential logic exists to transfer the register bits PD[12:0] into the programmable divider when this last has finish to count-down.

WARNING

Any change in the programmable divider ratio must be performed using two write operations in any order in any of the PLLR1 (5 MSBs) and PLLR2 (8 LSBs) registers. There is no need for the two write operations to take place within two consecutive cycles.

WARNING

It is forbidden to write PD<12:0>=$0000 in the PLLR1 and PLLR2 registers as this value jeopardizes the programmable divider functioning.

If we call PD the decimal content of the 13 bits constituting the programmable divider ratio, the synthesized LO frequency is given by the following equation:

$$F_{LO}\ [MHz] = PD/6$$

For example, the reset values of the PLLR1 and PLLR2 registers lead to a synthesized LO frequency of 666MHz (PD=3996), which corresponds to the UHF channel 45 for countries using 8MHz channel bandwidth and zero offset[1].
It is interesting to note that the VCO inside the PLL module runs at a frequency equals to 4* F_{LO}.

3.3.3 PLLR2 — PLL Control Register #2

The PLLR2 register contains the 8 LSBs of the programmable divider ratio.

Register address $02

	7	6	5	4	3	2	1	0
R W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Reset:	1	0	0	1	1	1	0	0

= Unimplemented or Reserved

Figure 3-6 PLL Control Register #2 (PLLR2)

All bits in the PLLR2 register are readable and writable anytime. See description and warnings in the previous section.

3.3.4 WBDCR1— Wide Band Detector Control Register #1

The WBDCR1 register contains bits to control the Wide Band Detector operation.

Register address $03

	7	6	5	4	3	2	1	0
R	0	0	IDISCHG2	IDISCHG1	IDISCHG0	ICHG2	ICHG1	ICHG0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 Wide Band Detector Control Register #1 (WBDCR1)

In all modes, bit 5-0 in register WBDCR1 are readable and writable anytime. Bits 7-6 cannot be written and always read “0”.

NOTES:
1. The DVB-T signal may be shifted upward or downward from the ideal channel center frequency by an offset frequency of +/- 1/6 MHz.

IDISCHG2-0 — Current Discharge selector.

These 3 bits set the amount of discharging current of the wide band detector as indicated in **Table 3-8**. They drive the decay rate of the WBD output for a given capacitor.

Table 3-8 Typical discharging current vs. IDISCHG[2:0]

IDISCHG[2:0]	Value (uA)
000	26.6
001	10.6
010	15.9
011	21.3
100	31.9
101	37.9
110	42.5
111	output disabled

ICHG2-0 — Current Charge selector.

These 3 bits control the level of charging current for the external capacitor as indicated in **Table 3-9**. This current controls the rise time of the WBD output.

Table 3-9 Typical charging current vs. ICHG[2:0]

ICHG[2:0]	Value (uA)
000	836
001	790
010	744
011	698
100	880
101	924
110	967
111	1011

3.3.5 WBDCR2 — Wide Band Detector Control Register #2

The WBDCR2 drives the detector transfer function offset and gain.

Register address $04

	7	6	5	4	3	2	1	0
R	0	0	DETOFF2	DETOFF1	DETOFF0	DETGAIN2	DETGAIN1	DETGAIN0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-10 Wide Band Detector Control Register #2 (WBDCR2)

In all modes, bit 5-0 in register WBDCR2 are readable and writable anytime. Bits 7-6 cannot be written and always read “0”.

DETOFF2-0 — Detector Offset Adjustment.

Adjusts the output current of the detector transfer function as shown **Table 3-11**.

Table 3-11 Typical current sourced vs. DETOFF[2:0]

DETOFF[2:0]	DC level (uA)
000	-10.9
001	-7.3
010	-3.6
011	0
100	3.9
101	7.7
110	11.6
111	15.4

DETGAIN2-0 — Detector Gain Adjustment.

Adjusts the detector transfer function gain as indicated **Table 3-12**.

Table 3-12 Typical detector gain vs. DETGAIN[2:0]

DETGAIN[2:0]	Gain
000	2.21
001	2.27
010	2.33
011	2.4
100	2.47

Table 3-12 Typical detector gain vs. DETGAIN[2:0]

DETGAIN[2:0]	Gain
101	2.55
110	2.64
111	2.74

3.3.6 LNAOSCR — Low Noise Amplifier & Oscillator Control Register

The LNAOSCR register contains bits to adapt the RFAGC loop and to control the oscillator buffer.

Register address $05

	7	6	5	4	3	2	1	0
R W	CLKBUF	CLKDD	ALC1	ALC0	ILVDS	PADCTRL	AGCOFF1	AGCOFF0
Reset:	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-13 Low Noise Amplifier & Oscillator Control Register (LNAOSCR)

In all modes, bits 7-0 in register LNAOSCR are readable and writable anytime.

CLKBUF — Reference Clock Buffer Selector.

This bit selects either the single-ended or LVDS buffer. Only active when the I2C bit PADCTRL (reg $05) is set to 1 (otherwise, as PADCTRL=0, the reference clock buffer selection is controlled by the multi-level pin#37 CLK_SEL).

1 = The single-ended buffer is selected.

0 = The LVDS buffer is selected.

CLKDD — Reference Clock Output Driver Disable

In case the reference clock generated by the MC44CD02 chip is not used, the CLKDD bit can be set HIGH to switch OFF the corresponding output driver (pins CLK_OUT, CLKOUTB), hence saving power consumption and minimizing radiated emissions.

1 = Reference clock output driver is disabled.

0 = Reference clock output driver is enable.

ALC1-0 — Amplitude Oscillator Control.

Determines according to **Table 3-14** the peak to peak sinewave clock amplitude at the XTAL pin.

Table 3-14 Crystal Oscillator Sine Wave Amplitude vs. ALC[1:0]

ALC[1:0]	Sine Wave Amplitude (Vpp)
00	-
01	-
10	1
11	-

ILVDS — Selects the LVDS buffer output current OR the Single-Ended buffer Clock Shape.

This bit can either selects the output current of the CLK_OUT customized LVDS buffer if this buffer is selected or selects the single-ended buffer clock shape.

1 = The output current is set to 1mA if the LVDS buffer is selected (CLKBUF=0) or set the CMOS 1.8V square wave if the single-ended buffer is selected (CLKBUF=1).

0 = The output current is set to 500uA if the LVDS buffer is selected (CLKBUF=0) or set the sine like wave if the single-ended buffer is selected (CLKBUF=1).

PADCTRL — Gives priority either to the multi-level pin#37 CLK_SEL or to the I2C to configure the MC44CD02 chip and its clock outputs with regards to the reference clock frequency and the application requirements.

1 = The I2C bits REFCLK (reg $01) and CLKBUF ($05) have priority.

0 = The multi-level pin#37 CLK_SEL has priority.

WARNING

When using the PADCTRL bit, two I2C messages are needed to program the device properly because of the registers order.

First I2C message: Write PADCTRL=1.
Whatever value is written during the same message in REFCLK bit will be ignored.

Second I2C message: Rewrite PADCTRL=1. REFCLK value will be take into account.

AGCOFF1-0 — AGC Loop Offset Selector.
These 2 bits control the offset of the AGC loop as indicated **Table 3-15**. Only the default value configuation (no offset) has to be used.

Table 3-15 AGC Loop Offset vs. AGCOFF[1:0]

AGCOFF[1:0]	RFAGC Knee voltage shift relative to nominal (mV)
00	0
01	NOT TO BE USED
10	NOT TO BE USED
11	NOT TO BE USED

3.3.7 MISCR— Miscellaneous Control Register

The MISCR register contains bits controlling the post-mixer amplifier (PMA), the anti-aliasing lowpass filter and the Logical Output Port (LOP) state, and some PLL test feature.

Register address $06

	7	6	5	4	3	2	1	0
R W	PFDTST0	AAFD	LNABO	LNAGS	PMAG1	PMAG0	BW1	BW0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-16 Miscellaneous Control Register (MISCR)

In all modes, bits 7-0 in register MISCR are readable and writable anytime.

PFDTST0 — PLL Test Feature.

Reverse the polarity of the reference clock signal driving the phase-frequency detector of the PLL.

AAFD — Anti-Aliasing Filter Disable.

The anti-aliasing filter is a sub-block of the whole baseband Low-pass Filter module.

1 = Anti-aliasing filter is disabled. Only the baseband channel low pass filter is activated, driving the baseband buffer towards the I/Q outputs.

0 = Anti-aliasing filter is enabled. The whole baseband filtering chain (channel low pass filter plus anti-aliasing filter), driving the baseband buffer towards the I/Q outputs.

LNABO — Topology of the Logical Output Port.

1 = The LOP buffer exhibits an open-drain, pull-down output.

0 = The LOP buffer exhibits a CMOS output.

LNAGS — State of the Logical Output Port.

1 = Pad LOP receives a logical “1”.

0 = Pad LOP receives a logical “0”.

PMAG1-0 — Post Mixer Amplifier Gain Setting.

The Post-Mixer Amplifier gain as a function of the state of the PMAG bits is indicated in **Table 3-17**.

Table 3-17 PMA gain vs. PMAG[1:0]

PMAG[1:0]	Gain (dB)
00	14
01	10
10	12
11	14

BW1-0 —Low-Pass Filter Bandwidth Selector.

Set the low-pass filter nominal bandwidth to 6MHz, 7MHz or 8MHz according to **Table 3-18**.

Table 3-18 Filter nominal bandwidth BW[1:0]

BW[1:0]	Nominal Bandwidth
00	8MHz
01	
10	7MHz
11	6MHz

3.3.8 MDTST1 — Module Disable Test Register #1

MDTST1 is a register reserved for test purposes.

Register address $07

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-19 Module Disable Test Register #1 (MDTST1)

In normal mode, the MDTST1 register read $00 and cannot be written.

3.3.9 MDTST2 — Module Disable Test Register #2

MDTST2 is a register reserved for test purposes.

Register address $08

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-20 Module Disable Test Register #2 (MDTST)bfddf

In normal mode, the MDTST2 register read $00 and cannot be written.

3.3.10 LPFTST — Baseband Low Pass Filter Test Register

LPFTST is a register reserved for test purposes

Register address $09

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-21 Baseband Low Pass Filter Test Register (LPFTST)

In normal mode, the LPFTST register reads $00 and cannot be written.

3.3.11 PLLTST1 — PLL Test Register #1

PLLTST1 is a register reserved for test purposes

Register address $0A

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-22 PLL Test Register #1 (PLLTST1)

In normal mode, register PLLTST1 reads $00 and cannot be written.

3.3.12 PLLTST2 — PLL Test Register #2

PLLTST2 is a register reserved for test purposes.

Register address $0B

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	1	1	0	1

= Unimplemented or Reserved

Figure 3-23 PLL Test Register #2 (PLLTST2)

In normal mode, register PLLTST2 reads $00 and cannot be written.

3.3.13 .RFTST — RF Blocks Test Register

RFTST is a register reserved for test purposes.

Register address $0C

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-24 RF Blocks Test register (RFTST)

In normal mode, the RFTST register reads $00 and cannot be written.

3.3.14 TLTST — Tracking Loop Test Register

TLTST is a register reserved for test purposes.

Register address $0D

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-25 Tracking Loop Test Register (TLTST)

In normal mode, the TLTST register read $00 and cannot be written.

3.3.15 VTBSTA — VCO Tuning Band Status Register

VTBSTA is a register reserved for test purposes.

Register address $0E

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-26 VCO Tuning Band Status Register (VTBSTA)

In normal mode, the VTBSTA register reads $00 and cannot be written.

3.3.16 TLSTA — Tracking Loop Status Register

TLSTA is a register reserved for test purposes.

Register address $0F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-27 Tracking Loop Status Register (TLSTA)

In normal mode, the TLSTA register reads $00 and cannot be written.

Section 4 Functional Description

The following sub-sections address some general key points about the MC44CD02device operation, then detail the functional descriptions of each sub-block in their respective operating modes.

4.1 Modes Of Operation

The MC44CD02 device includes three different power modes controlled by a combination of hardware (ENABLE pin) and software (state of the PDM bit in the MODE register at I2C address $00). The modes are summarized in **Table 4-1**. Furthermore, the PDM bit is automatically reset to 0 while entering in Deep Sleep mode. It is therefore impossible to switch from Deep Sleep to Power Down mode without going though the Normal mode. Finally, MC44CD02 device lasts 20ms to be stable when waking-up from Power Down mode to Normal mode, and 200ms when waking-up from Deep Sleep mode to Normal mode.

Table 4-1 Power Operating Mode vs. ENABLE & PDM States

ENABLE Pin	PDM Bit	Mode
0	X[1]	Deep Sleep
1	0	Normal
1	1	Power Down

NOTES:
1. Don't Care.

4.1.1 Normal Operation Mode

This is the normal operating mode of the receiver where all the internal stages are activated.
In this mode, the current consumption under typical conditions (VCC=2.775V and Temp.=27°C) is defined in the General MC44CD02 Electrical Specification, appendix A.3, ID 1.1.

4.1.2 Power Down Mode

In this mode the MC44CD02 circuit will have very low current drain. The 36 or 26 MHz reference oscillator core and its buffers are activated to provide the clock signal to the baseband demodulator. The logic section remains powered such that the received channel settings remain stored in their corresponding I2C registers. Furthermore, the superfilter (that provides the supply voltage to the VCOs) is also activated, for VCO/PLL settling time purposes. However, all the others blocks are disabled.
In this mode, the current consumption under typical conditions (VCC=2.775V and Temp.=27°C) is defined in the General MC44CD02 Electrical Specification, appendix A.3, ID 1.2.

4.1.3 Deep Sleep Mode

This mode is intended to have the lowest current drain. All stages are fully disabled except the power-on reset function which continuously monitors the voltage on the VCC_LOGIC pin such as to produce a reset and then place the chip in a known configuration in case of power failure or brown-out. Furthermore, the logic section remains powered such that the received channel settings remain stored in their corresponding I2C registers.
The circuit enters into deep-sleep mode through the control of an external pin that has priority on the power down/normal mode selection as shown in **Table 4-1**.
In deep-sleep mode, the reset (external pin RST), and address select (external pins ADSEL0 and ADSEL1) functionalities are disabled. Those functionalities are available as the circuit is on Normal or Power down mode only.

In this mode, the current consumption under typical conditions (VCC=2.775V and Temp.=27°C) is defined in the General MC44CD02Electrical Specification, appendix A.3, ID 1.3.

4.2 Filtering

The overall characteristic is composed by the analog filtering in the MC44CD02 (both channel filtering with programmable bandwidth, and anti-aliasing filtering), and a digital filtering in the baseband demodulator. Therefore the task of the MC44CD02 analog filter is to provide enough attenuation to the adjacent channel power in order not to saturate filtering stages in front of the baseband demodulator input and especially the Sigma-Delta AD converter, and to provide sufficient stop-band attenuation to cope with the baseband IC ADC sampling requirements. The final channel filtering is performed inside the baseband demodulator.

The system has to cope with different adjacent channel scenarii (adjacent upper channel vision carrier, adjacent lower channel sound carriers...). The adjacent channel can be an analog interferer (pattern S1) or a digital DVB-T adjacent channel interferer (pattern S2). These patterns are described in the reference [1] document. Those patterns define the channel filtering performance the MC44CD02 chip must perform.

Furthermore, the stopband attenuation specification was defined such that interferers beyond the Nyquist frequency, which will be folded into the wanted band during the A-to-D conversion and act like a noise contribution, do not hurt the required S/N ratio.

The MC44CD02 channel filtering section consists of a 8^{th} order baseband channel low pass filter LPFs (inverse Chebyshev structure) with variable gain amplifiers.

A first stage of additional filtering lies in the mixer output pole (15 MHz).

The MC44CD02 supports three different channel bandwidths: 6, 7, and 8 MHz.

The inverse Chebyshev characteristic is chosen such has to have a limited amplitude ripple in the passband.

The channel filter is followed by the baseband anti-aliasing low pass filter AAFs (4th order Butterworth structure) to provide the required stop band attenuation.

The I/Q output signals are provided by output buffers for driving purposes. The I/Q signals must fulfill the following requirements:

- Differential signal amplitude: 1.4Vpp maximum;
- Baseband differential input resistance: 10kΩ minimum;
- Baseband input capacitance: 5pF maximum.Control Loops

4.3 Control Loops

4.3.1 AGC Loops

The non-interrupted mode of the OFDM modulation for DVB-H forces a quasi continuous control of the AGC correction loop.

The AGC system is split between RF AGC (in the LNA) and baseband AGC. Both those AGCs are controlled through two dedicated pins by analog signals provided by Sigma-Delta (ΣΔ) DACs at the baseband demodulator IC output.

At the output of the internal LNA, a broadband RF detector (WBD module) takes part to this AGC system by sensing strong signals into the whole UHF band, and sending the information to the baseband demodulator IC through a dedicated pin (DETOUT).

The AGC correction algorithms are left to the baseband demodulator IC.

The Post Mixer Amplifier (PMA) also exhibits gain control capabilities (through I2C programming), but this capability is not part of AGC system.

4.3.1.1 RF AGC Control Loop

The AGC is directly controlled by an RC filtered pulse width modulated signal (filtered 1-bitΣΔ output) provided by the baseband demodulator with the following properties:

- Voltage range: from 0.1V to 1.8V;
- Impedance: RC filter with 10 kΩ in series and 22 nF to ground.

4.3.1.2 Baseband AGC control loop

AGC stages are inserted in the filtering chain in order to cover the overall dynamic range specifications. An AGC range of 35 dB minimum is required. Due to the large gain required in the baseband section, local DC offset correction loops for I and for Q are necessary to avoid saturation in cascaded stages. For this purpose each channel has its specific DC cancellation loop with an external storage capacitor.

The AGC is directly controlled by a RC filtered pulse width modulated signal (filtered 1-bit ΣΔ output) provided by the baseband demodulator with the following properties:

- Voltage range: from 0.1V to 1.8V;
- Impedance: RC filter with 10 kΩ in series and 22 nF to ground.

4.3.2 DC Offset Correction

Despite the AC coupling on I/Q signals between the MC44CD02 device and the baseband processor, and due to the high gain level required at baseband stages, the baseband section includes local DC offset correction loops to avoid signal distortion. No interaction with the baseband demodulator IC is required.

4.3.3 Filter Tracking

The MC44CD02 chip supports multiple OFDM modulation bandwidths (6, 7, 8 MHz) via I2C programming. The filter calibration is ensured by an autonomous tracking bandwidth system derived from the crystal oscillator reference, with a maximum frequency drift of 6%.

4.3.4 Common Mode Voltages

4.3.4.1 I/Q Buffers Outputs

The MC44CD02 chip and the baseband-demodulator IC are AC coupled (1kHz). No common mode voltage control loop is thus necessary.

4.3.4.2 CLK_OUT Outputs

The MC44CD02 chip either delivers a custom LVDS clock reference or a single-ended clock reference to the baseband processor. The reference clock buffer mode is selected by I2C programming.

The LVDS delivery of the clock reference implies the flowing of differential currents carrying the frequency information. A resistor is used at the baseband inputs level to generate a differential, small amplitude clock voltage. The common mode voltage of the CLK_OUT and CLK_OUTB pins is derived from a very accurate bandgap reference voltage, and therefore requires no common mode feedback system to ensure proper interfacing between the two chips.

The single-ended buffer of the clock reference provides either a 1.8V CMOS signal or a sine-like 1.5Vpp signal with 0.9V common mode voltage on pin CLK_OUT, while pin CLK_OUTB remains open.

4.3.5 I/Q Mismatch

The whole I/Q static mismatch compensation is performed in the baseband demodulator IC, not in the RF front-end chip.

4.4 Reference Clock Configuration

The MC44CD02 chip is able to handle two different reference clock frequencies, 26MHz and 36MHz. This reference frequency is either generated by means of crystal oscillator (using an external 26MHz or 36MHz crystal element connected between pin #20 EXTAL and pin #21 XTAL), or externally provided to the chip on its pin #20 EXTAL.
The MC44CD02 chip is also capable to provide two different clock output signal shapings (either LVDS or single-ended) to the baseband demodulator IC through the clock output pins #23 CLK_OUT and #24 CLK_OUTB.

At power on reset, a proper setting of the IC with regards to the reference clock frequency is suitable to fit the application requirements. Particularly, a correct power on reset configuration of the clock output signal is required, as this signal is potentially used to wake-up and clock the baseband demodulator IC.

Therefore, a multi-level pin (pin #37 CLK_SEL) is dedicated to adequately preset the MC44CD02 chip and its clock output signal in the configuration required by the application. See the AAF (multi-level pin) module description chapter for more details.

4.5 WBD Functional Description

4.5.1 General

The purpose of this section is to detail the WBD module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.5.2 Normal Mode

The Normal mode corresponds to the WBD operating in the receive chain in a regular manner.

The UHF wideband detector helps to prevent the RF stages from saturating in presence of strong interferers (PAL / SECAM / DVB-T) in the UHF band. If saturation occurs, severe distortion of the on-channel signal would result. The detector provides a measurement of the peak signal level present at the internal LNA-with-AGC output, and feeds this information back to the baseband demodulator IC via an analog output signal. The baseband processor then analyzes both the in-band signal information and the wideband signal information, and eventually correct the AGC response accordingly at both RF and baseband stages.

In any interferer case (PAL, SECAM, DVB-T interferers), the RF power detection with a peak detector is the more appropriate detection system. The detector requires a short "charge" time constant to rapidly detect the signal amplitude, but a long "discharge" time constant in order not to follow any AM modulation, which would cause AGC pumping.

The time constant will be defined in order to get a compromise between an analog TV signal detection and a DVB-T signal detection. A DVB-T signal can be considered as a pure noise signal where the peak-to-mean ration is given by the standard and limited to + 12 dB.

The cut-off frequency is defined by the sampling rate of the slow ADC integrated in the baseband demodulator. The effective sampling rate is in the order of 1 KHz that means that the cut-off frequency will stay below about 500 Hz which corresponds to a decay time of 2 ms. An external capacitor is used to generate such a long time constant. The combination between the value of this external capacitor and the discharging current of the MC44CD02 will define the time constant. This will be explained later on the application recommendations section.

The peak amplitude detection must be dimensioned according to the synchronization pulse of PAL modulated signals (**Figure 4-2**).

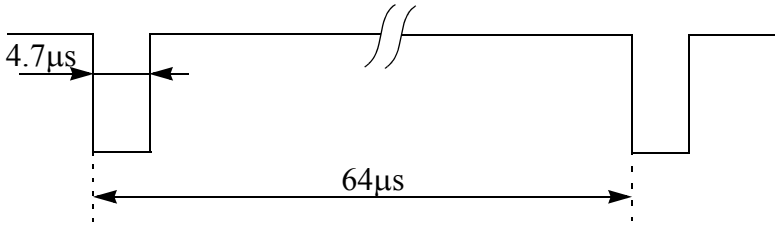

Figure 4-2 PAL Synchronization Signal

A cut-off frequency in the range of 500 Hz (2ms) is assumed, adequate for PAL modulated signals, and in agreement with the effective sampling rate of the baseband processor ADC. SECAM modulated signals are more problematic due to their positive modulation scheme, and may require additional signal processing in the baseband processor.

The decay rate is dimensioned according to the resolution of the baseband processor input ADC. 8 bits cover a range of about 2 volts, leading to a 1 LSB value of 8mV. Therefore, a decay rate of 5mV/2ms (2.5mV/ms) is appropriate.

The output signal dynamic must be dimensioned in order to take advantage of the 8-bits slow ADC resolution at the input of the baseband digital demodulator (effective sampling rate of 1kHz / voltage range 0.1V to 2.7V / resistance 20kΩ minimum). The linearization of the detector response will be performed inside the digital demodulator after the slow AD converter.

4.5.3 WBD calibration procedure

Tuning is mandatory in order to guarantee that WBD meets error specification. This tuning concerns one of the registers (WBD Control Register 2, $04 address) containing information about detection offset, and detector gain. Calibration algorithm is the following (frequency set at 666MHz, external LNA gain and RFAGC gain both set at their maximum values):

Step 1: With detector gain set to 3 (intermediate position) and -40dBm at the tuner input for maximum LNA gain condition, use detector offset bits to set the detection voltage output as close as possible to 1.6V.

Step 2: With this new setting of detector offset bits, keep tuning using the detector gain bits in order to set the detector output voltage as close as possible of the 1.6V target.

The I2C registers values found should be saved in system memory, and programmed into the tuner at start-up. This is normally a one time calibration routine that should occur in production.

4.5.4 Deep Sleep & Power Down Mode

The WBD module will be in low power mode (current consumption <1µA) when

- ENABLE (pin 26) is held at logic low.
- ENABLE is held at logic high and the PDM bit (in the MODE register at I2C address $00) is asserted.

4.6 OSC Functional Description

4.6.1 General

The purpose of this section is to detail the OSC module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Power Down Mode.
3. Deep Sleep

4.6.2 Normal Mode

The Normal Mode corresponds to the OSC module operating in a regular manner, i.e. in oscillation mode. The OSC module is set into normal mode once a high level is applied on the MC44CD02 input pin #26 ENABLE.

4.6.2.1 Crystal Oscillator Principle

The OSC module is made of a 36 or 26 MHz crystal oscillator based on the Pierce architecture. The active part of the oscillator is integrated on chip (active device of the negative impedance and biasing), while the passive parts (feedback capacitors and 36 or 26 MHz crystal element) are external and connected around the input pins #20 EXTAL and #21 XTAL.

The start-up of the oscillator is sped up by the use of a boost mode. The principle is to increase the biasing current at start-up, and to reduce it for normal mode operation after a pre-defined number of clocks is counted. This system ensures proper start-up and oscillation amplitude.

The 36MHz or 26MHz sinusoïdal oscillation signal is buffered and turned into a 36MHz or 26MHz CMOS signal, to provide the clock for the digital core of the MC44CD02 chip, the input clock of the reference divider of the PLL (division ratio 216 or 156 to generate 166.66kHz), and the refence clock for the baseband demodulator chip through one of the clock output buffer (either custom LVDS buffer driving the output pins #23 CLK_OUT and #24 CLK_OUTB, or the single-ended buffer driving the output pin #23 CLK_OUT).

4.6.2.2 Recommended Crystal Characteristics

The selected crystals are the NX3225DA 36MHz (W-191-563) or 26MHz (W-191-653) quartz's from the NDK company . The following **Table 4-3** and **Table 4-4** summarize their key characteristics.

Table 4-3 36MHz NX3225DA Quartz Key Characteristics

Feature	Typical Value
Operating Mode	Fundamental
Motional Inductance	4.90 mH
Motional Capacitance	3.99 fF

Table 4-3 36MHz NX3225DA Quartz Key Characteristics

Feature	Typical Value
Motional Resistance[1]	50 Ω
Case Capacitance	1 pF
Loading Capacitance	8 pF

NOTES:
1. Maximum value upon startup.

Table 4-4 26MHz NX3225DA Quartz Key Characteristics

Feature	Typical Value
Operating Mode	Fundamental
Motional Inductance	3.75 mH
Motional Capacitance	10 fF
Motional Resistance[1]	50 Ω
Case Capacitance	1 pF
Loading Capacitance	8 pF

NOTES:
1. Maximum value upon startup.

4.6.2.3 External Reference Clock

The EXTAL input pin of the OSC module can be used as the input gate for an external reference clock, that is then used as the reference clock for the whole chip including PLL. In that case, the OSC circuit does not behave anymore as a crystal oscillator (and the external crystal element and feedback capacitors must be removed from the application schematic - refer to the application information chapter of this document for additional details), but as as buffer for this reference clock.
Extreme care must be taken concerning the amplitude, duty-cycle, and jitter (phase noise) of the external reference clock not to impact digital core nor PLL performances. Constraints are detailled in the electrical specifications chapters of this document.

4.6.2.4 Reference Clock Frequency

The MC44CD02 chip is able to handle two different reference clock frequencies 36MHz and 26MHz. Different modules of the chip (digital core, PLL, tracking loop filter, clock outputs...) need to be configured according to the reference clock frequency used.

As the I2C bit PADCTRL (reg $05) is held at logic low, the chip configuration with regards to the clock frequency is set by the DC level applied on multi-level pin#37 CLK_SEL (see the MLP Functional Description chapter for more details). As the I2C bit PADCTRL is turned high, the chip configuration is forced by the value of the I2C bit REFCLK (reg $01).

The reset value of the I2C bit PADCTRL is 0, such as at power on reset, priority is given to the multi-level pin#37 CLK_SEL to configure the MC44CD02 chip according to the reference clock frequency used.

4.6.2.5 Reference Clock Ouput Interface

Two different clock buffers can be used for interfacing the 36MHz or 26MHz reference clock from the MC44CD02 chip to the baseband demodulator circuit. Both those buffers cannot be activated simultaneously.

As the I2C bit PADCTRL (reg $05) is held at logic low, the clock buffer selection is set by the DC level applied on multi-level pin#37 CLK_SEL (see the MLP Functional Description chapter for more details).
As the I2C bit PADCTRL is turned high, the clock buffer selection is forced by the value of the I2C bit CLKBUF (see the I2C Communication and Registers chapter for more details).
The reset value of the I2C bit PADCTRL is 0, such as at power on reset, priority is given to the multi-level pin#37 CLK_SEL to configure the clock buffer according to the application requirements.

4.6.2.5.1 Custom LVDS interface

A custom Low Voltage Differential Signaling (LVDS) technology is used for interfacing the 36MHz or 26MHz reference clock from the MC44CD02chip to the baseband demodulator circuit. Such a technology allows low noise and low electromagnetic interference spreading over the radio board.

The LVDS buffer is selected as the I2C bit CLKBUF is set to 0.
The MC44CD02 chip provides the 36MHz or 26MHz differential output currents on its output pins #23 CLK_OUT and #24 CLK_OUTB. The signal swing is generated through a load consisting of an external differential resistor. Two different current settings can be programmed through the I2C bit ILVDS. The custom LVDS swing is developed around a common mode level that is derived from a bandgap voltage sufficiently accurate to avoid the use of any common mode control loop.

The LVDS buffer can be disabled by setting the I2C bit CLKDD to high logic level.

4.6.2.5.2 Single-ended Clock interface

A single-ended buffer is also available for interfacing the 36MHz or 26MHz reference clock from the MC44CD02 chip to the baseband demodulator circuit.

The single-ended buffer is selected as the I2C bit CLKBUF is set to 1.
In that case, the MC44CD02 chip provides the 36MHz or 26MHz output signal on the output pin #23 CLK_OUT. The output signal is either 1.8V CMOS shaped as the I2C bit ILVDS is set to 1, or 1.5Vpp analog-like as the I2C bit ILVDS is set to 0.

The single-ended buffer can be disabled by setting the I2C bit CLKDD to high logic level.

4.6.3 Power Down Mode

There is no Power Down Mode (PDM) for the OSC module. When the MC44CD02 chip is in PDM, the OSC module remains in Normal Mode, providing the reference clock to the digital core, and to the baseband demodulator circuit through the selected clock buffer (either custom LVDS or single-ended).

4.6.4 Deep Sleep Mode

In Deep Sleep Mode, the OSC module is turned off by removing its biasing current. Oscillations and derived clocks are disactivated. The OSC module is set into deep sleep mode once a low level is applied on the input pin #26 ENABLE.

4.7 PLL Functional Description

4.7.1 General

The purpose of this section is to detail the PLL module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.7.2 Normal Mode

The Normal mode corresponds to the PLL operating in the receive chain in a regular manner.

4.7.2.1 PLL Characteristics

The MC44CD02 chip is able to receive all DVB-T channels in the UHF bands IV and V, ranging from 470 to 862 MHz. Furthermore, the DVB-T signal may be shifted from the ideal channel frequency 1/6 MHz up or downwards. Those considerations, coupled to phase noise requirements, drive the choice of the frequency synthesizer architecture.

The frequency synthesizer of the MC44CD02 chip is based on an integer mode PLL with 1/6 MHz reference frequency, derived from a 36 or 26 MHz crystal oscillator clock.

4.7.2.2 Loop Filter Considerations

Following **Figure 4-5** depicts the effective PLL loop filter. It can be noted that components Ri and Ci are actually parasitic components inside the MC44CD02 chip, nevertheless it is important to take them into account to be able to correctly predict the PLL behavior.

The choice of the loop bandwidth is mainly driven by phase noise, spur rejection considerations and stability. The major constraint is the integrated noise over the OFDM bandwidth 1kHz-3.8MHz (as we can consider that the VCO will dominate the noise at 1.45 MHz offset). The PLL acts as a high pass filter for VCO noise, while adding its own noise source in its band (mainly charge pump and reference oscillator). The higher the PLL bandwidth is, the more the PLL in-band noise sources contribute to the overall integrated noise, while VCO noise contribution decreases. The choice of the charge pump gain is therefore closely related to the PLL bandwidth and noise.

The PLL bandwidth must be sufficiently low to ensure a good rejection of the reference frequency spurs, falling into the OFDM bandwidth (at 1/6 MHz offset from carrier and harmonics). The level of those spurs will also be directly correlated to the quality of the matching between the up and down current sources of the charge pump.The target loop bandwidth has been set to 20kHz typical.

Lock time must also be considered for the choice of the PLL bandwidth.

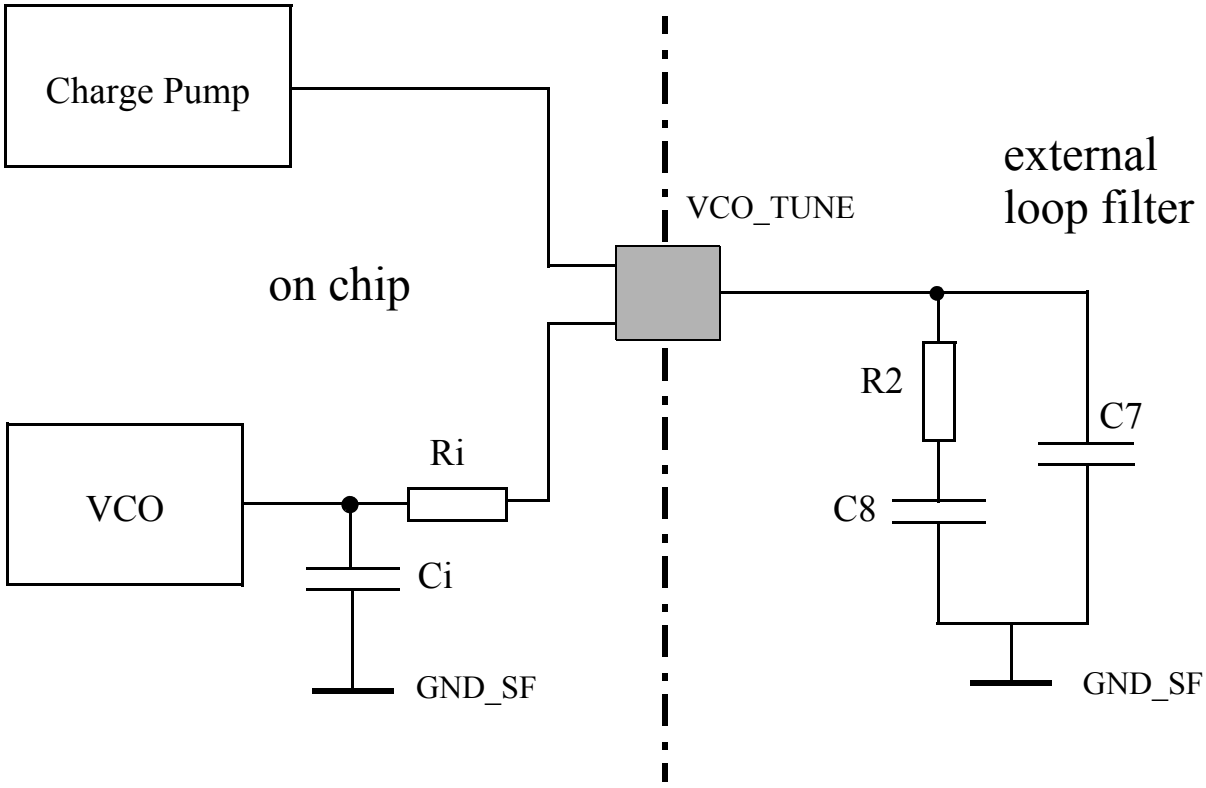

Figure 4-5 Effective PLL Loop Filter Schematic

4.7.3 Deep Sleep & Power Down Mode

The PLL module presents two different behaviours either when the IC is in Power Down mode or in Deep Sleep mode.

In Power Down mode (ENABLE (pin 26) is held at logic high and the PDM bit (in the MODE register at I2C address $00) is asserted, all the PLL blocks (charge-pump, frequency dividers, phase detector, VCOs...) are powered OFF, while the Superfilter providing the power supply to the VCOs remains active. The resulting current consumption under VCC_PLL is less than 1µA, while the current consumption under VCC_SF is around 400µA in typical conditions.

In Deep Sleep mode (ENABLE (pin 26) is held at logic low), all the PLL blocks are powered OFF. The resulting current consumption under VCC_PLL is less than 1µA, while the current consumption under VCC_SF is less than 1.5µA.

4.8 REM Functional Description

4.8.1 General

The purpose of this section is to detail the REM module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.8.2 Normal Mode

The Normal mode corresponds to the REM operating in the receive chain in a regular manner.

This block contains a bandgap voltage reference whose buffered output, vrbg, will be distributed inside the chip as required by other blocks. The limited drive capability of the buffer only permits low currents to be drawn (1uA maximum per user).
The bandgap voltage is also used to generate currents defined by an external resistor connected to pin 41 (REF_CUR). Those currents are then provided to some other blocks of the circuit.

4.8.3 Deep Sleep & Power Down Mode

The REM module will be in low power mode (current consumption <0.5µA) when

- ENABLE (pin 26) is held at logic low.
- ENABLE is held at logic high and the PDM bit (in the MODE register at I2C address $00) is asserted.

4.9 LOP Functional Description

4.9.1 General

The purpose of this section is to detail the LOP module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.9.2 Normal Mode

The Normal mode corresponds to the LOP operating on purpose as a digital output port, driving the output pin #7 LOP. The topology (CMOS output or open drain pull down output) and state of this pin are controlled by the I2C bits LNABO and LNAGS as described below.

LNABO — Topology of the Logical Output Port.
1 = The LOP buffer exhibits an open-drain, pull-down output with 35 Ohms maximum series resistor (large NMOS device connected to ground).
0 = The LOP buffer exhibits a CMOS output made of large devices (35 Ohms maximum series resistance for the NMOS - 120 Ohms maximum series resistance for the PMOS).

LNAGS — State of theLogical Output Port.
1 = pin #7 LOP receives a logical "1".
0 = pin #7 LOP receives a logical "0".

The specific application of this driver is to provide an enabling signal w/wo path to ground to the external LNA of the DVB-H receive system. Exemples of application are described in the Section 5 Initialization/Application Information of this document.

The LOP module is purely digital, draining no current at all, except the current sourced/sinked on the pin #7 LOP depending on the external application circuit.

The supply lines of the LOP module are pin #2 VCC_LNA and pin #6 GND_LNA2.

4.9.3 Deep Sleep & Power Down Mode

As the LOP module is purely digital draining no current at all, no specific Deep Sleep nor Power Down configurations are developped.

Nevertheless, when the MC44CD02 is in power down mode, the LOP module is still activated and maintains its output state if no change is applied on the I2C bits LNABO and LNAGS. It also maintains its output state when recovering Normal mode from Power Down mode.

4.10 MLP Functional Description

4.10.1 General

The purpose of this section is to detail the MLP module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.10.2 Normal Mode

The Normal mode corresponds to the MLP operating as a multi-level pin dedicated to properly configure the MC44CD02 chip and its output clock signal at power on reset, with regards to the reference frequency used (either 26MHz or 36MHz) and the baseband demodulator IC clock input requirements.

The pin #37 CLK_SEL is a 4-level pin that makes use of an internal 240kOhms pull-up resistor, and three analog comparators (three comparison thresholds), resulting in four different chip configurations. The four typical DC levels to be applied on pin #37 CLK_SEL, the corresponding external application scheme, and the resulting chip configurations are described in **Table 4-6** below.

Table 4-6 Multi-level Pin Configuration Table

Level #	Typical DC level applied on pin #37	Typical application on pin #37	Resulting Chip configuration
0	0	GROUND	36MHz reference frequency LVDS signal shaping on clock output pins
1	Vcc/3	120 kOhms to GROUND	36MHz reference frequency single-ended signal shaping on clock output pins
2	2Vcc/3	470 kOhms to GROUND	26MHz reference frequency LVDS signal shaping on clock output pins
3	Vcc	VCC or Open	26MHz reference frequency single-ended signal shaping on clock output pins

As the enable signal is applied on pin #26 ENABLE, the multi-level pin module configures the MC44CD02 chip according to the DC input level applied on pin #37.

The MLP module is made of comparators draining very low current when activated (few µA).

The MLP module forces the configuration of the MC44CD02 chip as long as the I2C bit PADCTRL (reg $05) is forced low.
As the I2C bit PADCTRL is forced high, priority is given to the I2C bits REFCLK (reg $01) and CLKBUF (reg $05) to turn the MC44CD02 chip and its clock outputs according to the application requirements (see the I2C Communication and Register chapters for more details).
The reset state of bit PADCTRL is 0.

4.10.3 Deep Sleep & Power Down Mode

There is no power down mode for multi-level pin MLP module. When the MC44CD02 chip is in Power Down Mode PDM (ENABLE pin is held at logic high, and I2C bit PDM reg$00 is asserted), the multi-level pin MLP module has the exact same functionality than in Normal Mode.

In deep-sleep mode (pin #26 ENABLE is held at logic low), the MLP module is disabled, and drains less than 0.5µA.

Section 5 Initialization/Application Information

This section provides stepwise instructions for initializing and exploiting the MC44CD02 Chip.

5.1 Reset Sources

1. VCC_LOGIC Voltage Monitor. The level sensitive VCC_LOGIC under-voltage detector supervises the CMOS control logic of the I2C sub-module. The detector circuit cannot be disabled and thus guarantees stable register content and hazard free logic operation.
2. External Reset. In case the RST pin is bonded out, this pin can be driven high by overriding the internal pull-down resistance, then the internal reset signal is asserted. This functionality is mainly provided for test and evaluation purposes.

5.2 Application Information

5.2.1 Application Schematic

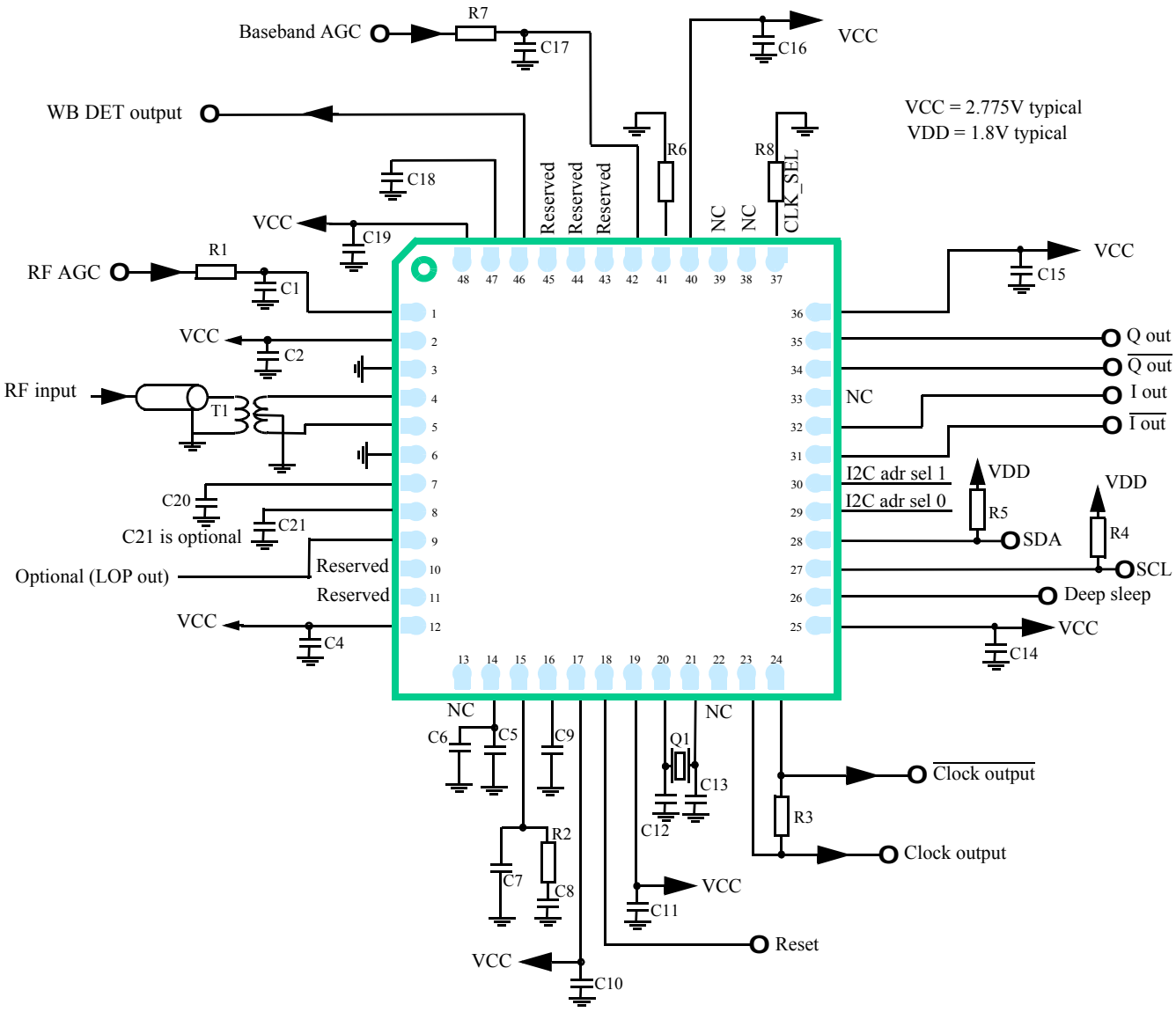

Figure 5-1 MC44CD02 Application Schematic (differential reference clock mode)

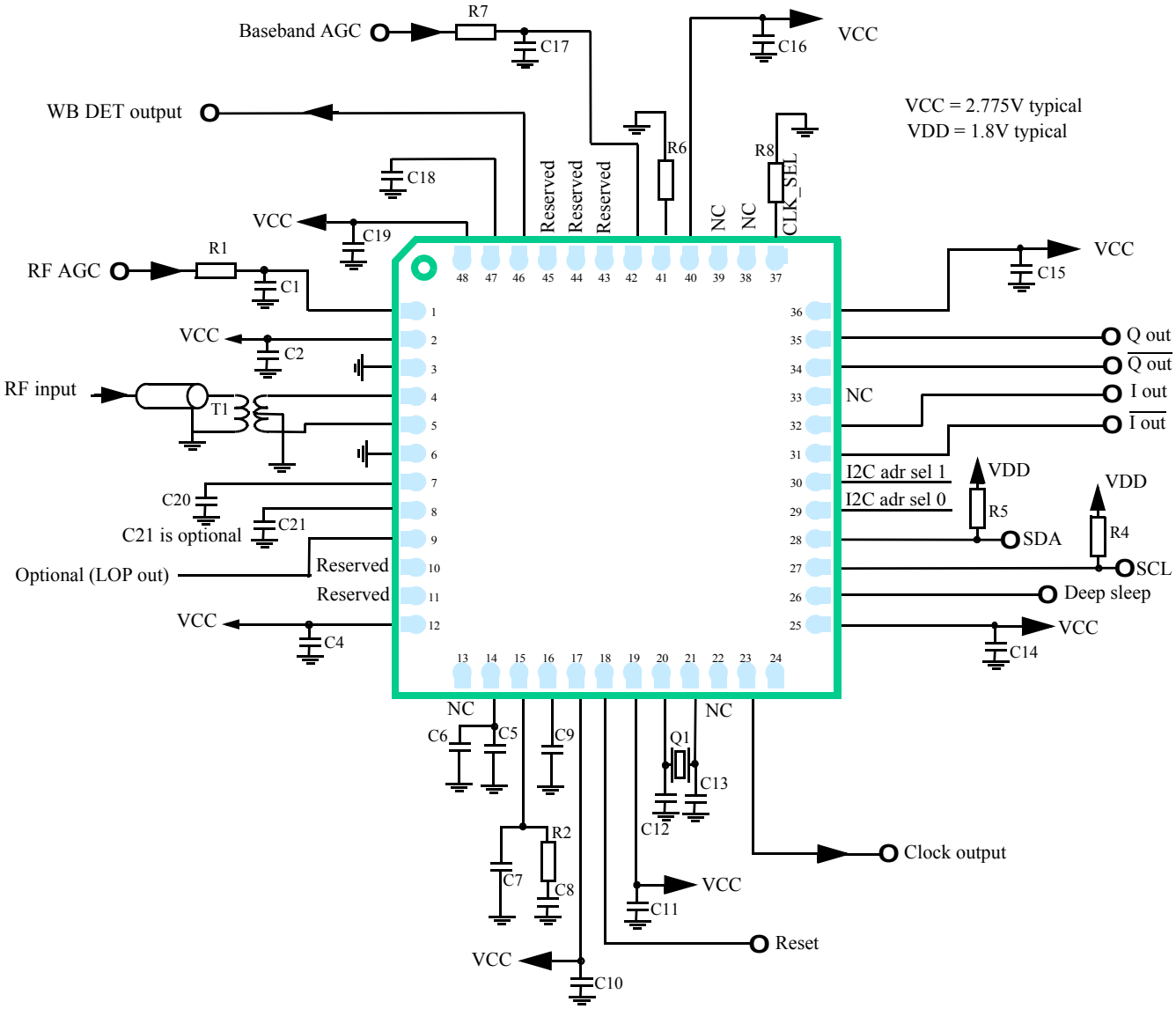

Figure 5-2 MC44CD02 Application Schematic (single ended reference clock mode)

5.2.2 Bill Of Material

Table 5-3 MC44CD02 Typical Application BOM

Part number	Value	Description
C1	22nF	LNA AGC PWM filter capacitor
C2	100nF	VCC LNA decoupling capacitor
C4	100nF	VCC PLL decoupling capacitor
C5	4µ7F	Super-Filter Output filtering capacitor (1)
C6	47nF	Super-Filter Output filtering capacitor (2)
C7	220p	RF PLL loop filter capacitor
C8	1n5	RF PLL loop filter capacitor
C9	4µ7	Super-Filter Bypass filtering capacitor
C10	100nF	VCC Super-FIlter decoupling capacitor
C11	100nF	VCC OSC decoupling capacitor
C12	12pF	Crystal oscillator tuning capacitor
C13	12pF	Crystal oscillator tuning capacitor
C14	100nF	VCC LOGIC decoupling capacitor
C15	100nF	VCC BUFF decoupling capacitor
C16	100nF	VCC BB decoupling capacitor
C17	22nF	Baseband AGC PWM filter capacitor
C18	47nF	Wideband detector time constant capacitor
C19	100nF	VCC Mixer decoupling capacitor
C20	1nF	RF decoupling cap 1
C21	1nF	RF decoupling cap 2
R1	10kΩ	LNA AGC PWM filter resistor
R2	18K	RF PLL loop filter resistor
R3	510R	LVDS external load resistor
R4	4.7kΩ to 47kΩ	SCL line pull-up (if required)
R5	4.7kΩ to 47kΩ	SDA line pull-up (if required)
R6	18kΩ 1%	Current reference resistor
R7	10kΩ	Baseband AGC PWM filter resistor
R8	see configuration table	Multi-level pin resistor for reference frequency and clock buffer configurations
Q1	36MHz or 26MHz	Crystal NX3225 DA (NDK)

Table 5-3 MC44CD02 Typical Application BOM

Part number	Value	Description
T1	UHF Balun	1:4 ratio RF transformer
IC1	MC44CD02	RF Front-End IC

5.2.3 Applications Recommendations

5.2.3.1 RF Inputs

The balanced RF inputs of the device require an external transformer or balun in order to do the impedance conversion and the additional voltage gain. As the inputs are 200Ω specified the external transformer will have a 4:1 impedance ratio (2:1 voltage gain).It is possible to use an RF transformer with 2 windings and a central tap (type 1) or an RF balun (type 2).
In the first configuration (type 1) the RF outputs (pins 2 and 4) are DC coupled to the input of the RF IC and the central tap is grounded.
In the second configuration (type 2) the RF inputs of the balun have to be AC coupled to insulate the DC from the inputs. The RF outputs (secondaries) of the balun are DC coupled to the device.
The choice between both types will depend on the required performance, availability and cost.
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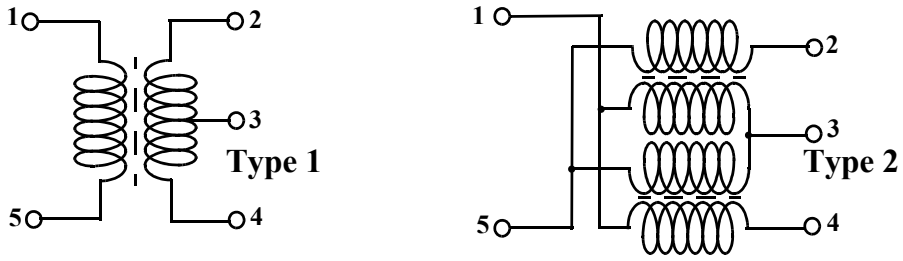

Figure 5-4 Transformer With Center Tap, Transformer Balun

5.2.3.2 I And Q Baseband Outputs

The I/Q output signals are provided by output buffers for driving purposes. The I/Q signals must fulfill the following requirements:

- differential signal amplitude: 1.4Vpp maximum;

- Baseband differential input resistance: 10kOhms minimum;

- Baseband input capacitance: 5pF maximum;

All I/Q outputs can be either AC or DC coupled to the baseband demodulator. For a DC coupling the output common mode voltage of the IC is about Vcc/2 which represents about 1.38V. Both outputs have the same common mode voltage.

The DC coupling mode depends on the electrical specifications of the input ADC of the demodulator.

It is recommended to implement a simple RFI filter at the ADC input. A simple RC combination is sufficient in this case but the structure and the cut off frequency depend on the application (PCB layout, proximity of the RFIC and demodulator, noise, clock parasitic, etc....).

The common mode voltage of the IQ differential outputs does not change with the gain and is tracked in temperature and process variation by an internal DC loop.

This DC loop is equivalent to a first order high pass filter and has a cut off frequency of about 700 Hz typical with a maximum of 1 KHz. This cut off frequency induces a notch in the OFDM carrier distribution but is negligible in term of BER degradation.

Of course it is possible to use a AC coupling between the device and the demodulator.

5.2.3.3 Decoupling And Power Distribution

All supply voltage pins of the device (including the SF_OUT and SF_BYP pins) have to be decoupled as close as possible of the device. It is recommended to provide a ground plane that will be directly connected to the exposed pad. The exposed pad of the device is the main ground.

Some sensitive parts (PLL loop filter pin 15, Wide band detector capacitor pin 47, crystal oscillator pins 20 and 21) have also to be placed close to their corresponding pins.

The RF inputs (pins 4 and 5) must be routed carefully taking into account the external transformer or balun. The differential clock outputs must be routed symmetrically to the baseband demodulator.

5.2.3.4 Crystal Oscillator

The target crystal device is the 36MHz or 26MHz NX3225DA sub-miniature part from the NDK company. Reference [3] gives access to the specifications of this device but **Table 5-5** summarizes the characteristics of this quartz.

Table 5-5 NDK NX3225DA Quartz Characteristics

Preliminary Reference	NX3225DA 36MHz W-191-563 or 26MHz W-191-653
Nominal Frequency	F_0 = 36MHz or 26MHz
Resonating Mode	Fundamental
Frequency Tolerance @ 25°C	+/- 10 ppm maximum
Recommended Temperature Range	-20 to +70°C
Functioning Temperature Range	-20 to +85°C
Frequency Stability in the -20 - 70°C temperature range	+/- 10 ppm maximum
CL, Loading Capacitor[1]	8pF

NOTES:

1. If Cc is the total capacitance across the crystal (dominated by the case capacitance), If Cte and Ctx are the values of the tuning capacitors plus any stray contributors between respectively the EXTAL or XTAL pin and ground, then CL = Cc + Cte*Ctx/(Cte+Ctx). If Cte=Ctx then CL = Cc + Cte/2

5.2.3.5 Using an external reference frequency

Instead of using the crystal oscillator, it is possible to provide the 36MHz or 26MHz reference clock to the chip through the EXTAL pin (pin #17). The application schematic is described in **Figure 5-6**.
The reference clock can be provided as a sine wave clock for harmonic content reduction, or as a rail-to-rail 1.875V or 2.775V digital clock. In any case, the clock must present sufficient amplitude, adequate duty-cycle, and very low jitter, so as not to impact chip functionality nor PLL phase noise performances. The detailed specifications related to this external reference clock are provided in the OSC Electrical Specifications chapter of this document.
The device has its own internal bias on the EXTAL pin, so the external sine wave reference clock must be AC biased through an external capacitor. This capacitor is not needed in case of rail-to-rail digital clock.

The selection of the reference clock frequency value (26 or 36MHz) is either controlled by the multi-level pin#37 CLK_SEL, or by the I2C bus, as described in the dedicated paragraph «Reference clock frequency and clock output buffer selection» below.

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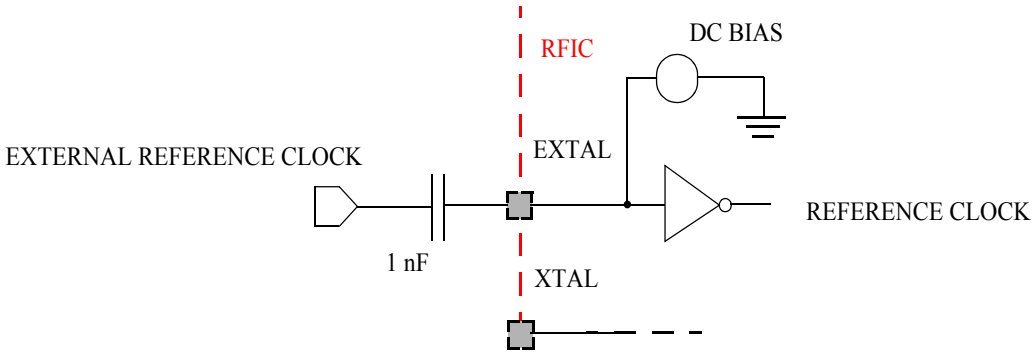


Figure 5-6 Driving the EXTAL pin with an external reference clock

5.2.3.6 Providing the reference crystal clock to the baseband demodulator

To reduce the number of crystals of the whole receiver solution, it is possible to output the reference crystal oscillator clock to the baseband demodulator. There are 2 main configurations, that cannot be used simultaneously.

The first one uses a differential mode to get a better immunity to the common mode parasitic signals. In this case the chip provides the 36 or 26 MHz differential output currents on its output pins #23 CLK_OUT and #24 CLK_OUTB. The signal swing is generated through a load consisting of an external differential resistor. Two different current settings can be programmed through the I2C bit ILVDS. The custom LVDS swing is developed around a common mode level that is derived from a bandgap voltage sufficiently accurate to avoid the use of any common mode control loop. The custom LVDS buffer can be disabled by setting the I2C bit CLKDD to high logic level.

The second one uses the single ended mode. In that case, the chip provides the 36 or 26MHz output signal on the output pin #23 CLK_OUT. The output signal is either 1.8V CMOS shaped as the I2C bit ILVDS is

set to 1, or 1.5Vpp analog-like as the I2C bit ILVDS is set to 0. The single-ended buffer can be disabled by setting the I2C bit CLKDD to high logic level.

The selection of the reference clock frequency value (26 or 36MHz) as well as the selection of the clock buffer mode (LVDS or single-ended) is either controlled by the multi-level pin#37 CLK_SEL, or by the I2C bus, as described in the dedicated paragraph «Reference clock frequency and clock output buffer selection» below.

5.2.3.7 Reference clock frequency and clock output buffer configuration

At power on reset, a proper setting of the IC with regards to the reference clock frequency is suitable to fit the application requirements. Particularly, a correct power on reset configuration of the clock output signal is required, as this signal is potentially used to wake-up and clock the baseband demodulator IC.

Therefore, a multi-level pin (pin #37 CLK_SEL) is dedicated to adequately preset the MC44CD02 chip and its clock output signal in the configuration required by the application.
The selection of both the reference clock frequency (either 26 or 36MHz) and the clock output buffer mode (either LVDS or single-ended) is be done by adjusting the value of the external resistor connected to pin#37 CLK_SEL according to **Table 5-7**.

Table 5-7 Multi-level Pin Configuration Table

External resistor value (pull-down) on pin#37 CLK_SEL	Typical DC level on pin#37 CLK_SEL	Clock mode selected
Vcc or Open	Vcc	26MHz reference clock frequency single-ended clock buffer
470 K	2Vcc/3	26MHz reference clock frequency LVDS clock buffer
120 K	Vcc/3	36MHz reference clock frequency single-ended clock buffer
GND	0	36MHz reference clock frequency LVDS clock buffer

When single-ended mode is chosen, the format is square wave at start-up (I2C bit ILVDS=0 in reg $05), this allows making sure that the BB chip will wake-up. The shape can then be programmed to sine wave if desired (ILVDS=1).Similarly, when LVDS mode is chosen, the LVDS current is set to 500uA at start-up (ILVDS=0). This can be modified to 1mA via I2C (ILVDS=1).

Priority can be given to the I2C to select the reference clock frequency and the clock buffer mode by asserting the I2C bit PADCTRL to 1 (reg $05). In that case, the control is given to the I2C bits REFCLK (reg $01) and CLKBUF (reg $05).
At power on reset, the value of this PADCTRL bit is 0, such as the priority is left to the multi-level pin#37 CLK_SEL.

5.2.3.8 PLL Loop Filter Calculation

The 3rd order PLL uses an external 2nd order loop filter as described in **Figure 5-8**.

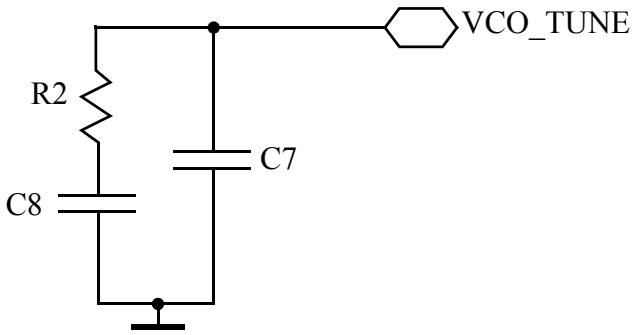


Figure 5-8 External 2nd Order Loop Filter

The choice of the loop bandwidth is mainly driven by phase noise and spur rejection considerations. The major constraint is the integrated noise over the OFDM bandwidth 1 kHz -3.8MHz (as we can consider that the VCO only will dominate the noise at 1.45 MHz offset). The PLL acts as a high pass filter for VCO noise, while adding its own noise source in its band (mainly charge pump and reference oscillator). The higher the PLL bandwidth, the more the PLL in-band noise sources contribute to the overall integrated noise, while VCO noise contribution decreases. The choice of the charge pump gain is therefore closely related to the PLL bandwidth.

The PLL bandwidth must be sufficiently low to ensure a good rejection (to be defined) of the reference frequency spurs, falling into the OFDM bandwidth (at 1/6 MHz offset from carrier and harmonics). The level of those spurs will also be directly correlated to the quality of the matching between the up and down current sources of the charge pump.

Lock time must also be considered for the choice of the PLL bandwidth.

5.2.3.9 RF And Baseband AGC

The AGC inputs of the device (both RF and Baseband BB) are controlled by the baseband demodulator via a PWM filtering network (RC combination). This combination is intended to filter the pulse modulation that operates at the system clock level of the demodulator.

The recommended combination is R = 10K and C = 22 nF

5.2.3.10 Wideband Detector Response Time Calculation

The charging time and discharging slew rate are defined by the internal current sources and the external capacitor (pin 47). The voltage swing on the pin 47 is 2.5 V.

With a recommended capacitor of 47nF and a discharging current of 25 uA, the discharging time is then 4.7 ms. For a charging current of 800 uA and the same capacitor the charging time is 150 us.

Of course both times can be adjusted in the application by the value of the capacitor and will depend on the required response time in presence of PAL or DVB-T interferers in the whole UHF band.

Furthermore it is possible to adjust the ratio between the charging time and the discharging time by I2C bus. This option is important to adjust this ratio according to the different scenarii, for instance a PAL interferer versus a DVB-T interferer. The charging current can be adjusted between 680 and 960 uA with a nominal value at 800 uA. The discharging current can be adjusted between 10 and 40 uA with a nominal value at 25 uA.

5.2.3.11 Controlling The Gain Of An External LNA Using the LOP Pin

Most of the modern LNA integrated circuits have digital control of their gain and standby/linearity modes, such as recommended Freescale MBC13720, originally designed for cellular applications up to 2GHz, that has demonstrated efficiency in this DVB-H application.

In that case, LOP pin is used in CMOS mode (register $06, bit LNABO=0) and LNAGS bit in the same register is used to control operating mode (high/low gain, high/low linearity, standby...).

With other LNA devices without digital control pins, it is possible to use LOP output in open-drain configuration with a moderate bias current as shown in **Figure 5-9**. In that configuration, user has to be careful to switching time and polarity of the LNAGS bit.

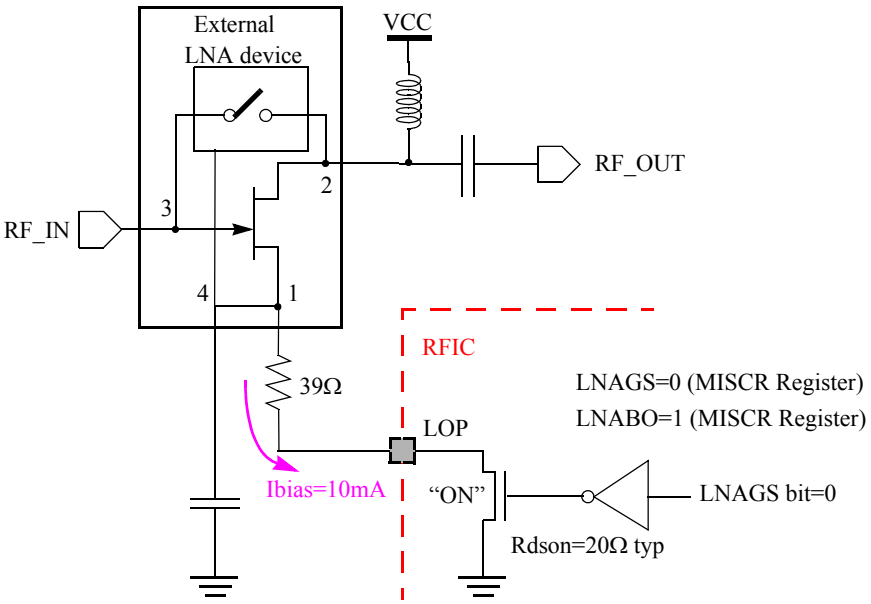


Figure 5-9 Controlling The Gain Of An External LNA

Section 6 References

[1] EICTA-TAC-MBRAI: Mobile DVB-T RF Specification.

[2] Digital Video Broadcast (DVB); Framing Structure, channel coding and modulation for digital terrestrial television. ETSI EN 300 744 V.1.4.1 January 2001.

[3] NDK specifications for the W-191-563 36MHz quartz, case NX3225DA. Document reference EXS11B-00775.

[4] Philips I2C Specifications Version 2.1 January 2000. Document Order Number 9398 393 40011.

Appendix A Electrical Specifications

A.1 MC44CD02 Thermal Specifications

Table A-1 Thermal Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient[1]	RΘJA	Free air		82		°C/W

NOTES:
1. As per JEDEC EIA/JESD51-2.

A.2 MC44CD02 Moisture Sensitivity Level Consideration

The device meets moisture sensitivity level 3 (lead-free reflow profiles with peak temperature of 260°C).

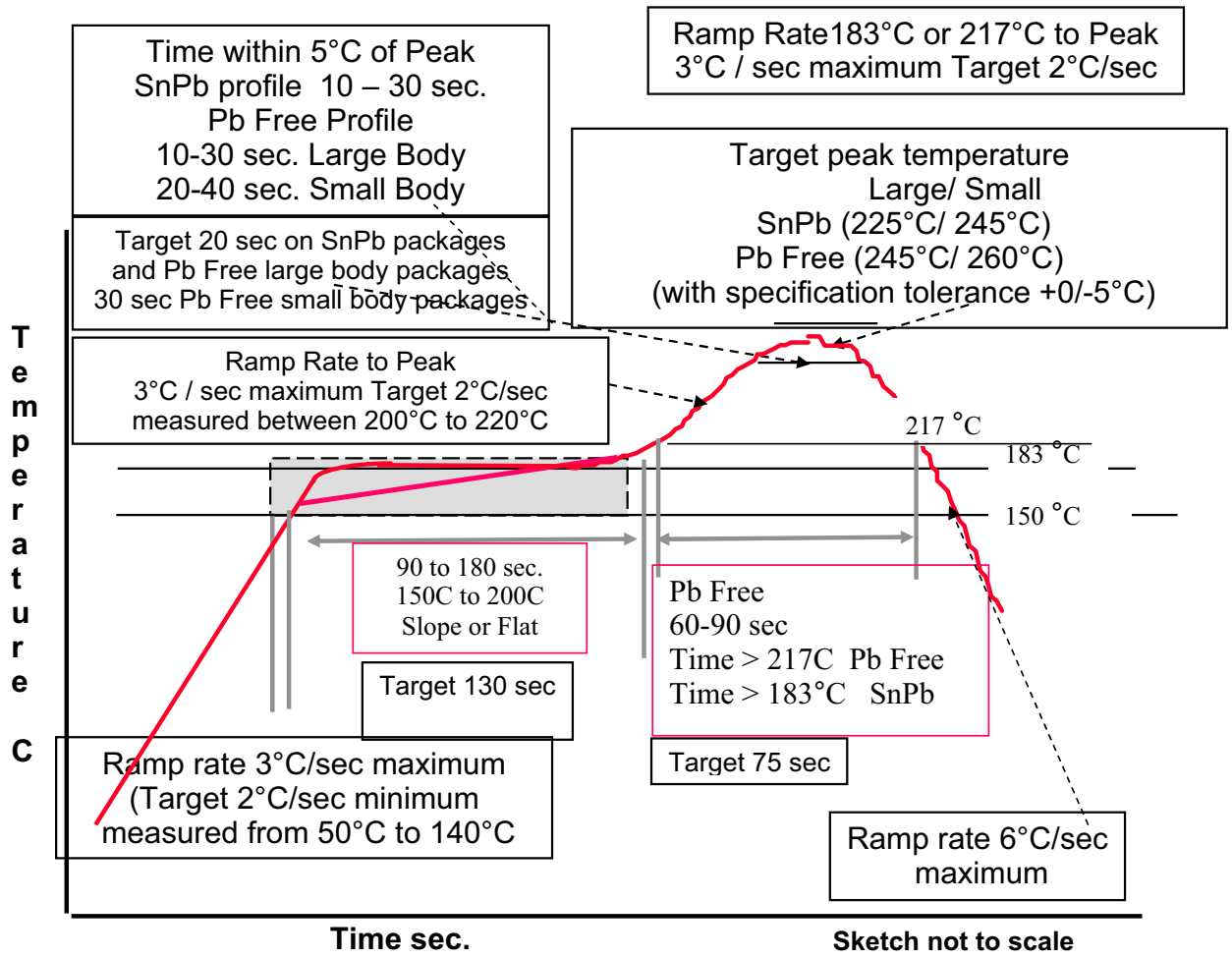


Figure 6-1 High temperature reflow profile

A.3 MC44CD02 ESD Specifications

Table A-2 ESD Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Machine Model ESD	ESD MM	JEDEC JESD22-A115	200			V
Human Body Model ESD	ESD HBM	JEDEC JESD22-A114	2000			V
Charge Device Model ESD	ESD CDM	JEDEC JSED22-C101C	500			V

A.4 General MC44CD02 Electrical Specifications

Unless otherwise noted all specifications are given for a supply voltage set to 2.775V and an operating temperature TA=-30 to +85°C. The correspondence between the type associated with a parameter and the specification method is given below:

- A = 100% tested
- B = 100% correlation tested
- C = Characterized on samples
- D = Guaranteed by design or technology

Table A-3 Electrical specifications and maximum ratings

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
	Supply Voltage	2,12,17, 19,25,36 ,40,48		2.63	2.775	2.92	V	C
	Supply Voltage Max Rating[1]	2,12,17, 19,25,36 ,40,48				3.15	V	D
	Power Consumption	2,12,17, 19,25,36 ,40,48	Normal Mode[2]		270		mW	B
	Operating Temperature			-30		85	°C	C
	Storage Temperature			-65		150	°C	D
1.1	Normal Operation Current	2,12,17, 19,25,36 ,40,48	Normal Mode		98	110	mA	A
1.2	Power Down Current	2,12,17, 19,25,36 ,40,48	Power Down Mode[3]		3.5	4.2	mA	A

Table A-3 Electrical specifications and maximum ratings

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
1.3	Deep Sleep Current	2,12,17, 19,25,36 ,40,48	Deep Sleep Mode[4]			20	µA	A
1.5	Line Regulation	2,12,17, 19,25,36 ,40,48	GSM Slot			1	mV	D
1.6	PSRR	2,12,17, 19,25,36 ,40,48	GSM Slot (about 1.8kHz)	40			dB	D
1.7	IC Wake-up Time from power down		Conditions[5]		5	20	ms	C
1.8	IC Wake-up Time from deep sleep		Conditions[6]		6	200	ms	C

NOTES:

1. Maximum ratings are those values beyond which damage to the device may occur. For functional operation, voltage should be restricted to the Recommended Operating Condition.
2. ENABLE Pin at Vcc level. PDM bit cleared in the MODE register (address $00).
3. ENABLE Pin at Vcc level. PDM bit set in the MODE register (address $00).
4. ENABLE pin grounded.
5. Definition of the setup: measured at I/Q outputs when reaching 90% of the final amplitude.
6. Definition of the setup: measured at I/Q outputs when reaching 90% of the final amplitude.

A.5 MC44CD02 RF Performances

The RF path between the UHF antenna and the MC44CD02 chip includes:

- An external single-ended LNA with the following characteristics:
  - Power gain: G = +10dB
  - Noise figure: NF = +3.5dB
- A transformer (balun) 2:1 with 50Ω input impedance and center tap, providing the single-ended to differential transformation with a voltage gain of 2X as well as the impedance conversion (50Ω το 200Ω) required to drive the MC44CD02's differential RF inputs.

Table A-4 describes the general receiver specifications, derived from the DVB-T/H standard specifications.

WARNING

The reference point for all the specifications displayed in Table A-4 is the antenna (external LNA input). The typical LNA characteristics indicated above are then assumed. This reference point is changed to the IC (internal LNA) inputs in Table A-5.

Unless otherwise noted all specifications are given for a supply voltage set to 2.775V and an ambiant temperature TA=-30 to +85°C.

Table A-4 DVB Receiver RF Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit
2.1	RF Input Range	4,5	UHF Band IV & V	470		862	MHz
2.2	Max. Total Input Level	4,5		-25			dBm
2.3	Input Sensitivity	4,5		-95			dBm
2.4	Backstop Noise	4,5		33			dBc
2.5	Overall Maximum Gain[1]	4,5		89			dB

NOTES:
1. PMAG[1:0]=11 in the MISCR register.

Table A-5 MC44CD02 RF Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
3.1	Noise Figure	4,5	Max Gain		9	10	dB	C
3.2	Input IP2[1]	4,5	See **Table A-7**	40			dBm	C
3.3	Input IP3[2]	4,5	See **Table A-6**	6	7		dBm	A
3.4	Overall AGC Range	4,5	Both RF & BB AGC	70	75		dB	A
3.5	Return losses	4,5				7	dB	D

Table A-5 MC44CD02 RF Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
3.10	Overall Maximum Voltage Gain[3]	4,5	Without external balun	73			dB	A
3.11	Max. Total Input Level	4,5		-15			dBm	D
3.12	Input Sensitivity	4,5		-85			dBm	C
3.13	Noise Figure degradation in presence of strong interferer[4]	4,5	Any gain condition			3	dB	C
3.14	1dB Compression Point[5]	4,5		-3			dBm	C
3.15	LO leakage	4,5	Measured at balun[6] input from 1896MHz to 3432MHz			-30	dBm	C

NOTES:
1. Measured with -20dB RF LNA gain reduction and maximum baseband gain.
2. Measured with -20dB RF LNA gain reduction and maximum baseband gain.
3. PMAG[1:0]=11(b) in the MISCR register. Without external balun.
4. Single -25dBm N+i UHF channel interferer.
5. Measured with -20dB RF LNA gain reduction and maximum baseband gain.
6. Balun TDK HHM1589B1

Table A-6 Input IP3 Measurement Conditions

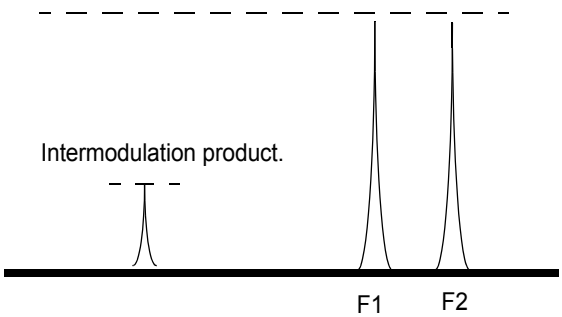
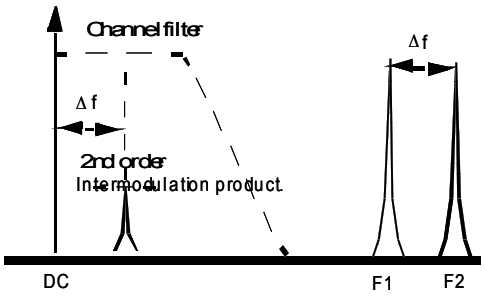
Device & Signals Set-up	Measurements Set-up
2-tone measurements at low, medium and high UHF band. The intermodulation product falls back in the wanted UHF channel. Conditions: RF inputs @ -30 dBm. -20 dB RF LNA gain reduction. The RF PLL is tuned on the central frequency of the corresponding DVB-T channel. Low UHF, F1 = 487.25 MHz, F2 = 503.25 MHz that gives an intermodulation product at 471.25 MHz that corresponds to the vision carrier of the channel 21. Mid UHF, F1 = 631.25 MHz, F2 = 647.25 MHz that gives an intermodulation product at 663.25 MHz that corresponds to the vision carrier of the channel 45. High UHF, F1 = 823.25 MHz, F2 = 839.25 MHz that gives an intermodulation product at 855.25 MHz that corresponds to the vision carrier of the channel 69.	

Table A-7 Input IP2 Measurement Conditions

IIP2	
Device and Signals Set-up	Measurement Set-up
2-tone measurements at low, medium and high UHF band. The parameter represents the leakage of the mixer. The 2 signals F1 and F2 mix with each other to generate a distorsion component inside the useful baseband bandwidth. In this case the LO is programmed out of this region to avoid any direct down mixing product. Only the leakage F1-F2 is measured at the output. Conditions: RF inputs @ -30 dBm. -20 dB RF LNA gain reduction. Low UHF, F1 = 477.25 MHz, F2 = 479.25 (that corresponds to the vision carrier of the channel 22 MHz). This gives a 2nd order intermodulation product at 2 MHz. The LO is set to 666 MHz. Mid UHF, F1 = 661.25 MHz, F2 = 663.25 MHz (that corresponds to the vision carrier of the channel 45). This gives a 2nd order intermodulation product at 2 MHz. The LO is set to 858 MHz. High UHF, F1 = 853.25 MHz, F2 = 855.25)that corresponds to the vision carrier of the channel 69 MHz). This gives a 2nd order intermodulation product at 2 MHz. The LO is set to 474 MHz.	

A.6 RFLNA Electrical Specifications

Table A-8 RFLNA Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
3.6	RF AGC Range	1			40		dB	B
3.7	RF AGC Slope	1			+ 35		dB/V	A
3.8	RF AGC Voltage Range	1		0.1		1.8	V	A
3.9	RF AGC Input Impedance	1	Resistor to Supply	400			kΩ	D
3.10	RF AGC Gain variations over reduced temperature range (-10 to 50 C)	4,5		-2	-	+2	dB	C
3.11	RF AGC Gain variations over process and temperature	4,5		-6	-	+6	dB	C

A.7 WBD Electrical Specifications

Table A-9 WBD Performances after required calibration (see section 4.5.3 for procedure)

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
4.1	Input Operating Range	4, 5	See[1]	-60		-30	dBm	A
4.2	Gain[2] at high power[7]	46	See[7]		70		mV/dBm	C
4.3	Output Voltage Range	46		0.1		2.6	V	A
4.4	Charging Current[3]	47		600	836	1000	μA	A
4.5	Discharging Current[4]	47		21	26	32	μA	A
4.7	Error[10] over temperature at high power[7]	46	See[7]			1	dBm	C
4.8	Error[10] over temperature at low power[8]	46	See[8]			4	dBm	C
4.9	Error[10] over Process/Supply at high power[9]	46	See[9]			2.5	dBm	C
4.10	Gain at minimum input power[11]	46	See[10]	7			mV/dBm	A

NOTES:
1. Measured at RF inputs with maximum LNA gain.
2. Adjustable using the DETGAIN[2:0] bits in the WBDCR2 register at address $04.
3. Measured with default register value. Adjustable using the ICHG[2:0] bits in the WBDCR1 register at address $03.
4. Measured with default register value. Adjustable using the IDISCHG[2:0] bits in the WBDCR1 register at address $03.
7. Temperature range is -10 to +50 deg C, Power range is -30dBm to -10dBm referred to WBD inputs.
8. Temperature range is -10 to +50 deg C, Power range is -40dBm to -30dBm referred to WBD inputs.
9. Power Range is -30dBm to -10dBm referred to WBD inputs. Calibration using WBD I^2C bits required.
10. Defined as (Maximum Indicated Power-Minimum Indicated Power)/2, since WBD input power is not measured.
11. Minimum input power is -40dBm referred to WBD inputs.

A.8 MIXER Electrical Specifications

Table A-10 MIXER Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
11.1	RF Input Frequency Range			470		862	MHz	B
11.2	LO Input Frequency Range			470		862	MHz	B

A.9 PMA Electrical Specifications

Table A-11 PMA Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
12.1	Maximum Voltage Gain		PMAG[1:0]=00[1]		14		dB	B
12.2	Intermediate Voltage Gain		PMAG[1:0]=10		12		dB	B
12.3	Minimum Voltage Gain		PMAG[1:0]=01		10		dB	B
12.4	Voltage Gain Step size			1.5	2	2.5	dB	A

NOTES:
1. Reset value.

A.10 LPF Electrical Specifications

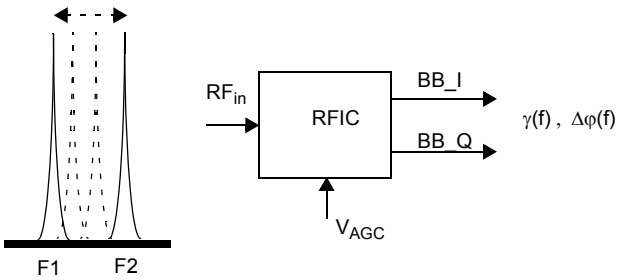
Table A-12 LPF Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
5.1	Attenuation for 8 MHz channel	31, 32, 34, 35	@ 3.8MHz		1	5	dB	A
5.2	Attenuation for 7 MHz channel	31, 32, 34, 35	@ 3.33MHz		1	5	dB	A
5.3	Attenuation for 6 MHz channel	31, 32, 34, 35	@ 2.85MHz		1	5	dB	A
5.4	Stopband Attenuation	31, 32, 34, 35	@ 5.7MHz	40			dB	A
5.5	PAL Rejection	31, 32, 34, 35	@ 5.25MHz	29			dB	A
5.51	Anti Aliasing Rejection	31, 32, 34, 35	@ 11.2MHz	65			dB	A
5.6	Group Delay	31, 32, 34, 35			400	700	ns	D
5.7	In-band Ripple	31, 32, 34, 35				2	dB	A
5.8	Constant IQ Gain Imbalance	31, 32, 34, 35		-3		3	dB	A
5.9	Constant IQ Phase Imbalance	31, 32, 34, 35		-10		10	degree	A
5.10	Frequency dependant IQ Gain and Phase Imbalance	31, 32, 34, 35	See **Table A-13**			-35	dBc	A
5.11	AC Coupling Cut-off	31, 32, 34, 35	@ -3dB			1	kHz	C
5.12	Output DC Offset	31, 32, 34, 35		-100		100	mV	A
5.13	Output Voltage Range	31, 32, 34, 35	Differential			700	mVp	C
5.15	Output DC Level	31, 32, 34, 35		1.1	1.4	1.7	V	A
	Baseband AGC							
6.1	Total BB AGC Range	42		35			dB	A
6.2	AGC Input Voltage Range	42		0.1		1.8	V	A

Table A-12 LPF Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
6.3	BB AGC Slope	42			+ 35		dB/V	B
6.4	AGC Input Impedance	42		400			kΩ	D
6.5	BB AGC Gain variations over reduced temp. range -10°C to 50°C			-1		1	dB	C
6.6	BB AGC Gain variations over process and temperature			-6		+6	dB	C

Table A-13 IQ Gain/Phase Imbalance Contribution to S/N Degradation

Device & Signals Set-up	Measurements Set-up
Sweep tone measurement of total IQ amplitude and phase imbalance (constant and ripple) for three different RF input signals: Low UHF: From F1 to F2 = 474 to 478 MHz Medium UHF: From F1 to F2 = 666 to 670 MHz High UHF: From F1 to F2 = 858 to 862 MHz and for three different baseband AGC settings: Low gain: minimum baseband gain Medium gain: (max. gain - min. gain)/2 High gain: maximum baseband gain Detecting the amplitude $\gamma(f)$ and phase $\Delta\varphi(f)$ difference between baseband I- and Q- outputs. Calculating mean value, deviation and interference variance according to: $$\varepsilon(f) = \frac{\gamma(f)-1}{\gamma(f)+1}$$ $$\sigma_\varepsilon = \sqrt{\overline{[\varepsilon(f)-\overline{\varepsilon(f)}]^2}}$$ $$\sigma_{\Delta\varphi} = \sqrt{\overline{[\Delta\varphi(f)-\overline{\Delta\varphi(f)}]^2}}$$ Interference variance: $$\sigma^2 = \frac{1}{\sigma_\varepsilon^2 \cdot \left(\cos\left(\frac{\sigma_{\Delta\varphi}}{2}\right)\right)^2 + \left(\sin\left(\frac{\sigma_{\Delta\varphi}}{2}\right)\right)^2}$$	

A.11 OSC Electrical Specifications

Unless otherwise noted, the following specifications assume the proper mounting of a 36MHz or 26MHz NDK NX3225DA quartz element, associated with 12pF tuning capacitors.

Table A-14 OSC Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
Crystal Oscillator								
7	Recommended Crystal's: 36MHz NDK 3225 DA reference W-191-563 or 26MHz NDK 3225 DA reference W-191-653							
7.1	Motional Capacitance	20,21			3.99		fF	N/A
7.2	Motional Inductance	20,21			4.8		mH	N/A
7.3	Parallel Capacitance	20,21		0.85	1	1.15	pF	N/A
7.4	Series Resistance	20,21				50	Ω	N/A
7.5	Load Capacitance	20,21			8		pF	N/A
LVDS Outputs[1]								
8.1	Differential Output Clock Current	23, 24	i_lvds_adj = 0 i_lvds_adj = 1	0.375 0.750	0.5 1.0	0.625 1.250	mApk mApk	A
8.2	Common Mode Voltage	23, 24		0.70	0.95	1.30	V	A
8.3	External Load (differential)	23, 24	i_lvds_adj = 0 i_lvds_adj = 1		500 250		Ω	N/A
8.4	Start-up Time	23, 24	See Note[2]			5	ms	C
8.5	Output Clock Duty Cycle	23, 24		45	50	55	%	C
8.6	Output Clock Jitter	23, 24	cycle-to-cycle (1MHz bandwitdh)			35	ps	D
8.7	Maximum Load Capacitance (differential)	23, 24				1	pF	D
Single-ended Buffer Output[3]								
8.8	Output Voltage Swing	23	i_lvds_adj = 0 i_lvds_adj = 1		1.5 [0:1.8]		Vpp CMOS	C
8.9	Common Mode Voltage	23	i_lvds_adj = 0 i_lvds_adj = 1		0.9 NA		V NA	C
8.10	Start-up Time	23	See Note[4]			5	ms	C
8.11	Output Clock Duty Cycle	23		45	50	55	%	C

Table A-14 OSC Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
8.12	Output Clock Jitter	23	cycle-to-cycle (1MHz bandwitdh)			35	ps	D
8.13	Maximum Load Capacitance (differential)	23				5	pF	D
External Reference Clock[5]								
8.14	Reference Clock Frequency	20			36 or 26		MHz	D
8.15	Reference Clock Amplitude	20	AC coupled ?	220			mVrms	D
8.16	Reference Clock Duty-Cycle	20		45		55	%	D
8.17	Reference Clock Jitter	20	cycle-to-cycle integrated from 1kHz to 100kHz			0.5	ps	D
8.18	Reference Clock Phase Noise	20	@ 1kHz offset			-120	dBc/Hz	D

NOTES:

1. The implementation of LVDS inside the MC44CD02 chip does not obey ANSI/TIA/EIA-644. The LVDS buffer is selected as I2C bit CLKBUF=0 in the LNAOSCR $05 register.
2. Measured from assertion of the ENABLE pin to delivery of output clock on the CLK_OUT/B pins.
3. The single-ended buffer is selected as I2C bit CLKBUF=1 in the LNAOSCR $05 register.
4. Measured from assertion of the ENABLE pin to delivery of output clock on the CLK_OUT pin.
5. Specifications as the 36MHz or 26MHz external reference clock is externally provided to the chip through the EXTAL input pin.

A.12 PLL Electrical Specifications

Unless otherwise noted, the following specifications assume the proper mounting of a loop filter made of R2=27 kΩ, C8= 820 pF and C7= 120 pF.

Table A-15 PLL Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
9.2	VCO_TUNE Minimum Voltage[1]	15		0.5			V	A
9.3	VCO_TUNE Maximum Voltage[2]	15				1.7	V	A
9.4	PLL In-band Accumulated Phase Noise 1kHz-3.8MHz					-33	dBc	C
9.5	PLL Phase Noise @ 1.45MHz offset					-125	dBc/Hz	C
9.6	PLL Phase Noise @ 9.45MHz offset					-132	dBc/Hz	C
9.7	Reference Frequency[3]				1/6		MHz	B
9.8	Reference Frequency Spurs @ Fref offset in UHF band					-38	dBc	A

NOTES:
1. Threshold below which the band-switch system will select an alternate VCO and/or sub-band.
2. Threshold above which the band-switch system will select an alternate VCO and/or sub-band.
3. Derived from a 36MHz or 26MHz crystal oscillator.

A.13 REM Electrical Specifications

Table A-16 REM Performances

ID	Parameter	Pin	Conditions	Min	Typ	Max	Unit	Type
1.8	DC operating voltage of the REF_CUR pin	41		1.05	1.11	1.17	V	A

A.14 LOP Electrical Specifications

Table A-17 LOP Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
13.2	LOP Buffer Rise Time[1]	7	CLoad=10pF		3	4	ns	D
13.3	LOP Buffer Fall Time[2]	7	CLoad=10pF		1.5	2.5	ns	D
13.4	LOP Buffer RdsON[3] LNAGS=X / LNABO=1 LNAGS=1 / LNABO=0	7	Iload=5mA sourced sinked			 35 120	 Ω Ω	A

NOTES:
1. LNBAO=0 in the MISCR register. Measured from 10% to 90% output swing.
2. LNBAO=0 in the MISCR register. Measured from 90% to 10% output swing.
3. LNAGS and LNABO in the MISCR register. Static measurement.

A.15 MLP Electrical Specifications

Table A-18 MLP Performances

ID	Parameter DC level on pin#37[1]	Pin(s)	Conditions	Resulting Chip Configuration
13.1	Vdc < (Vcc/6)-100mV	37	PADCTRL=0 (reg $05)	36MHz reference frequency LVDS signal shaping on clock output pins
13.1	Vdc >(Vcc/6)+100mV and Vdc<(Vcc/2)-100mV	37	PADCTRL=0 (reg $05)	36MHz reference frequency single-ended signal shaping on clock output pins
13.1	Vdc >(Vcc/2)+100mV and Vdc<(5Vcc/6)-100mV	37	PADCTRL=0 (reg $05)	26MHz reference frequency LVDS signal shaping on clock output pins
13.1	Vdc >(5Vcc/6)+100mV	37	PADCTRL=0 (reg $05)	26MHz reference frequency single-ended signal shaping on clock output pins

NOTES:

1. DC level on pin#37 CLK_SEL is preferably generated by connecting an external resistor to ground as described in the chapter MLP Functional Description and the chapter Initialization/Application Information of this document.

A.16 RCI Electrical Specifications

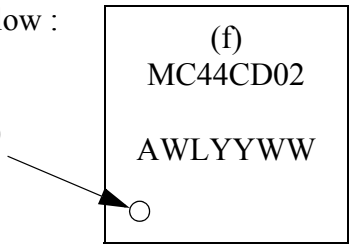
Table A-19 RCI Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
10.1	SDA/SCL Low Input Level	27, 28				0.3	V	A
10.2	SDA/SCL High Input Level	27, 28		1.5			V	A
10.3	ACK Low Output Level	28	Sinking 3mA load current			0.3	V	A
10.4	I2C Communication Speed	27, 28	See Reference [4]			400	kbits/s	A
10.5	Digital Inputs Low Input Level	10,18,26, 29,30		0		0.3	V	A
10.6	Digital Inputs High Input Level	10,18,26, 29,30		1.5		Vcc	V	A
10.7	Digital Inputs Input Capacitance	10,18,26, 29,30			1		pF	D
10.8	RESET Pull-down Resistor	18			120		kΩ	A

Appendix B Marking, Shipping Instructions & Case Outline

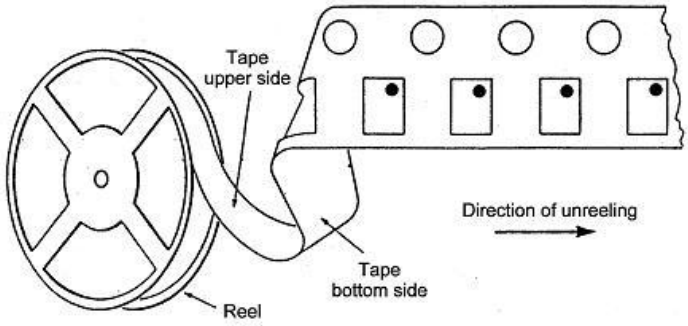
Upon standard specification 12MRH00191A, marking is described as follow :

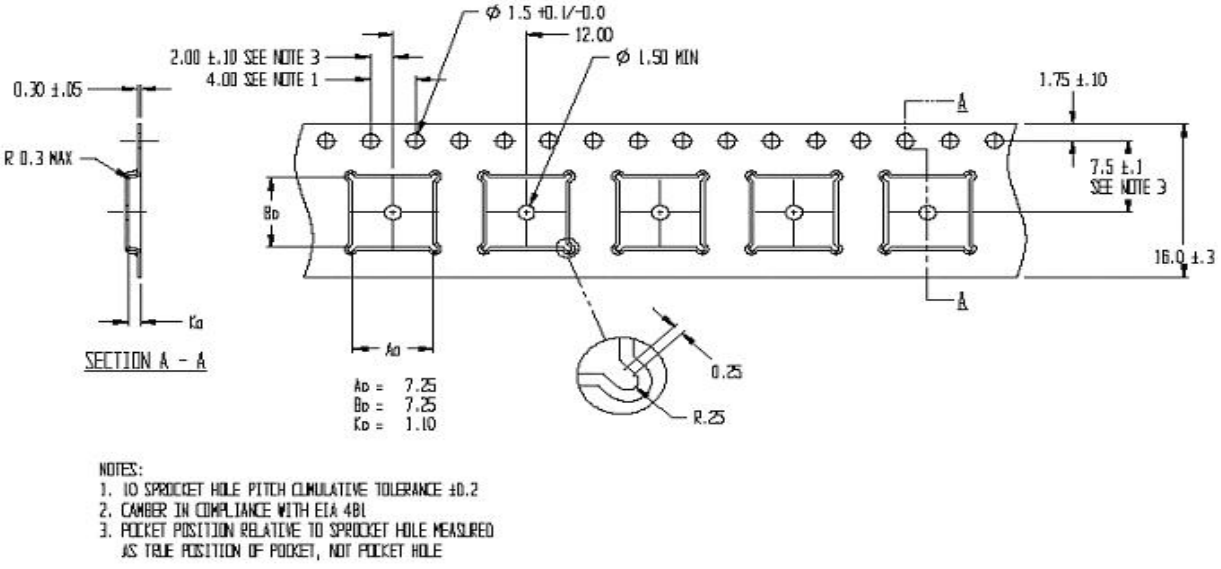
- Format code = 057
- (f) = Freescale logo
- yy = assembly year, ww = assembly week
- A = assembly site code / test site code, WL = wafer lot code



Samples are tape & reeled in accordance with the Freescale standard, per 2000, under the following conditions:

- Advantek P/N: ML0707-A
- Tape Width: 16mm
- Tape Pitch (part to part): 12 mm
- Reel diameter: 13 inches





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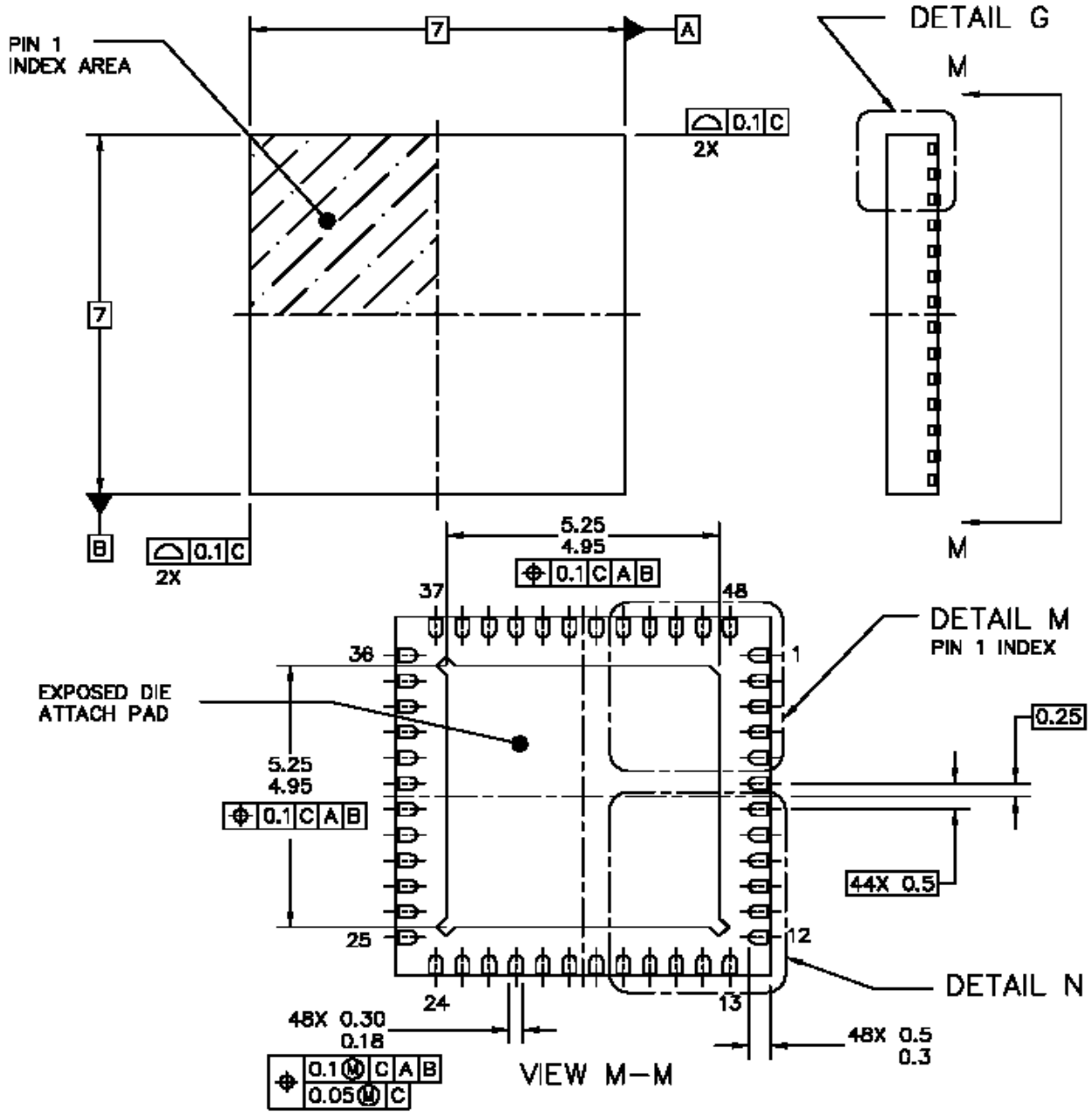

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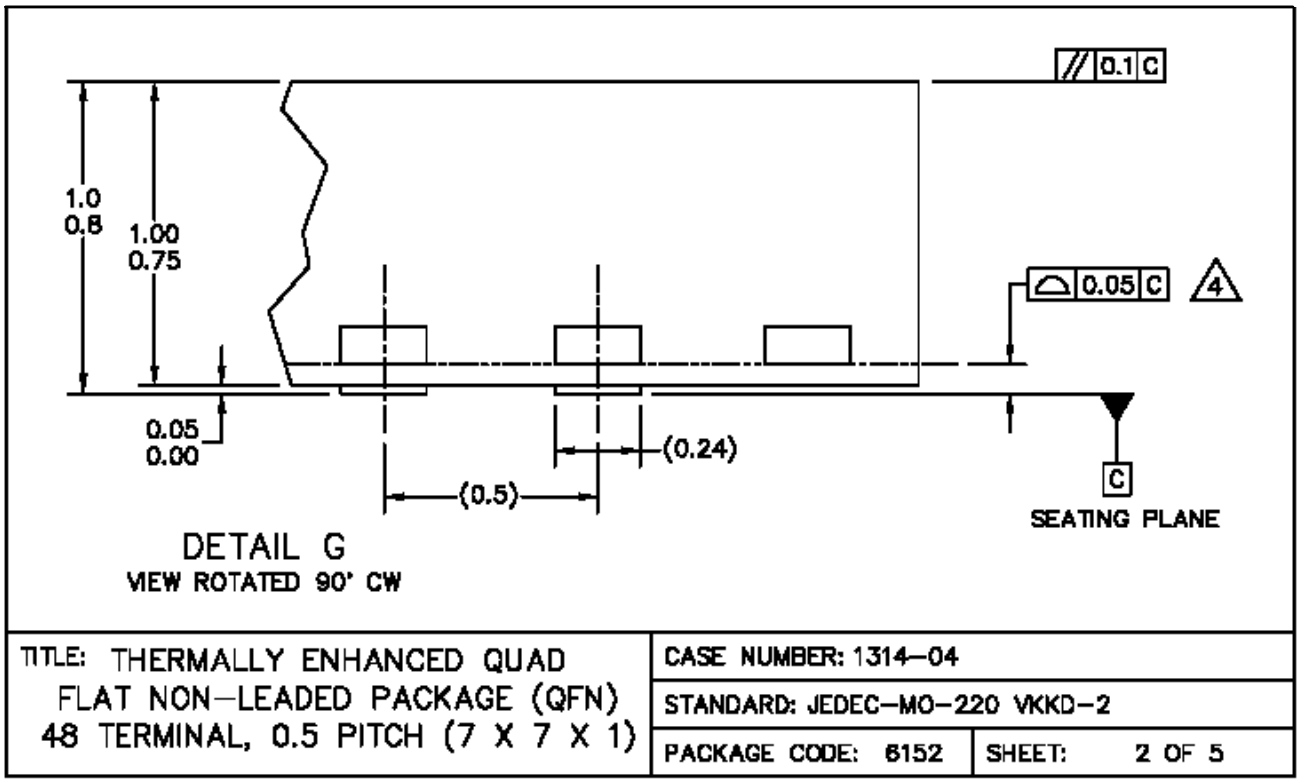
PACKAGE CODE: 6152
SHEET: 1 OF 5



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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	CASE NUMBER: 1314–04	
	STANDARD: JEDEC–MO–220 VKKD–2	
	PACKAGE CODE: 6152	SHEET: 4 OF 5

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