AK4426

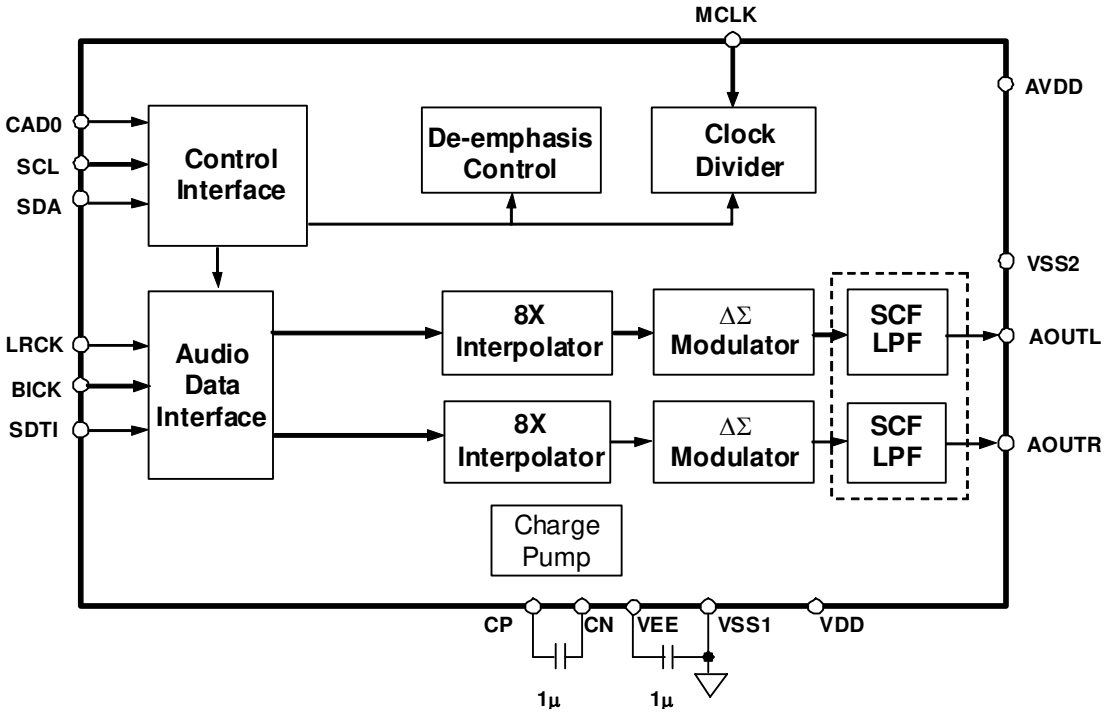
192kHz 24-Bit Stereo ΔΣ DAC with 2Vrms Output

GENERAL DESCRIPTION

The AK4426 is a 5V 24-bit stereo DAC with an integrated 2Vrms output buffer. A charge pump in the buffer develops an internal negative power supply rail that enables a ground-referenced 2Vrms output. Using AKM's multi bit modulator architecture, the AK4426 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4426 integrates a combination of switched-capacitor and continuous-time filters, increasing performance for systems with excessive clock jitter. The 24-bit word length and 192kHz sampling rate make this part ideal for a wide range of consumer audio applications, such as DVD, AV receiver system and set-top boxes. The AK4426 is offered in a space saving 16pin TSSOP package.

FEATURES

- **Sampling Rate Ranging from 8kHz to 192kHz**
- **128 times Oversampling (Normal Speed Mode)**
- **64 times Oversampling (Double Speed Mode)**
- **32 times Oversampling (Quad Speed Mode)**
- **24-Bit 8 times FIR Digital Filter**
- **Switched-Capacitor Filter with High Tolerance to Clock Jitter**
- **Single Ended 2Vrms Output Buffer**
- **Digital De-emphasis Filter: 32kHz, 44.1kHz or 48kHz**
- **Soft mute**
- **Digital Attenuator (Linear 256 Step)**
- **Control I/F: I^2C-Bus**
- **Audio I/F format: 24Bit MSB justified, 24/20/16 LSB justified or I^2S compatible**
- **Master clock: 256fs, 384fs, 512fs, 768fs or 1152fs (Normal Speed Mode)**
  128fs, 192fs, 256fs or 384fs (Double Speed Mode)
  128fs, 192fs (Quad Speed Mode)
- **THD+N: -91dB**
- **Dynamic Range: 106dB**
- **Automatic Power-on Reset Circuit**
- **Power supply: +4.5 ~ +5.5V**
- **Ta = -40 to 85 °C**
- **Small Package: 16pin TSSOP (6.4mm x 5.0mm)**

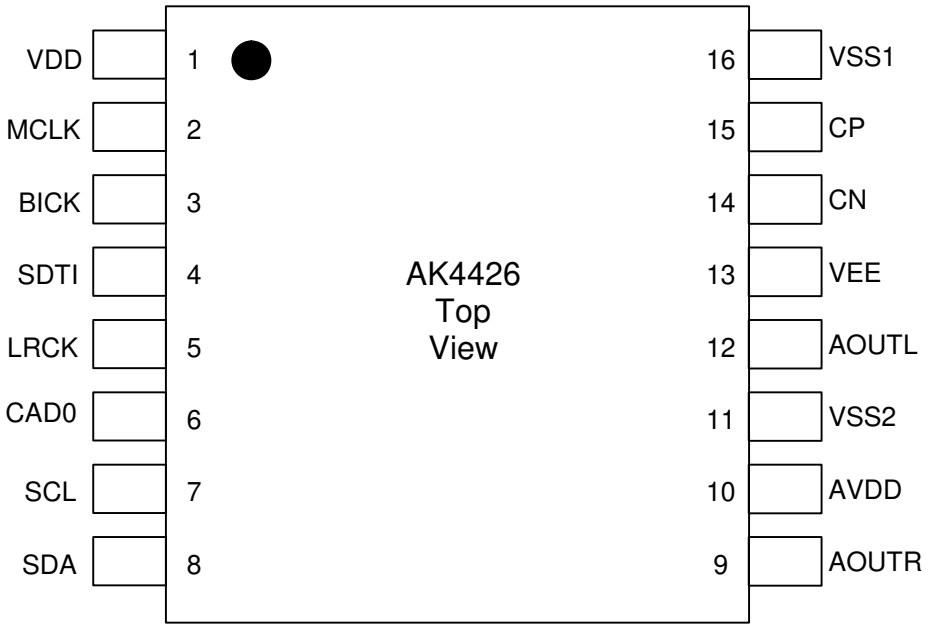


Block Diagram

■ Ordering Guide

AK4426VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4426	Evaluation Board for AK4426	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VDD	-	Digital Circuit and Charge Pump Circuit Power Supply Pin: 4.5V~5.5V
2	MCLK	I	Master Clock Input Pin An external TTL clock must be input on this pin.
3	BICK	I	Audio Serial Data Clock Pin
4	SDTI	I	Audio Serial Data Input Pin
5	LRCK	I	L/R Clock Pin
6	CAD0	I	Chip Address 0bit
7	SCL	I	Control Clock input Pin
8	SDA	I/O	Control Data Input/Output pin
9	AOUTR	O	Rch Analog Output Pin When power down, outputs VSS(0V, typ).
10	AVDD	-	Analog Block Power Supply Pin: 4.5V~5.5V
11	VSS2	-	Ground Pin2
12	AOUTL	O	Lch Analog Output Pin When power down, outputs VSS(0V, typ).
13	VEE	O	Negative Voltage Output Pin Connect to VSS1 with a 1.0μF capacitor which is low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin must be connected to the VSS1 pin. Non polarity capacitors can also be used.
14	CN	I	Negative Charge Pump Capacitor Terminal Pin Connect to CP with a 1.0μF capacitor which is low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin must be connected to the CP pin. Non polarity capacitors can also be used.
15	CP	I	Positive Charge Pump Capacitor Terminal Pin Connect to CN with a 1.0μF capacitor which is low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin must be connected to the CP pin. Non polarity capacitors can also be used.
16	VSS1	-	Ground Pin1

Note: All input pins except for the CN pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD CVDD	-0.3 -0.3	+6.0 +6.0	V V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS1, VSS2 connect to the same analog ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD AVDD	+4.5	+5.0 VDD	+5.5	V

Note 3. AVDD should be equal to VDD

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = +5.0V; fs = 44.1 kHz; BICK = 64fs; Signal Frequency = 1 kHz;
24bit Input Data; Measurement frequency = 20Hz ~ 20kHz; R_L ≥5kΩ)

Parameter		min	typ	max	Units
Resolution				24	Bits
Dynamic Characteristics (Note 4)					
THD+N (0dBFS)	fs=44.1kHz, BW=20kHz		-91	-84	dB
	fs=96kHz, BW=40kHz		-91	-	dB
	fs=192kHz, BW=40kHz		-91	-	dB
Dynamic Range (-60dBFS with A-weighted. (Note 5)		100	106		dB
S/N (A-weighted. (Note 6)		100	106		dB
Interchannel Isolation (1kHz)		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
DC Accuracy					
DC Offset	(at output pin)	-5	0	+5	mV
Gain Drift			100	-	ppm/°C
Output Voltage (Note 7)		2.05	2.2	2.35	Vrms
Load Capacitance (Note 8)				25	pF
Load Resistance		5			kΩ
Power Supplies					
Power Supply Current: (Note 9)					
Normal Operation (fs≤96kHz)			24	36	mA
Normal Operation (fs=192kHz)			27	40	mA
Power-Down Mode (Note 10)			10	100	μA

Note 4. Measured by Audio Precision (System Two). Refer to the evaluation board manual.
Note 5. 98dB for 16bit input data
Note 6. S/N does not depend on input data size.
Note 7. Full-scale voltage (0dB). Output voltage is proportional to the voltage of AVDD,
AOUT (typ.@0dB) = 2.2Vrms × AVDD/5.
Note 8. In case of driving capacitive load, inset a resistor between the output pin and the capacitive load.
Note 9. The current into VDD and AVDD.
Note 10. All digital inputs including clock pins (MCLK, BICK and LRCK) are fixed to VSS1(VSS2) or VDD(AVDD).

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = +4.5 ~ +5.5V; fs = 44.1 kHz; DEM = OFF; SLOW = "0")

Parameter			Symbol	min	typ	max	Units
Digital filter							
Passband ±0.05dB (Note 11)			PB	0		20.0	kHz
–6.0dB				-	22.05	-	kHz
Stopband (Note 11)			SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay (Note 12)			GD	-	19.3	-	1/fs
Digital Filter + LPF							
Frequency Response	20.0kHz	fs=44.1kHz	FR	-	± 0.05	-	dB
	40.0kHz	fs=96kHz	FR	-	± 0.05	-	dB
	80.0kHz	fs=192kHz	FR	-	± 0.05	-	dB

Note 11. The passband and stopband frequencies scale with fs(system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 12. Calculated delay time caused by digital filter. This time is measured from setting the 16/24bit data of both channels to input register to the output of the analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD = AVDD = +4.5 ~ +5.5V; fs = 44.1kHz; DEM = OFF; SLOW = "1")

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband ±0.04dB (Note 13)			PB	0		8.1	kHz
-3.0dB				-	18.2	-	kHz
Stopband (Note 13)			SB	39.2			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay (Note 12)			GD	-	19.3	-	1/fs
Digital Filter + LPF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0/-5	-	dB
	40.0kHz	fs=96kHz	FR	-	+0/-4	-	dB
	80.0kHz	fs=192kHz	FR	-	+0/-5	-	dB

Note 13. The passband and stopband frequencies scale with fs(system sampling rate).
For example, PB=0.185×fs (@±0.04dB), SB=0.888×fs.

DC CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = +4.5 ~ +5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
Input Leakage Current	Iin	-	-	± 10	µA

SWITCHING CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = +4.5 ~ +5.5V)

Parameter	Symbol	min	Typ	max	Units
Master Clock Frequency	fCLK	2.048	11.2896	36.864	MHz
Duty Cycle	dCLK	30		70	%
LRCK Frequency					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	32		96	kHz
Quad Speed Mode	fsq	120		192	kHz
Duty Cycle	Duty	45		55	%
Audio Interface Timing					
BICK Period					
Normal Speed Mode	tBCK	1/128f			ns
Double Speed Mode	tBCK	sn			ns
Quad Speed Mode	tBCK	1/64fs			ns
BICK Pulse Width Low	tBCKL	d			ns
Pulse Width High	tBCKH	1/64fs			ns
BICK "↑" to LRCK Edge (Note 14)	tBLR	q			ns
LRCK Edge to BICK "↑" (Note 14)	tLRB	30			ns
SDTI Hold Time	tSDH	30			ns
SDTI Setup Time	tSDS	20			ns
		20			
		20			
		20			
Control Interface Timing (I2C Bus) (Note 15)					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time	tHD:STA	0.6		-	µs
(prior to first clock pulse)					
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 16)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise	tSP	0		50	ns
Suppressed by Input Filter					
Capacitive load on bus	Cb			400	pF

Note 14. BICK rising edge must not occur at the same time as LRCK edge.
Note 15. I^2C-bus is a trademark of NXP B.V.
Note 16. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

■ Timing Diagram

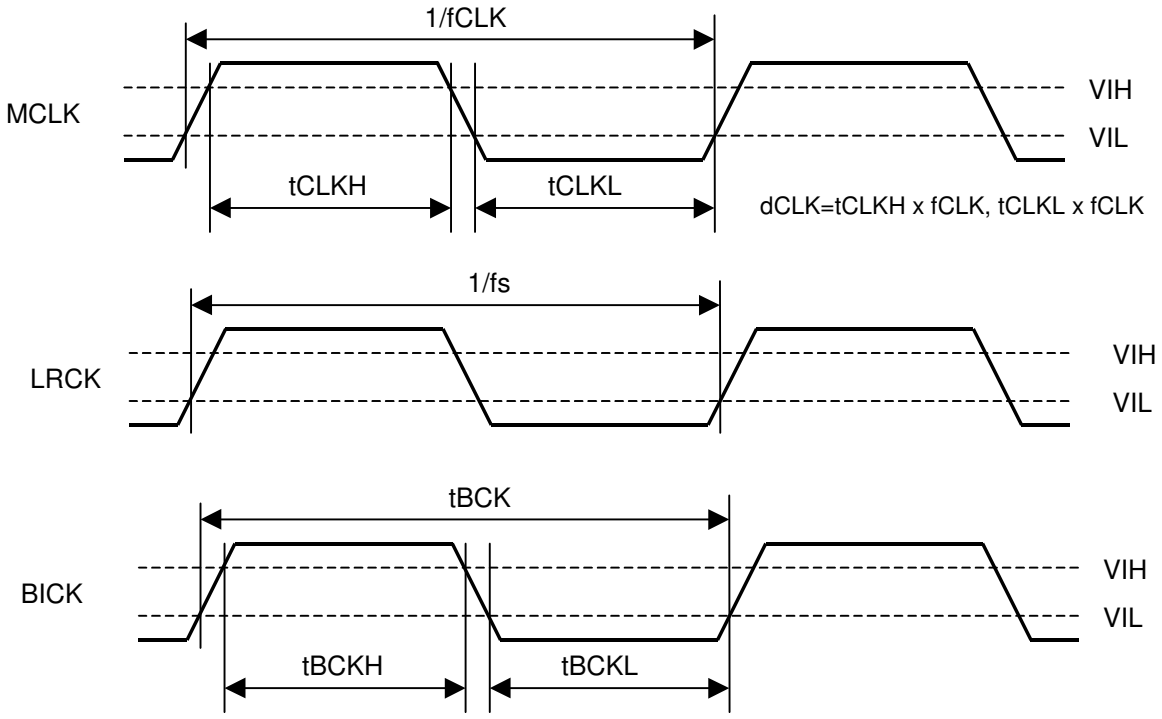


Figure 1. Clock Timing

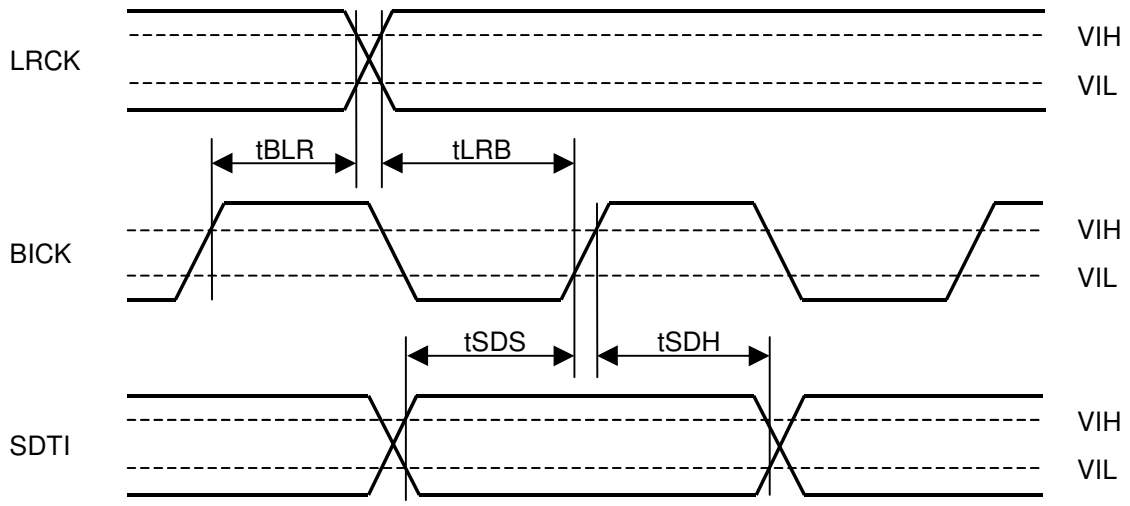


Figure 2. Serial Interface Timing

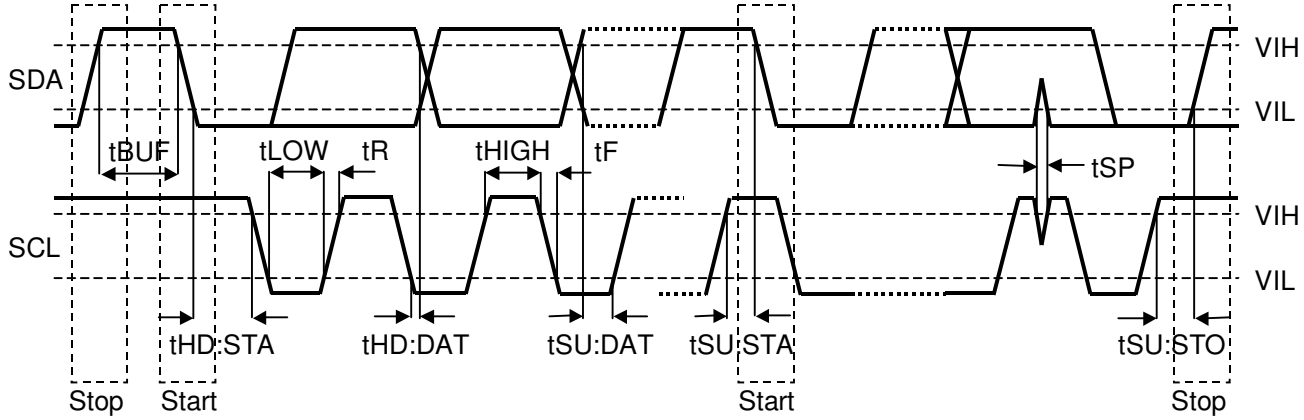


Figure 3. I^2C Bus mode Timing

OPERATION OVERVIEW

■ System Clock

The external clocks required to operate the AK4426 are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = "0": Register 00H), the sampling speed is set by DFS0/1 (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 2) When the power applied, the AK4426 is in Auto Setting Mode. In Auto Setting Mode (ACKS = "1": Default), as MCLK frequency is detected automatically (Table 3) and the internal master clock becomes the appropriate frequency (Table 4), it is not necessary to set DFS0/1.

The AK4426 is automatically placed in power saving mode when MCLK, LRCK and BICK stop during normal operation mode, and the analog output is forced to 0V(typ). When MCLK, LRCK and BICK are input again, the AK4426 is powered up. After power-up, the AK4426 is in the power-down mode until MCLK, LRCK and BICK are input.

DFS1	DFS0	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	(default)
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 1. Sampling Speed (Manual Setting Mode)

DFS1	DFS0	Sampling Speed	LRCK (kHz)	MCLK (MHz)							BICK (MHz)
			fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	64fs
0	0	Normal	32.0	-	-	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480
0	0		44.1	-	-	11.2896	16.9344	22.5792	33.8688	-	2.8224
0	0		48.0	-	-	12.2880	18.4320	24.5760	36.8640	-	3.0720
0	1	Double	88.2	11.2896	16.9344	22.5792	33.8688	-	-	-	5.6448
0	1		96.0	12.2880	18.4320	24.5760	36.8640	-	-	-	6.1440
1	0	Quad	176.4	22.5792	33.8688	-	-	-	-	-	11.2896
1	0		192.0	24.5760	36.8640	-	-	-	-	-	12.2880

Table 2. System Clock Example (Manual Setting Mode)

MCLK		Sampling Speed
1152fs		Normal (fs=32kHz only)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 3. Sampling Speed(Auto Setting Mode: Default)

LRCK	MCLK (MHz)							Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	-	
48.0kHz	-	-	-	-	24.5760	36.8640	-	
32.0kHz			8.192	12.288				Double
44.1kHz			11.2896	16.9344				
48.0kHz			12.288	18.432				
88.2kHz	-	-	22.5792	33.8688	-	-	-	
96.0kHz	-	-	24.5760	36.8640	-	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	-	

Table 4. System Clock Example (Auto Setting Mode)

When MCLK= 256fs/384fs, the AK4425 supports sampling rate of 32kHz~96kHz in auto setting mode (Table 4). But, when the sampling rate is 32kHz~48kHz, DR and S/N will degrade as compared to when MCLK= 512fs/768fs.

MCLK	DR,S/N
256fs/384fs	103dB
512fs/768fs	106dB

Table 5. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz) (Auto Setting Mode)

■ Audio Serial Interface Format

The audio data is shifted in via the SDTI pin using the BICK and LRCK inputs. The DIF2-0 bit can select within five serial data modes as shown in Table 6. In all modes the serial data is MSB-first, two's complement format and it is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI Format	BICK	Figure	
0	0	0	0	16bit LSB Justified	≥32fs	Figure 4	
1	0	0	1	20bit LSB Justified	≥40fs	Figure 5	
2	0	1	0	24bit MSB Justified	≥48fs	Figure 6	(default)
3	0	1	1	24bit I^2S Compatible	≥48fs	Figure 7	
4	1	0	0	24bit LSB Justified	≥48fs	Figure 5	

Table 6. Audio Data Format in Serial control mode

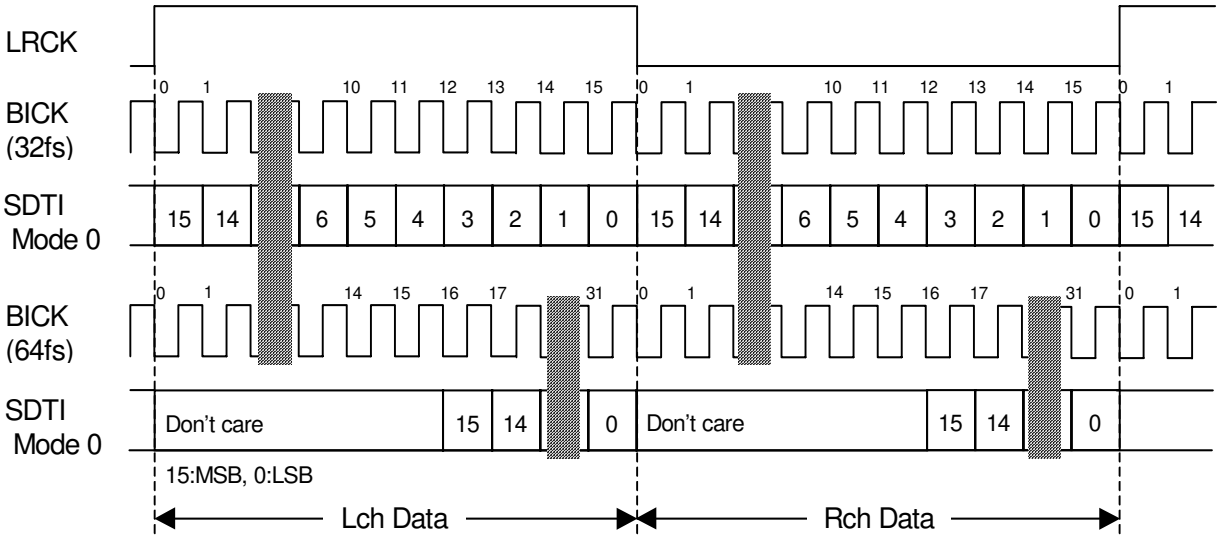


Figure 4. Mode 0 Timing

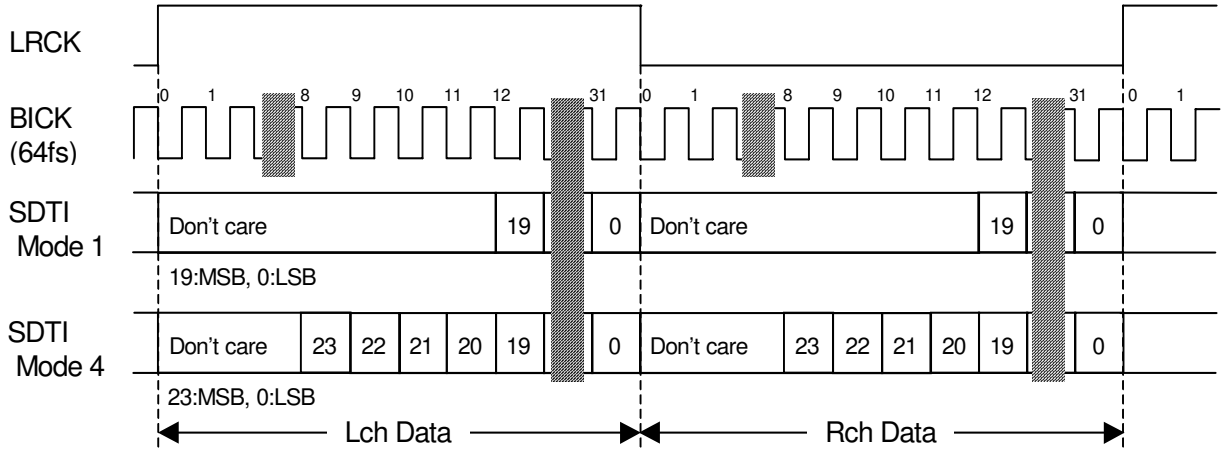


Figure 5. Mode 1/4 Timing

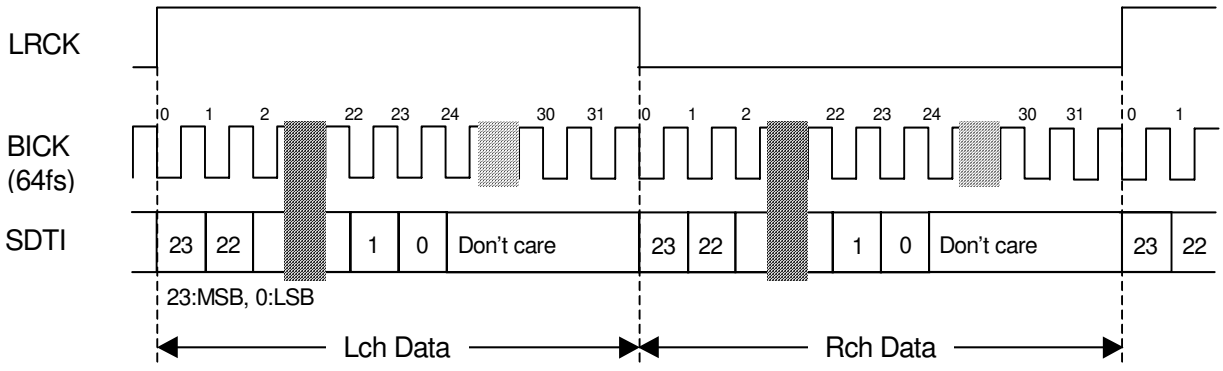


Figure 6. Mode 2 Timing

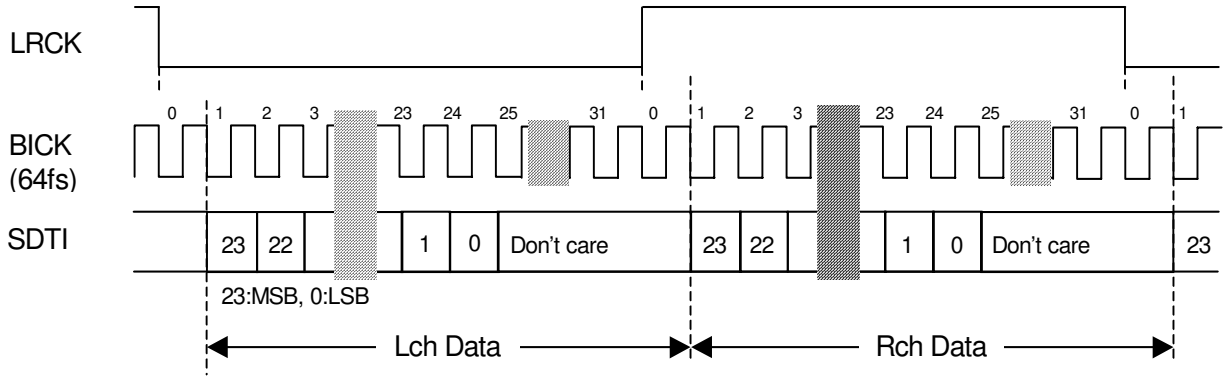


Figure 7. Mode 3 Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled with DEM0 and DEM1. In case of double speed and quad speed mode, the digital de-emphasis filter is always OFF.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 7. De-emphasis Filter Control (Normal Speed Mode)

■ Analog Output Block

The internal negative power supply generation circuit (Figure 8) provides a negative power supply for the internal 2Vrms amplifier. It allows the AK4426 to output an audio signal centered at VSS (0V, typ) as shown in Figure 9. The negative power generation circuit (Figure 8) needs 1.0uF low ESR (Equivalent Series Resistance) capacitors (Ca, Cb). If this capacitor is polarized, the positive polarity pin should be connected to the CP and VSS1 pins. This circuit operates by clocks generated from MCLK. When MCLK stops, the AK4426 is placed in the reset mode automatically and the analog outputs settle to VSS (0V, typ).

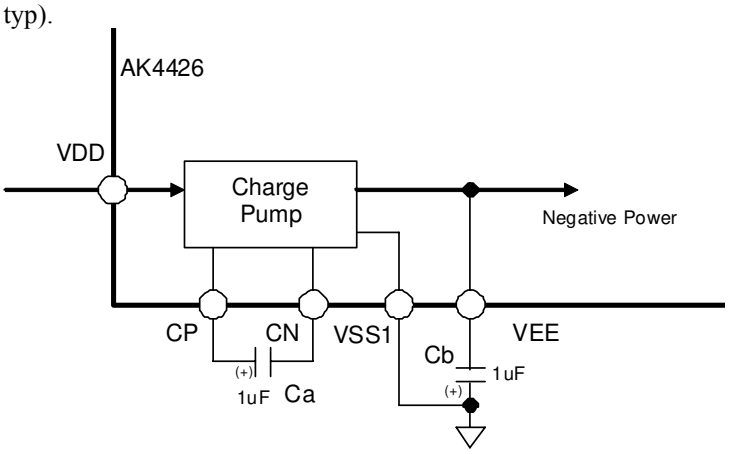


Figure 8. Negative Power Generation Circuit

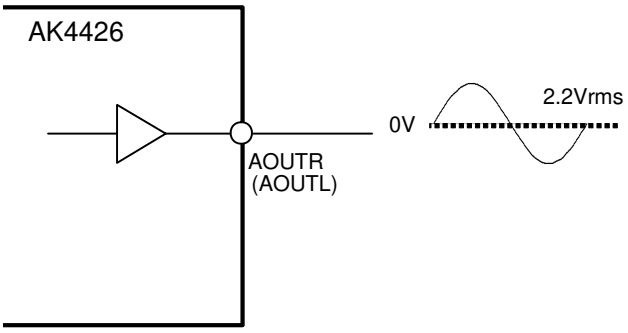


Figure 9. Audio Signal Output

■ Output Volume

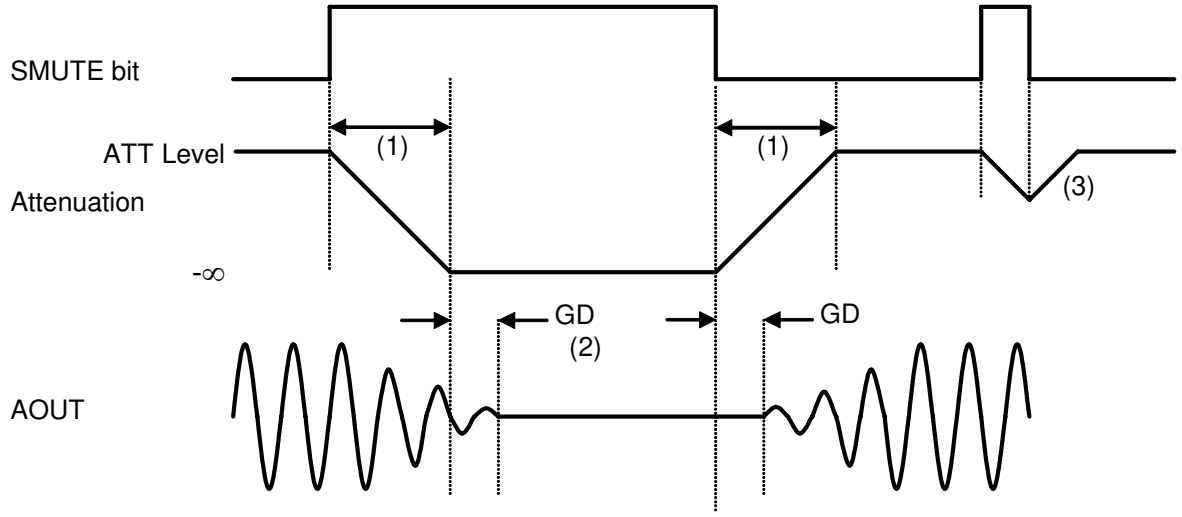
The AK4426 includes channel independent digital output volumes (ATT) with 256 levels at linear step including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to –48dB and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. The transition time of 1 level and all 256 levels is shown in Table 8.

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

Table 8. ATT Transition Time

■ Soft Mute Operation

Soft mute operation is performed in digital domain. When the SMUTE bit goes to “1”, the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 8) from the current ATT level. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 8). For example, in Normal Speed Mode, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255.

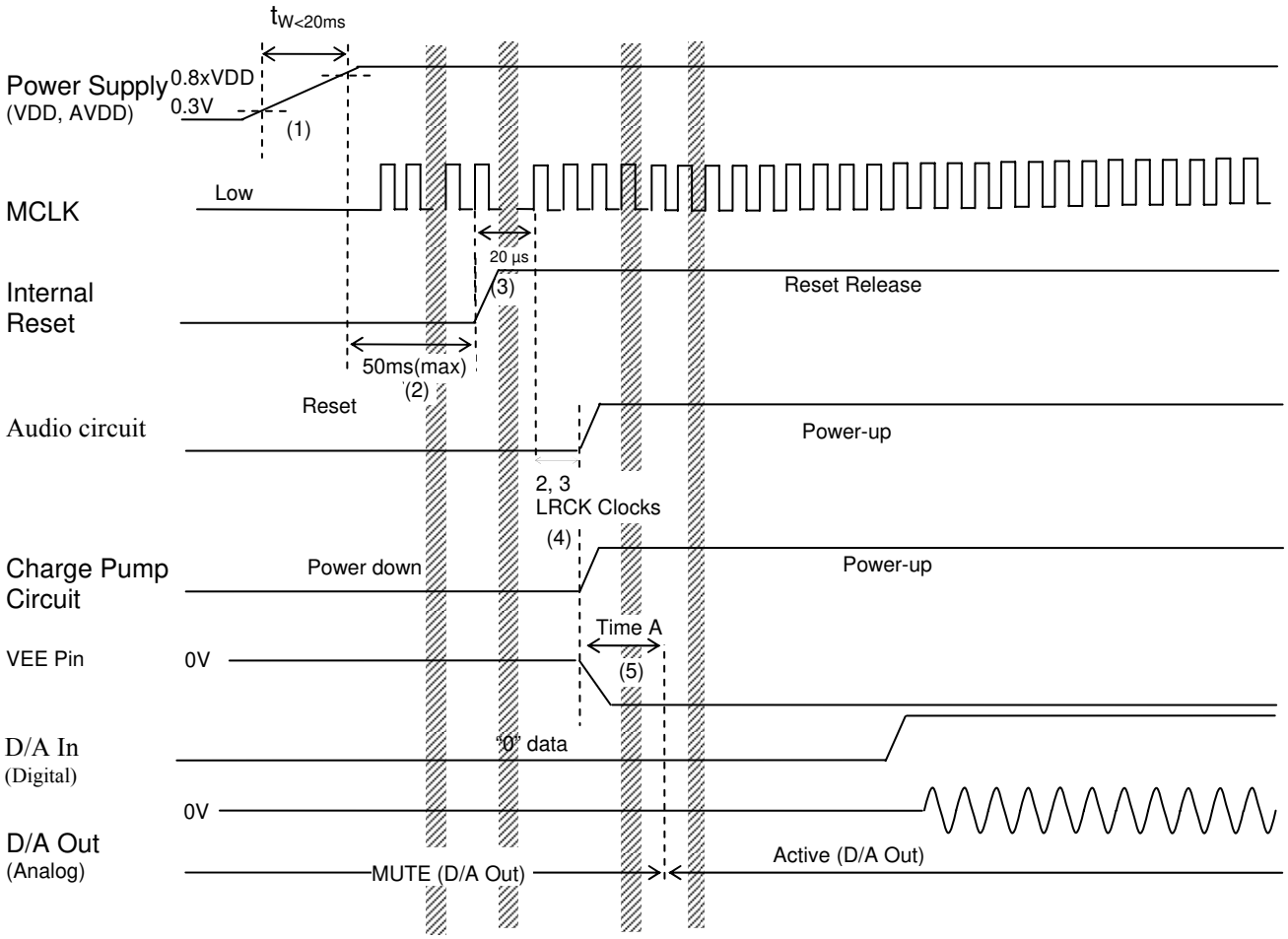
(2) The analog output corresponding to the digital input has group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 10. Soft Mute function

■ System Reset

The AK4426 is in power down mode upon power-up. The MLCK should be input after the power supplies are ramped up. The AK4426 is in power-down mode until LRCK are input.

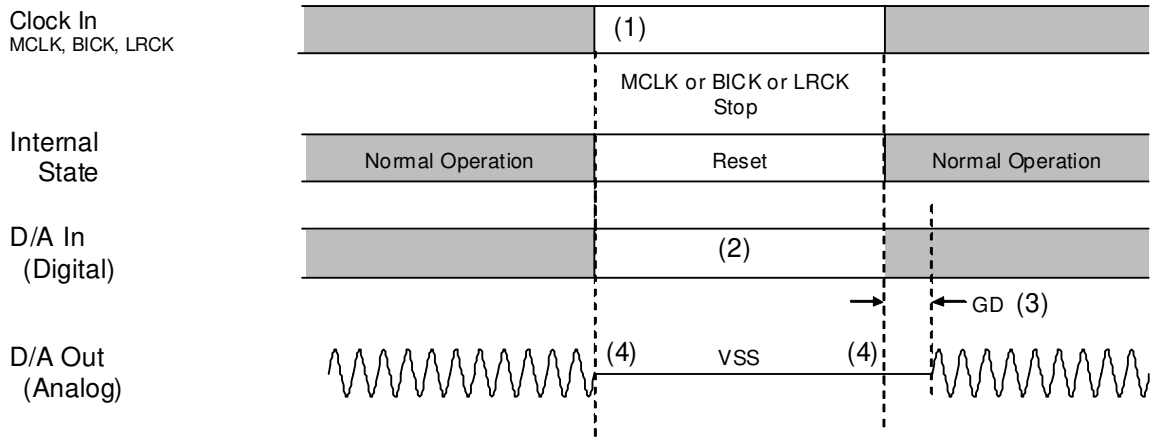


Notes:
(1) The AK4426 includes an internal Power on Reset Circuit which is used to reset the digital logic into a default state after power up. Therefore, the power supply voltage must reach 80% VDD from 0.3V in less than 20msec.
(2) Register writings are valid after 50ms (max).
(3) When internal reset is made, approximately 20us after a MCLK input, the internal analog circuit is powered-up.
(4) The digital circuit and charge pump circuit are powered-up in 2, 3 LRCK cycle when the analog circuit is powered-up.
(5) The charge pump counter starts after the charge pump circuit is powered-up. The DAC outputs a valid analog signal after Time A.
Time A = 1024/(fs x 16): Normal speed mode
Time A = 1024/(fs x 8): Double speed mode
Time A = 1024/(fs x 4): Quad speed mode

Figure 11. System Reset Diagram

■ Reset Function

When the MCLK, LRCK or BICK stops, the AK4426 is placed in reset mode and its analog outputs are set to VSS (0V, typ). When the MCLK, LRCK and BICK are restarted, the AK4426 returns to normal operation mode.



Notes:

(1) Clocks (MCLK, BICK, LRCK) can be stopped in the reset mode (MCLK or LRCK is stopped).
(2) Digital data can be stopped. The click noise after MCLK and LRCK are input again can be reduced by inputting the "0" data during this period.
(3) The analog output corresponding to a specific digital input has group delay (GD).
(4) No audible click noise occurs under normal conditions.

Figure 12. Reset Timing Example

■ Mode Control Interface

I²C-bus Control Mode

1. WRITE Operations

Figure 13 shows the data transfer sequence in I²C-bus mode. All commands are preceded by START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 17). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit which is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001000". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets this device address bit (Figure 14). If the slave address match that of the AK4426 and R/W bit is "0", the AK4426 generates an acknowledge and the write operation is executed. If R/W bit is "1", the AK4426 does not answer any acknowledge (Figure 17). The second byte consists of the address for control registers of the AK4426. The format is MSB first, and those most significant 6-bits are fixed to zeros (Figure 15). The data after the second byte contain control data. The format is MSB first, 8bits (Figure 16). The AK4426 generates an acknowledge after each byte is received. A data transfer is always terminated by STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 17).

The AK4426 can execute multiple one byte write operations in a sequence. After receipt of the third byte, the AK4426 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 04H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 19) except for the START and the STOP condition.

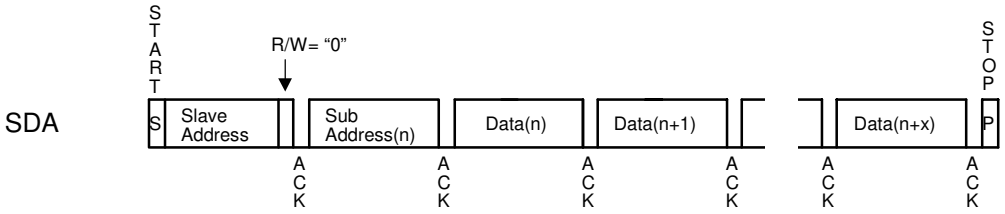


Figure 13. Data Transfer Sequence at I²C-bus Mode

0	0	1	0	0	0	CAD0	R/W

Figure 14. The First Byte (The CAD0 should match with CAD0 pin)

0	0	0	0	0	0	A1	A0

Figure 15. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 16. Byte Structure After The Second Byte

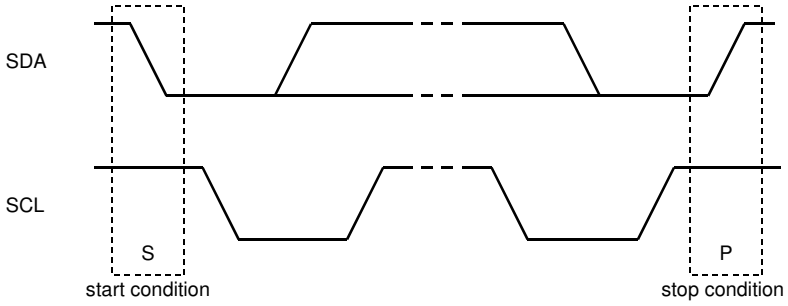


Figure 17. START and STOP Conditions

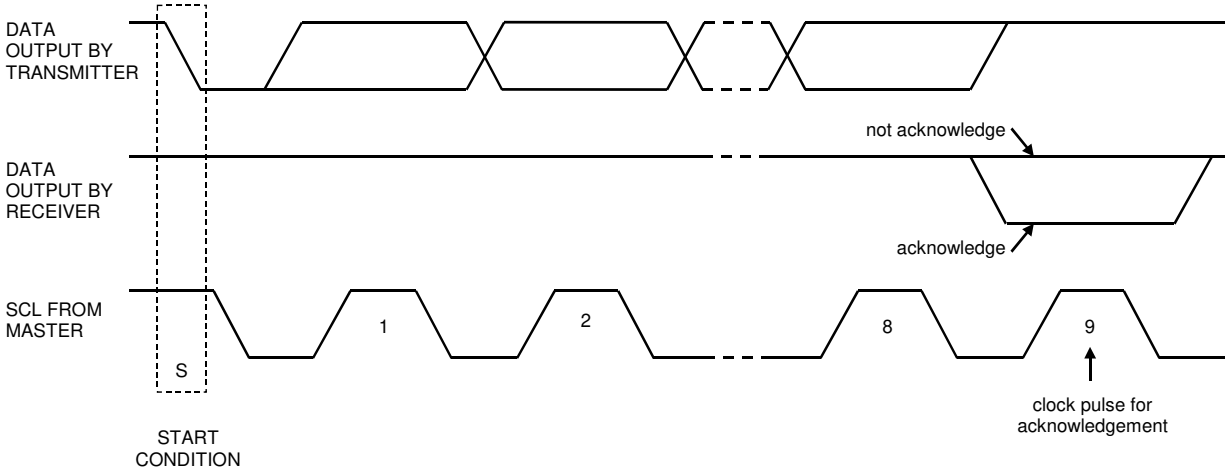


Figure 18. Acknowledge on the I^2C-bus

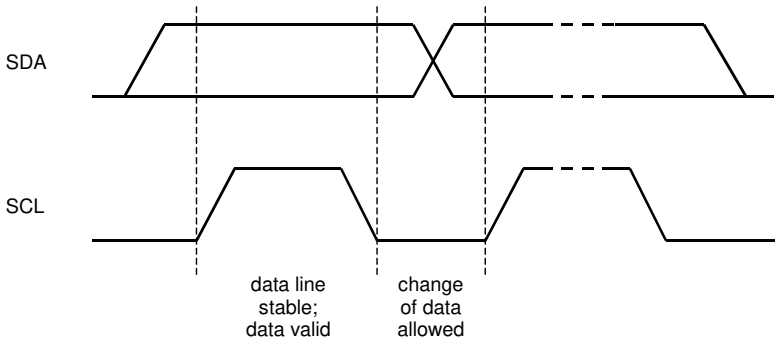


Figure 19. Bit Transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
01H	Control 2	0	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	RRST	0	0	INVL	INVR	0	0	0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:

Do not write any data to the register over 05H directly.

When RSTN bit goes “0”, the only internal timing is reset and the registers are not initialized to their default values. All data can be written to the register even if PW or RSTN bit is “0”.

Do not write the registers within 50msec after the power supplies are fed.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
default		1	0	0	0	1	0	1	1

RSTN: Internal timing reset control
0: Reset. All registers are not initialized.
1: Normal Operation
The click noise, which occurs when MCLK frequency or DFS is changed, can be reduced by RSTN bit.

PW: Power down control
0: Power down. All registers are not initialized.
1: Normal Operation

DIF2-0: Audio data interface formats (Table 6)
Default: "010", Mode 2

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the settings of DFS1-0 are ignored. When this bit is "0", DFS1-0 set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
default		0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal operation
1: DAC outputs soft muted

DEM1-0: De-emphasis Response (Table 7)
Default: "01", OFF

DFS1-0: Sampling speed control
00: Normal Speed Mode
01: Double Speed Mode
10: Quad Speed Mode
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

SLOW: Slow Roll-off Filter Enable
0: Sharp Roll-off Filter
1: Slow Roll-off Filter

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	RRST	0	0	INVL	INVR	0	0	0
default		0	0	0	0	0	0	0	0

INVR: Inverting Lch Output Polarity
0: Normal Output
1: Inverted Output

INVL: Inverting Rch Output Polarity
0: Normal Output
1: Inverted Output

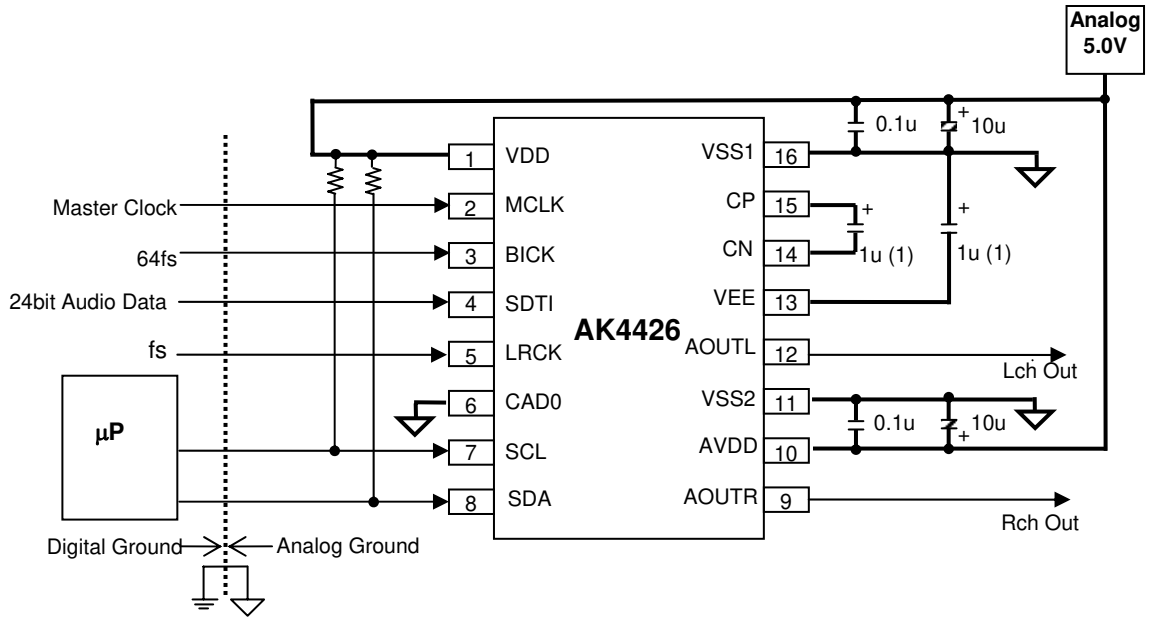
RRST: Register Reset
0: Normal Operation
1: Register Reset (except RRST bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
default		1	1	1	1	1	1	1	1

$ATT = 20 \log_{10} (ATT\_DATA / 255)$ [dB]
00H: Mute

SYSTEM DESIGN

Figure 20 shows the system connection diagram. An evaluation board (AKD4426) is available for fast evaluation as well as suggestions for peripheral circuitry.



Note:

Use low ESR (Equivalent Series Resistance) capacitors. When using polarized capacitors, the positive polarity pin should be connected to the CP and VSS2 pin.

VSS1 and VSS2 should be separated from digital system ground.

Digital input pins should not be allowed to float.

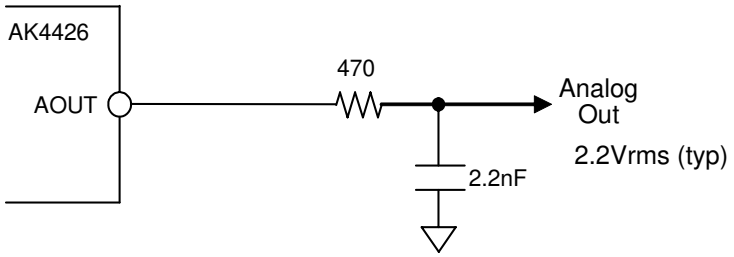
Figure 20. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

VDD and AVDD are supplied from the analog supply and should be separated from the system digital supply. Decoupling capacitors, especially 0.1μF ceramic capacitors for high frequency bypass, should be placed as near to VDD and AVDD as possible. The VSS1 and VSS2 must be connected to the same analog ground plane. **Power-up sequence between VDD and AVDD is not critical.**

2. Analog Outputs

The analog outputs are single-ended and centered around the VSS (ground) voltage. The output signal range is typically 2.2Vrms (typ @VDD=5V). The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Using single a 1st-order LPF (Figure 21) can reduce noise beyond the audio passband.

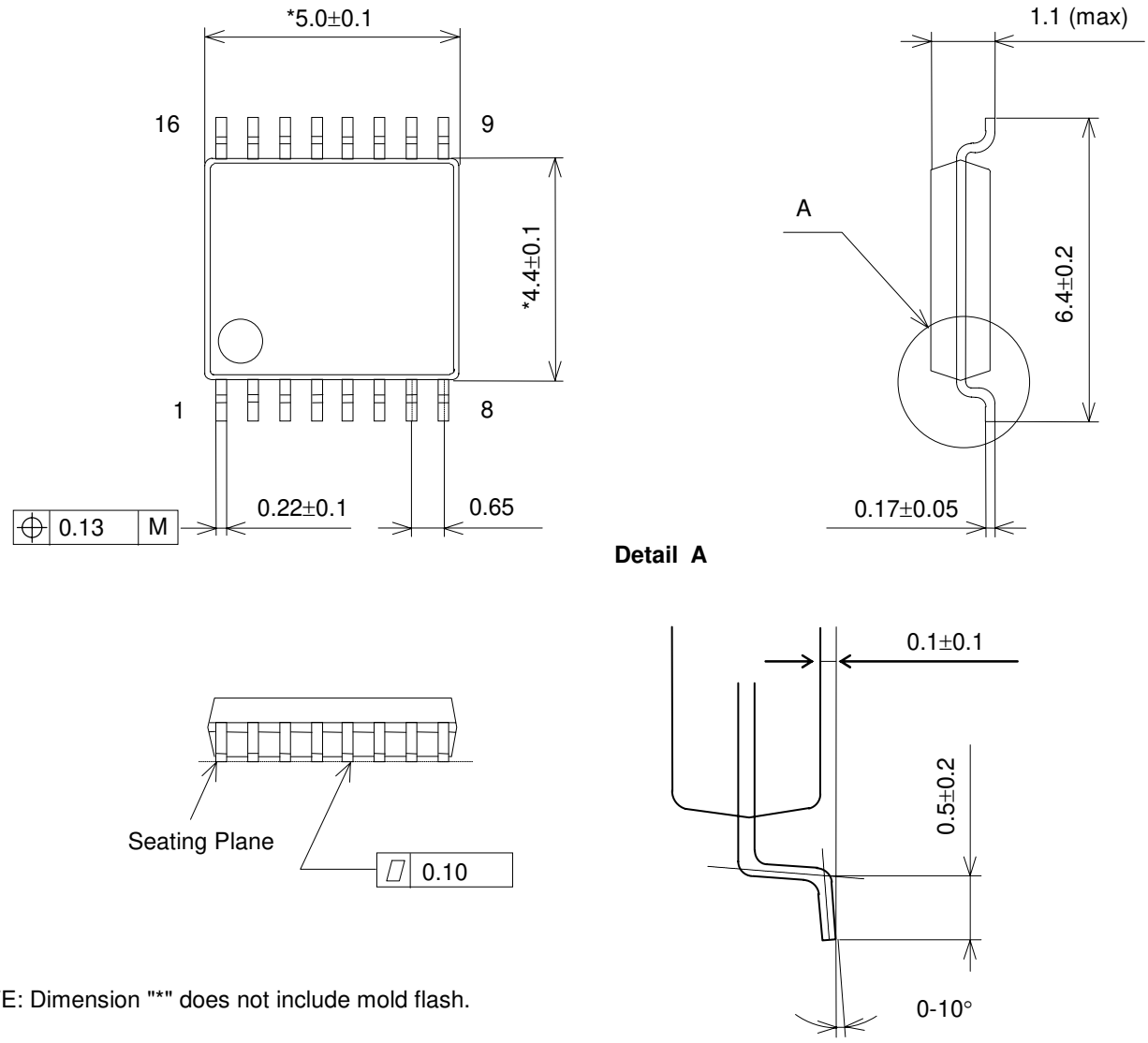


(fc = 154kHz, gain = -0.28dB @ 40kHz, gain = -1.04dB @ 80kHz)

Figure 21. External 1st order LPF Circuit Example1

PACKAGE

16pin TSSOP (Unit: mm)

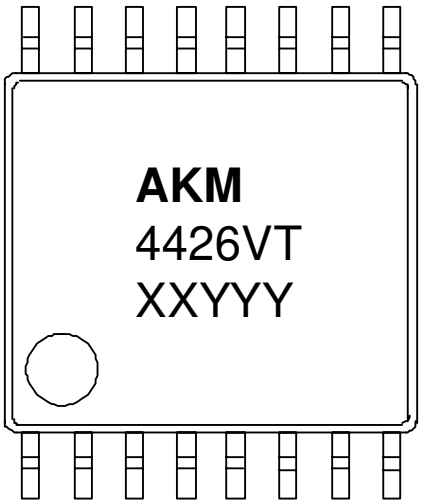


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4426VT
4) Asahi Kasei Logo

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
10/06/07	00	First Edition		
10/07/22	01	Error Correction	19-20	■ Mode Control Interface The description was corrected.
11/03/01	02	Error Correction	25	1. Grounding and Power Supply Decoupling The description was changed.

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