

FEATURES

- Optimized for dc to 3.75 Gbps data
- Programmable input equalization
 - Up to 22 dB boost at 1.875 GHz
 - Compensates up to 30 meters of CX4 cable up to 3.75 Gbps
 - Compensates up to 40 inches of FR4 up to 3.75 Gbps
- Programmable output pre-emphasis/de-emphasis
 - Up to 12 dB boost at 1.875 GHz (3.75 Gbps)
 - Compensates up to 15 meters of CX4 cable up to 3.75 Gbps
 - Compensates up to 40 inches of FR4 up to 3.75 Gbps
- Flexible 1.8 V to 3.3 V core supply
- Per lane P/N pair inversion for routing ease
- Low power: 125 mW/channel up to 3.75 Gbps
- DC- or ac-coupled differential CML inputs
- Programmable CML output levels
- 50 Ω on-chip termination
- Loss-of-signal detection
- Temperature range operation: -40°C to +85°C
- Supports 8b10b, scrambled, or uncoded NRZ data
- I²C control interface
- 64-lead LFCSP (QFN) package

APPLICATIONS

- 10GBase-CX4
- HiGig™
- InfiniBand®
- 1×, 2× Fibre Channel
- XAUI™
- Gigabit Ethernet over backplane or cable
- CPRI™
- 50 Ω cables

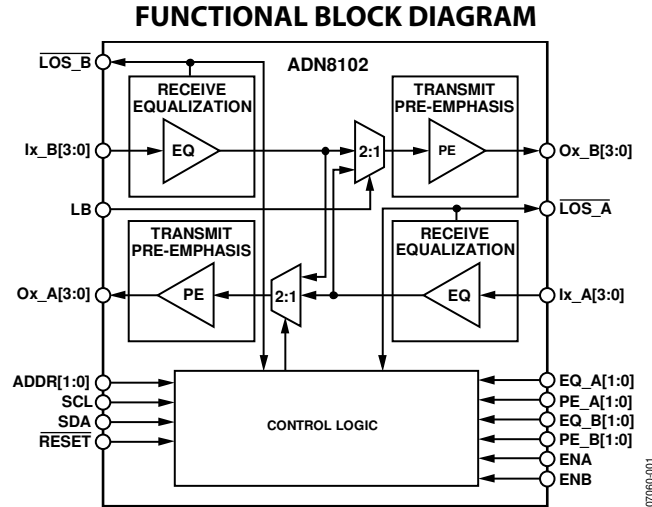


Figure 1.

GENERAL DESCRIPTION

The ADN8102 is a quad, bidirectional, CX4 cable/backplane equalizer with eight differential PECL-/CML-compatible inputs with programmable equalization and eight differential CML outputs with programmable output levels and pre-emphasis or de-emphasis. The operation of this device is optimized for NRZ data at rates up to 3.75 Gbps.

The receive inputs provide programmable equalization to compensate for up to 30 meters of CX4 cable (24 AWG) or 40 inches of FR4, and programmable pre-emphasis to compensate for up to 15 meters of CX4 cable (24 AWG) or 40 inches of FR4 at 3.75 Gbps. Each channel also provides programmable loss-of-signal detection and loopback capability for system testing and debugging.

The ADN8102 is controlled through toggle pins, an I²C® control interface that provides more flexible control, or a combination of both. Every channel implements an asynchronous path supporting dc to 3.75 Gbps NRZ data, fully independent of other channels. The ADN8102 has low latency and very low channel-to-channel skew.

The main application for the ADN8102 is to support switching in chassis-to-chassis applications over CX4 or InfiniBand cables.

The ADN8102 is packaged in a 9 mm × 9 mm 64-lead LFCSP (QFN) package and operates from -40°C to +85°C.

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REVISION HISTORY

8/2021—Rev. B to Rev. C

| | |
|----------------------------------|----|
| Change to Figure 4 | 7 |
| Updated Outline Dimensions | 33 |
| Changes to Ordering Guide | 33 |

10/2010—Rev. A to Rev. B

| | |
|--|----|
| Changes to Power Supply/Supply Current Parameter, Table 1... 4 | |
| Added t _{RESET} Parameter and Note 1, Table 2 and Figure 3; | |
| Renumbered Sequentially..... | 5 |
| Added Junction Temperature Parameter, Table 3 | 6 |
| Changes to Introduction Section..... | 16 |
| Added Table 5; Renumbered Sequentially | 16 |
| Changes to Equalization Settings Section | 17 |
| Added Table 7 and Advanced Equalization Settings Section ... | 17 |
| Changes to Table 8..... | 18 |
| Added Table 12 | 20 |
| Changes to Loopback Section and Changes to Table 13 | 20 |
| Added Table 14 | 21 |
| Changes to Table 15..... | 21 |
| Changes to Table 17..... | 22 |
| Deleted High Current Setting and Output Level Shift | |
| Section..... | 23 |
| Deleted Table 14; Renumbered Sequentially | 24 |
| Changes to Table 18..... | 24 |
| Added Table 19 | 24 |

| | |
|---|----|
| Deleted Table 15 | 25 |
| Added Applications Information Section and Output | |
| Compliance Section | 27 |
| Moved TxHeadroom and Figure 44 | 27 |
| Changes to TxHeadroom and Figure 44 | 27 |
| Added Table 20 | 27 |
| Added Table 21 | 28 |
| Deleted Transmission Lines Section and Soldering Guidelines | |
| for Chip Scale Package Section..... | 28 |
| Changes to Printed Circuit Board (PCB) Layout Guidelines | |
| Section..... | 29 |
| Added Figure 45, Supply Sequencing Section, Thermal Paddle | |
| Design Section, and Figure 46 | 29 |
| Added Stencil Design for the Thermal Paddle, Figure 47, and | |
| Figure 48 | 30 |

8/2008—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to Features Section | 1 |
| Changes to Loss of Signal/Signal Detect Section | 18 |
| Added Recommended LOS Settings Section..... | 18 |
| Deleted Figure 39; Renumbered Sequentially | 18 |
| Exposed Paddle Notation Added to Outline Dimensions | 31 |

5/2008—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 1.8\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{TTI} = V_{TTO} = V_{CC}$, $R_L = 50\ \Omega$, differential output swing = 800 mV p-p differential, 3.75 Gbps, PRBS $2^7 - 1$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---------------------------------|--|------|----------------|------|----------|
| DYNAMIC PERFORMANCE | | | | | |
| Maximum Data Rate/Channel (NRZ) | | 3.75 | | | Gbps |
| Deterministic Jitter | Data rate < 3.75 Gbps; BER = 1×10^{-12} | | 33 | | ps p-p |
| Random Jitter | $V_{CC} = 1.8\text{ V}$ | | 1.5 | | ps rms |
| Residual Deterministic Jitter | | | | | |
| With Input Equalization | Data rate < 3.25 Gbps; 0 inches to 40 inches FR4 | | 0.20 | | UI |
| | Data rate < 3.25 Gbps; 0 meters to 30 meters CX4 | | 0.19 | | UI |
| | Data rate < 3.75 Gbps; 0 inches to 40 inches FR4 | | 0.24 | | UI |
| | Data rate < 3.75 Gbps; 0 meters to 30 meters CX4 | | 0.21 | | UI |
| With Output Pre-Emphasis | Data rate < 3.25 Gbps; 0 inches to 40 inches FR4 | | 0.13 | | UI |
| | Data rate < 3.25 Gbps; 0 meters to 15 meters CX4 | | 0.37 | | UI |
| | Data rate < 3.75 Gbps; 0 inches to 40 inches FR4 | | 0.14 | | UI |
| | Data rate < 3.75 Gbps; 0 meters to 15 meters CX4 | | 0.41 | | UI |
| Output Rise/Fall Time | 20% to 80% | | 75 | | ps |
| Propagation Delay | | | 1 | | ns |
| Channel-to-Channel Skew | | | 50 | | ps |
| OUTPUT PRE-EMPHASIS | | | | | |
| Equalization Method | 1-tap programmable pre-emphasis | | | | |
| Maximum Boost | 800 mV p-p output swing | | 6 | | dB |
| | 200 mV p-p output swing | | 12 | | dB |
| Pre-Emphasis Tap Range | Minimum | | 2 | | mA |
| | Maximum | | 12 | | mA |
| INPUT EQUALIZATION | | | | | |
| Minimum Boost | EQBY = 1 | | 1.5 | | dB |
| Maximum Boost | Maximum boost occurs at 1.875 GHz | | 22 | | dB |
| Number of Equalization Settings | | | 8 | | |
| Gain Step Size | | | 2.5 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Voltage Swing | Differential, $V_{ICM}^1 = V_{CC} - 0.6\text{ V}$ | 300 | | 2000 | mV p-p |
| Input Voltage Range | Single-ended absolute voltage level, V_L minimum | | $V_{EE} + 0.4$ | | V p-p |
| | Single-ended absolute voltage level, V_H maximum | | $V_{CC} + 0.5$ | | V p-p |
| Input Resistance | Single-ended | 45 | 50 | 55 | Ω |
| Input Return Loss | Measured at 2.5 GHz | | 5 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | DC, differential, PE = 0, default, $V_{CC} = 1.8\text{ V}$ | 635 | 740 | 870 | mV p-p |
| | DC, differential, PE = 0, default, $V_{CC} = 3.3\text{ V}$ | | 800 | | mV p-p |
| | DC, differential, PE = 0, minimum output level, ² $V_{CC} = 1.8\text{ V}$ | | 100 | | mV p-p |
| | DC, differential, PE = 0, minimum output level, ² $V_{CC} = 3.3\text{ V}$ | | 100 | | mV p-p |
| | DC, differential, PE = 0, maximum output level, ² $V_{CC} = 1.8\text{ V}$ | | 1300 | | mV p-p |
| | DC, differential, PE = 0, maximum output level, ² $V_{CC} = 3.3\text{ V}$ | | 1800 | | mV p-p |

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| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--------------------------------|---|----------------|----------------|-----|----------------|
| Output Voltage Range | Single-ended absolute voltage level, TxHeadroom = 0; V_L minimum | | $V_{CC} - 1.1$ | | V |
| | Single-ended absolute voltage level, TxHeadroom = 0; V_H maximum | | $V_{CC} + 0.6$ | | V |
| | Single-ended absolute voltage level, TxHeadroom = 1; V_L minimum | | $V_{CC} - 1.2$ | | V |
| | Single-ended absolute voltage level, TxHeadroom = 1; V_H maximum | | $V_{CC} + 0.6$ | | V |
| Output Current | Minimum output current per channel | | 2 | | mA |
| | Maximum output current per channel, $V_{CC} = 1.8$ V | | 21 | | mA |
| Output Resistance | Single-ended | 43 | 50 | 57 | Ω |
| Output Return Loss | Measured at 2.5 GHz | | 5 | | dB |
| LOS CHARACTERISTICS | | | | | |
| Assert Level | IN_A/IN_B LOS threshold = 0x0C | | 20 | | mV diff |
| Deassert Level | IN_A/IN_B LOS hysteresis = 0x0D | | 225 | | mV diff |
| POWER SUPPLY | | | | | |
| Operating Range | | | | | |
| V_{CC} | $V_{EE} = 0$ V | 1.7 | 1.8 | 3.6 | V |
| DV_{CC} | $V_{EE} = 0$ V, $DV_{CC} \leq (V_{CC} + 1.3$ V) | 3.0 | 3.3 | 3.6 | V |
| V_{TTI} | $(V_{EE} + 0.4$ V + $0.5 \times V_{ID}) < V_{TTI} < (V_{CC} + 0.5$ V) | $V_{EE} + 0.4$ | 1.8 | 3.6 | V |
| V_{TTO} | $(V_{CC} - 1.1$ V + $0.5 \times V_{OD}) < V_{TTO} < (V_{CC} + 0.5$ V) | $V_{CC} - 1.1$ | 1.8 | 3.6 | V |
| Supply Current | | | | | |
| I_{TTO} | $V_{TTO} = 1.8$ V, all outputs enabled | | 63 | 69 | mA |
| I_{CC} | $V_{CC} = 1.8$ V, all outputs enabled | | 460 | 565 | mA |
| LOGIC CHARACTERISTICS | | | | | |
| Input High, V_{IH} | $DV_{CC} = 3.3$ V | 2.5 | | | V |
| Input Low, V_{IL} | | | | 1.0 | V |
| Output High, V_{OH} | | 2.5 | | | V |
| Output Low, V_{OL} | | | | 1.0 | V |
| THERMAL CHARACTERISTICS | | | | | |
| Operating Temperature Range | | -40 | | +85 | $^{\circ}$ C |
| θ_{JA} | | | 22 | | $^{\circ}$ C/W |

¹ V_{ICM} is the input common-mode voltage.

² Programmable via I²C.

TIMING SPECIFICATIONS

Table 2. I²C Timing Parameters

| Parameter | Min | Max | Unit | Description |
|---------------------|-----|----------------|------|--|
| f _{SCL} | 0 | 400 | kHz | SCL clock frequency |
| t _{HD:STA} | 0.6 | Not applicable | μs | Hold time for a start condition |
| t _{SU:STA} | 0.6 | Not applicable | μs | Setup time for a repeated start condition |
| t _{LOW} | 1.3 | Not applicable | μs | Low period of the SCL clock |
| t _{HIGH} | 0.6 | Not applicable | μs | High period of the SCL clock |
| t _{HD:DAT} | 0 | Not applicable | μs | Data hold time |
| t _{SU:DAT} | 10 | Not applicable | ns | Data setup time |
| t _R | 1 | 300 | ns | Rise time for both SDA and SCL |
| t _F | 1 | 300 | ns | Fall time for both SDA and SCL |
| t _{SU:STO} | 0.6 | Not applicable | μs | Setup time for a stop condition |
| t _{BUF} | 1 | Not applicable | ns | Bus free time between a stop and a start condition |
| C _{IO} | 5 | 7 | pF | Capacitance for each I/O pin |
| t _{RESET} | 10 | Not applicable | ns | Reset pulse width ¹ |

¹ Reset pulse width is defined as the time $\overline{\text{RESET}}$ is held below the logic low threshold (V_{IL}) listed in Table 1 while the DV_{CC} supply is within the operating range in Table 1.

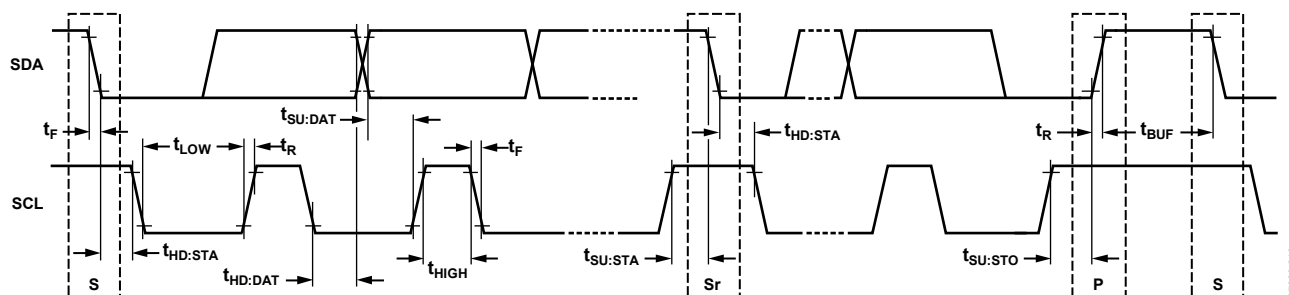


Figure 2. I²C Timing Diagram

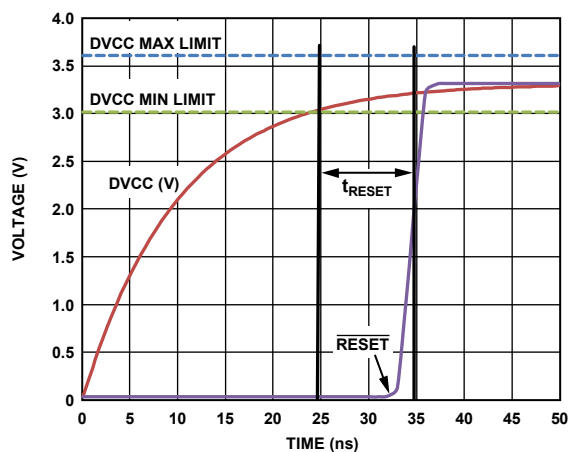


Figure 3. Reset Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|----------------------------|--|
| V_{CC} to V_{EE} | 3.7 V |
| V_{TI} | $V_{CC} + 0.6$ V |
| V_{TO} | $V_{CC} + 0.6$ V |
| Internal Power Dissipation | 4.26 W |
| Differential Input Voltage | 2.0 V |
| Logic Input Voltage | $V_{EE} - 0.3$ V < V_{IN} < $V_{CC} + 0.6$ V |
| Storage Temperature Range | -65°C to +125°C |
| Lead Temperature | 300°C |
| Junction Temperature | 125°C |

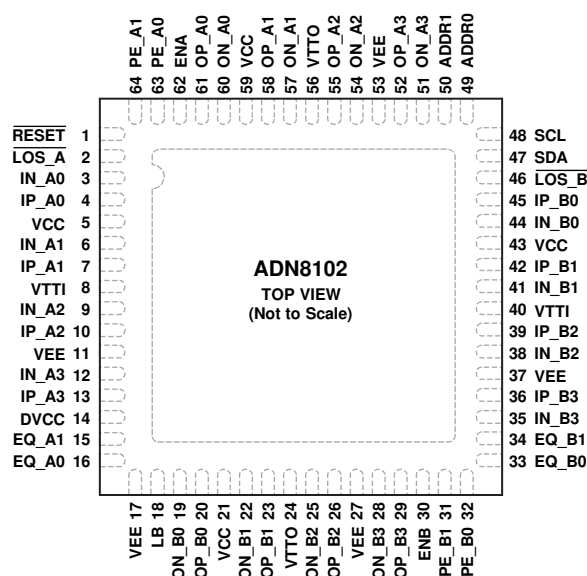
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD MUST BE CONNECTED TO VEE.

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|---------|----------|-------------|--|
| 1 | RESET | Control | Reset Input, Active Low |
| 2 | LOS_A | Digital I/O | Port A Loss of Signal Status, Active Low |
| 3 | IN_A0 | I/O | High Speed Input Complement |
| 4 | IP_A0 | I/O | High Speed Input |
| 5 | VCC | Power | Positive Supply |
| 6 | IN_A1 | I/O | High Speed Input Complement |
| 7 | IP_A1 | I/O | High Speed Input |
| 8 | VTTI | Power | Input Termination Supply |
| 9 | IN_A2 | I/O | High Speed Input Complement |
| 10 | IP_A2 | I/O | High Speed Input |
| 11 | VEE | Power | Negative Supply |
| 12 | IN_A3 | I/O | High Speed Input Complement |
| 13 | IP_A3 | I/O | High Speed Input |
| 14 | DVCC | Power | Digital Power Supply |
| 15 | EQ_A1 | Control | Port A Input Equalization MSB |
| 16 | EQ_A0 | Control | Port A Input Equalization LSB |
| 17 | VEE | Power | Negative Supply |
| 18 | LB | Control | Loopback Control |
| 19 | ON_B0 | I/O | High Speed Output Complement |
| 20 | OP_B0 | I/O | High Speed Output |
| 21 | VCC | Power | Positive Supply |
| 22 | ON_B1 | I/O | High Speed Output Complement |
| 23 | OP_B1 | I/O | High Speed Output |
| 24 | VTTI | Power | Output Termination Supply |
| 25 | ON_B2 | I/O | High Speed Output Complement |
| 26 | OP_B2 | I/O | High Speed Output |
| 27 | VEE | Power | Negative Supply |

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| Pin No. | Mnemonic | Type | Description |
|---------|---------------------------|-------------|--|
| 28 | ON_B3 | I/O | High Speed Output Complement |
| 29 | OP_B3 | I/O | High Speed Output |
| 30 | ENB | Control | Port B Enable |
| 31 | PE_B1 | Control | Port B Output Pre-Emphasis MSB |
| 32 | PE_B0 | Control | Port B Output Pre-Emphasis LSB |
| 33 | EQ_B0 | Control | Port B Input Equalization LSB |
| 34 | EQ_B1 | Control | Port B Input Equalization MSB |
| 35 | IN_B3 | I/O | High Speed Input Complement |
| 36 | IP_B3 | I/O | High Speed Input |
| 37 | VEE | Power | Negative Supply |
| 38 | IN_B2 | I/O | High Speed Input Complement |
| 39 | IP_B2 | I/O | High Speed Input |
| 40 | VTTI | Power | Input Termination Supply |
| 41 | IN_B1 | I/O | High Speed Input Complement |
| 42 | IP_B1 | I/O | High Speed Input |
| 43 | VCC | Power | Positive Supply |
| 44 | IN_B0 | I/O | High Speed Input Complement |
| 45 | IP_B0 | I/O | High Speed Input |
| 46 | $\overline{\text{LOS}}_B$ | Digital I/O | Port B Loss of Signal Status, Active Low |
| 47 | SDA | Control | I ² C Control Interface Data Input/Output |
| 48 | SCL | Control | I ² C Control Interface Clock Input |
| 49 | ADDR0 | Control | I ² C Control Interface Address LSB |
| 50 | ADDR1 | Control | I ² C Control Interface Address MSB |
| 51 | ON_A3 | I/O | High Speed Output Complement |
| 52 | OP_A3 | I/O | High Speed Output |
| 53 | VEE | Power | Negative Supply |
| 54 | ON_A2 | I/O | High Speed Output Complement |
| 55 | OP_A2 | I/O | High Speed Output |
| 56 | VTT0 | Power | Output Termination Supply |
| 57 | ON_A1 | I/O | High Speed Output Complement |
| 58 | OP_A1 | I/O | High Speed Output |
| 59 | VCC | Power | Positive Supply |
| 60 | ON_A0 | I/O | High Speed Output Complement |
| 61 | OP_A0 | I/O | High Speed Output |
| 62 | ENA | Control | Port A Enable |
| 63 | PE_A0 | Control | Port A Output Pre-Emphasis LSB |
| 64 | PE_A1 | Control | Port A Output Pre-Emphasis MSB |
| EP | EPAD | Power | EPAD Must Be Connected to VEE |

TYPICAL PERFORMANCE CHARACTERISTICS

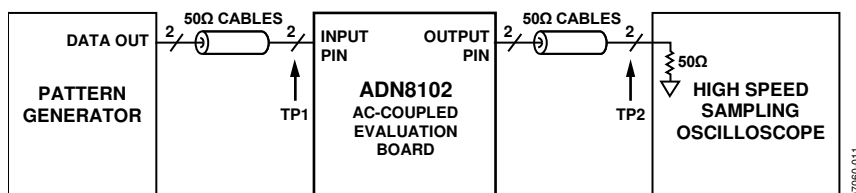


Figure 5. Standard Test Circuit (No Channel)

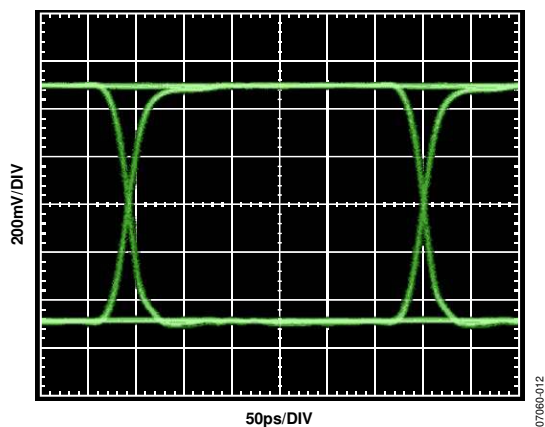


Figure 6. 3.25 Gbps Input Eye (TP1 from Figure 5)

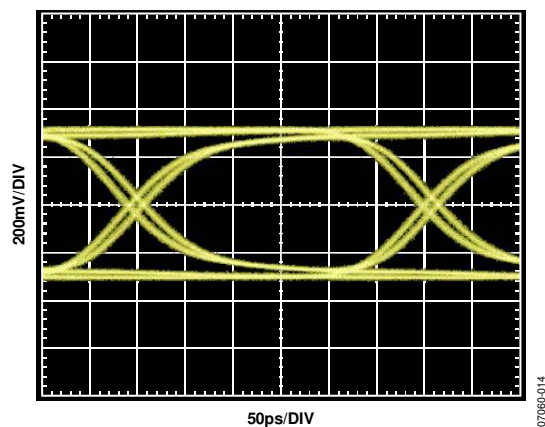


Figure 8. 3.25 Gbps Output Eye, No Channel (TP2 from Figure 5)

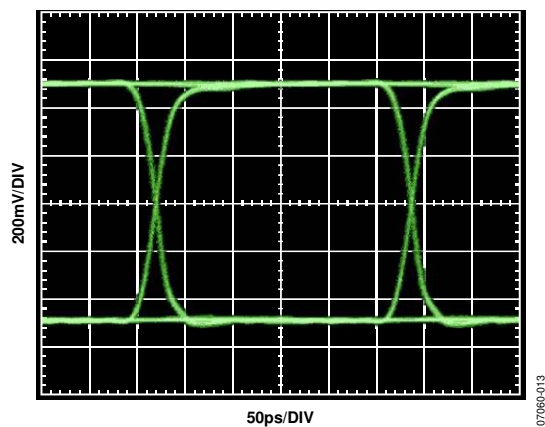


Figure 7. 3.75 Gbps Input Eye (TP1 from Figure 5)

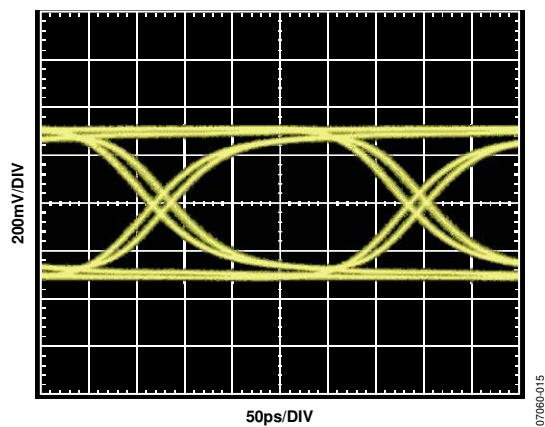


Figure 9. 3.75 Gbps Output Eye, No Channel (TP2 from Figure 5)

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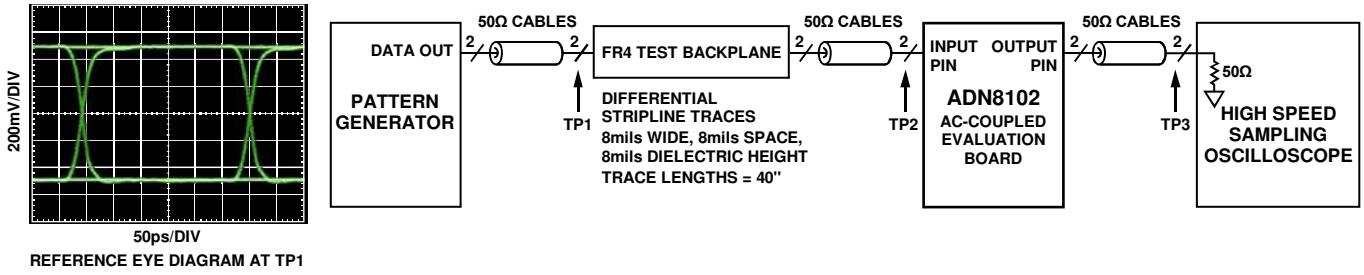


Figure 10. Input Equalization Test Circuit, FR4

07060-016

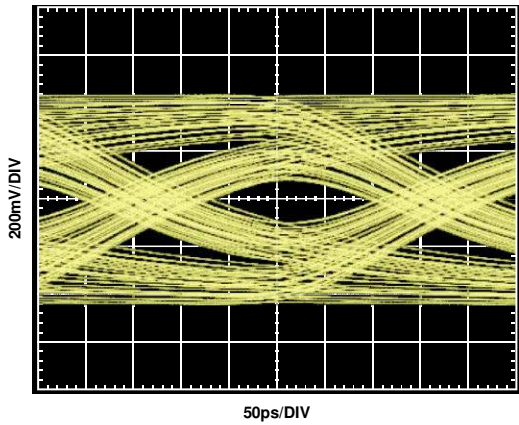


Figure 11. 3.25 Gbps Input Eye, 40 Inch FR4 Input Channel (TP2 from Figure 10)

07060-017

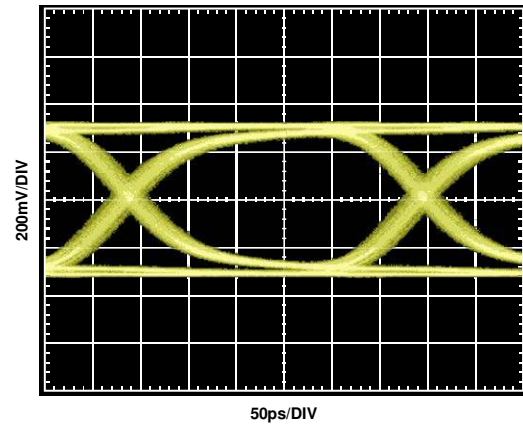


Figure 13. 3.25 Gbps Output Eye, 40 Inch FR4 Input Channel, Best EQ Setting (TP3 from Figure 10)

07060-019

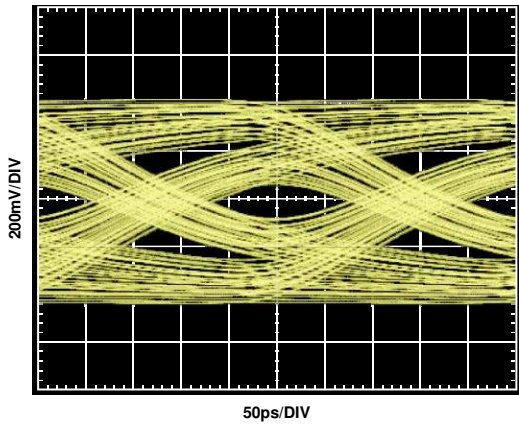


Figure 12. 3.75 Gbps Input Eye, 40 Inch FR4 Input Channel (TP2 from Figure 10)

07060-018

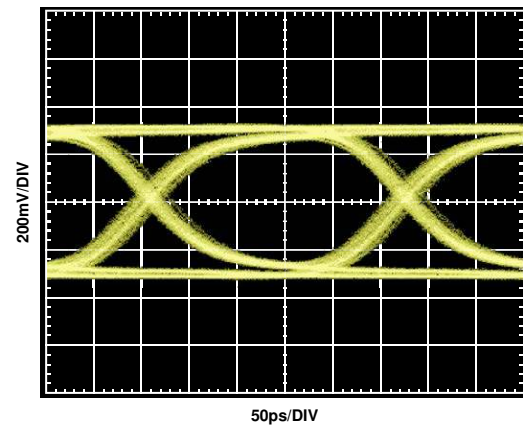


Figure 14. 3.75 Gbps Output Eye, 40 Inch FR4 Input Channel, Best EQ Setting (TP3 from Figure 10)

07060-020

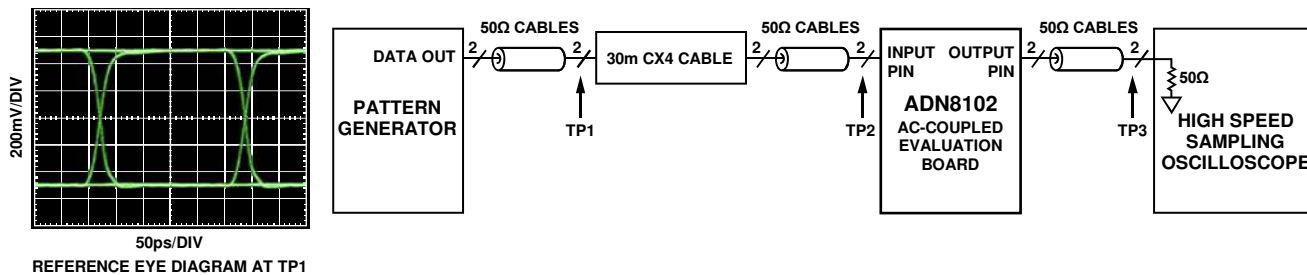


Figure 15. Input Equalization Test Circuit, CX4

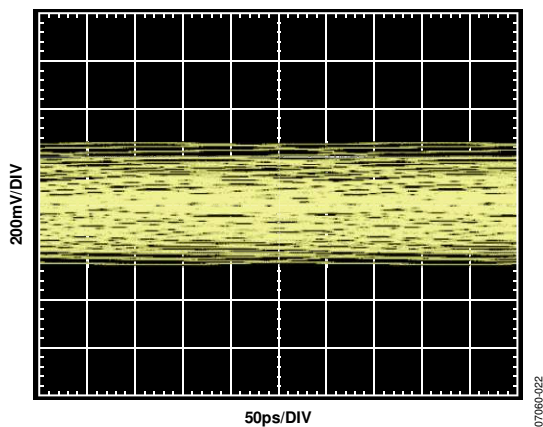


Figure 16. 3.25 Gbps Input Eye, 30 Meters CX4 Cable (TP2 from Figure 15)

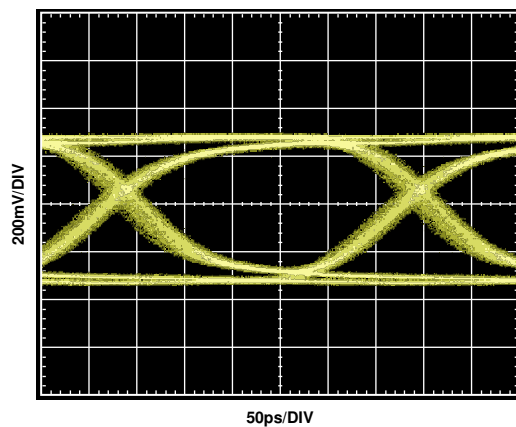


Figure 18. 3.25 Gbps Output Eye, 30 Meters CX4 Cable, Best EQ Setting (TP3 from Figure 15)

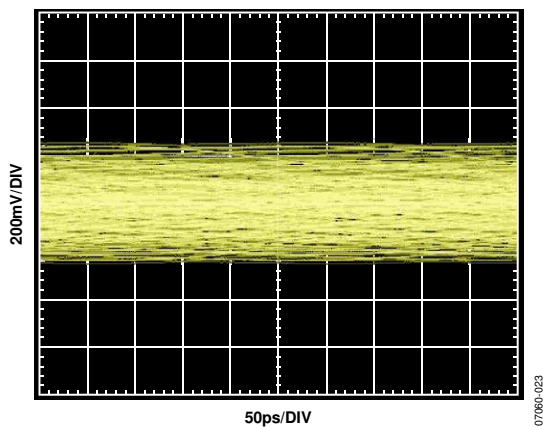


Figure 17. 3.75 Gbps Input Eye, 30 Meters CX4 Cable (TP2 from Figure 15)

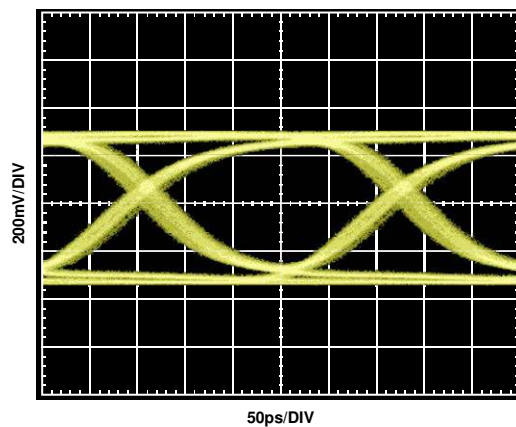


Figure 19. 3.75 Gbps Output Eye, 30 Meters CX4 Cable, Best EQ Setting (TP3 from Figure 15)

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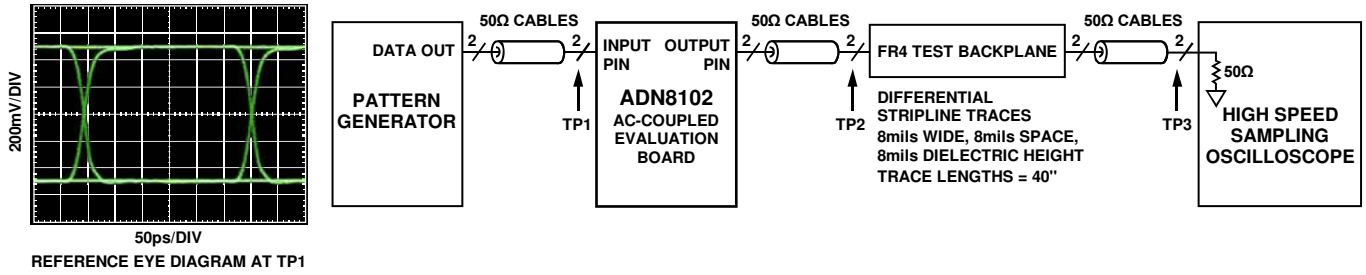


Figure 20. Output Pre-Emphasis Test Circuit, FR4

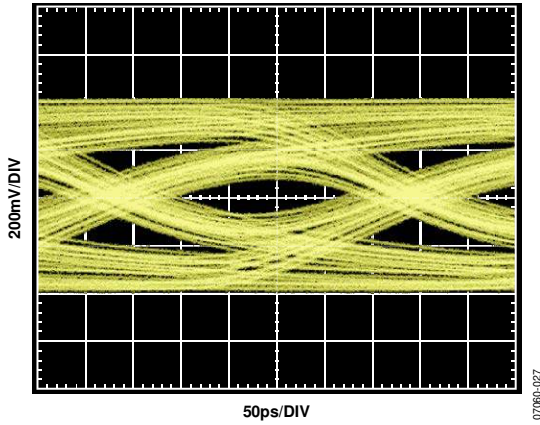


Figure 21. 3.25 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = 0 (TP3 from Figure 20)

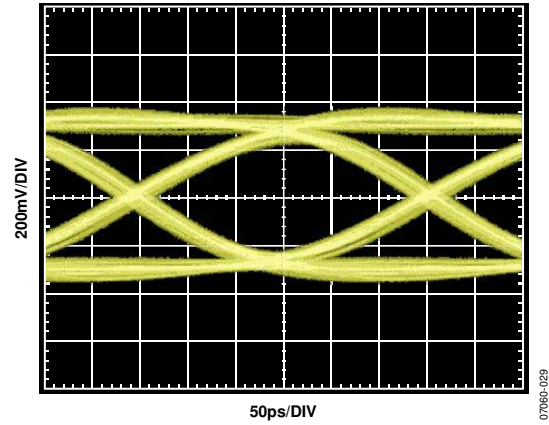


Figure 23. 3.25 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = Best Setting (TP3 from Figure 20)

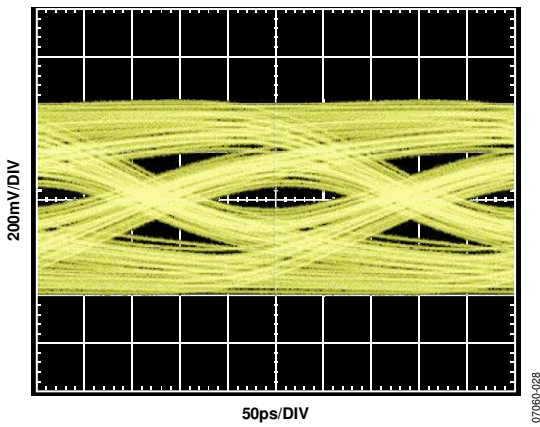


Figure 22. 3.75 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = 0 (TP3 from Figure 20)

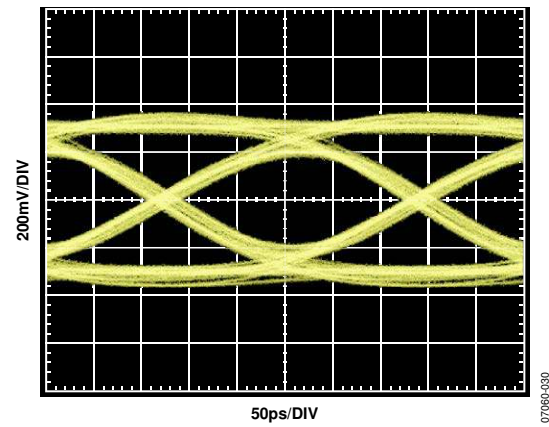


Figure 24. 3.75 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = Best Setting (TP3 from Figure 20)

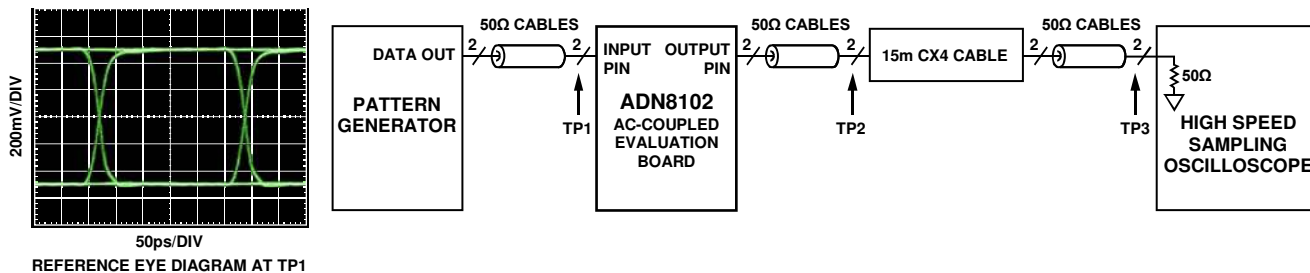


Figure 25. Output Pre-Emphasis Test Circuit, CX4

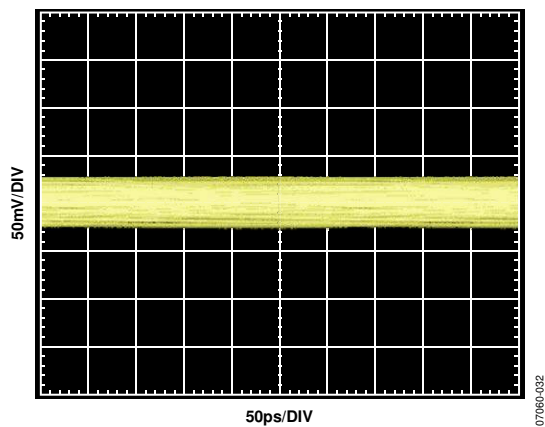


Figure 26. 3.25 Gbps Output Eye, 15 Meters CX4 Cable, PE = 0 (TP3 from Figure 25)

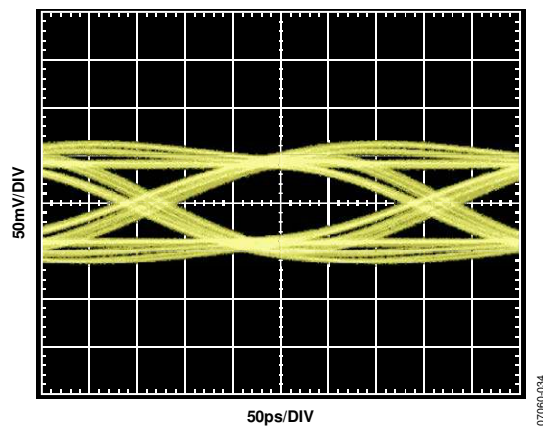


Figure 28. 3.25 Gbps Output Eye, 15 Meters CX4 Cable, PE = Best Setting (TP3 from Figure 25)

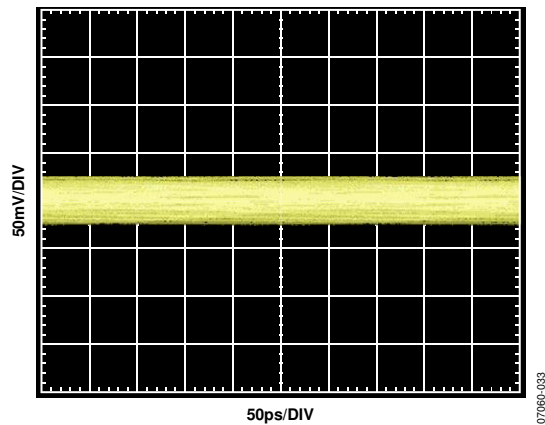


Figure 27. 3.75 Gbps Output Eye, 15 Meters CX4 Cable, PE = 0 (TP3 from Figure 25)

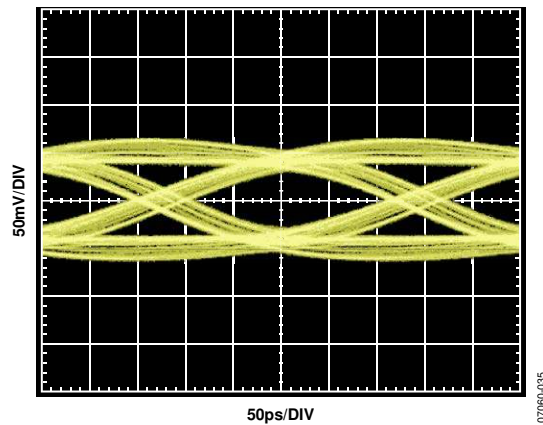


Figure 29. 3.75 Gbps Output Eye, 15 Meters CX4 Cable, PE = Best Setting (TP3 from Figure 25)

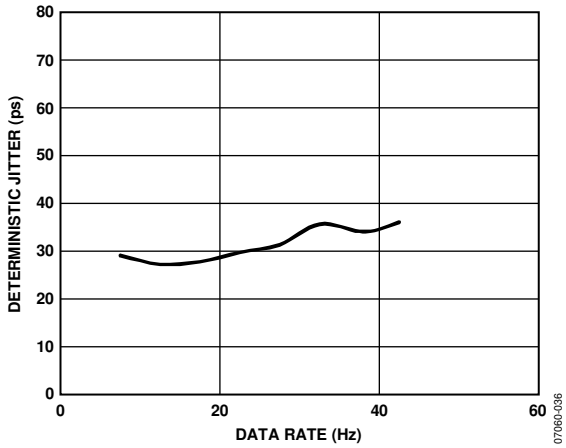


Figure 30. Deterministic Jitter vs. Data Rate

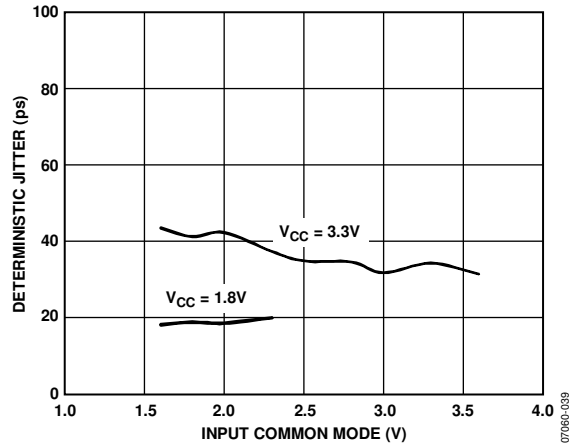


Figure 33. Deterministic Jitter vs. Input Common Mode

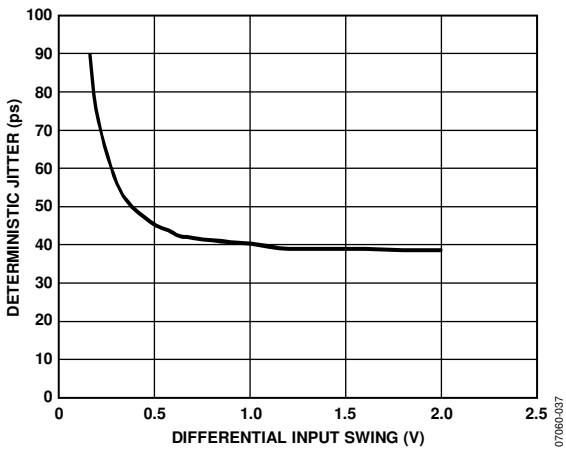


Figure 31. Deterministic Jitter vs. Differential Input Swing

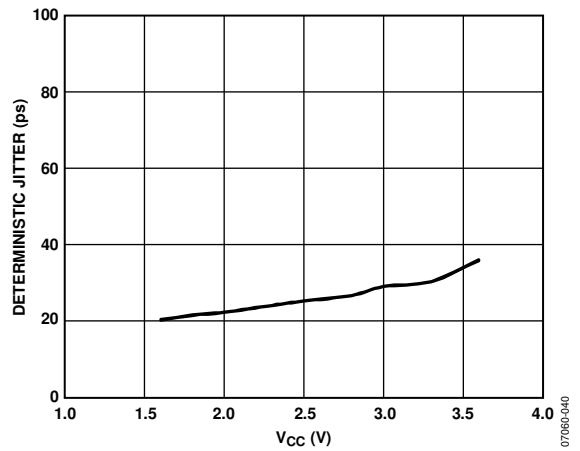


Figure 34. Deterministic Jitter vs. Supply Voltage (V_{CC})

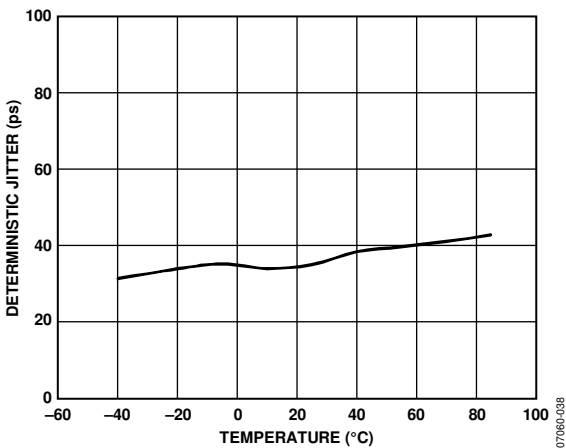


Figure 32. Deterministic Jitter vs. Temperature

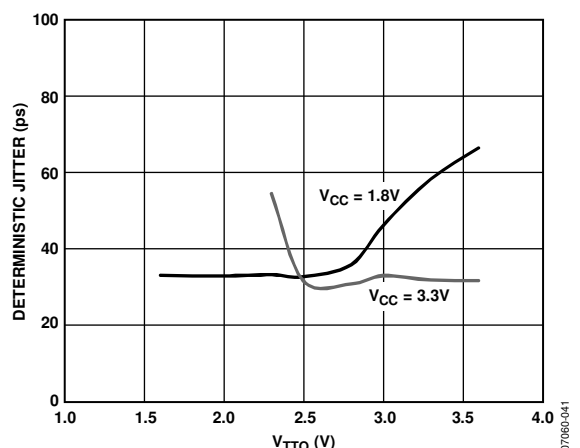


Figure 35. Deterministic Jitter vs. Output Termination Voltage (V_{TT0})

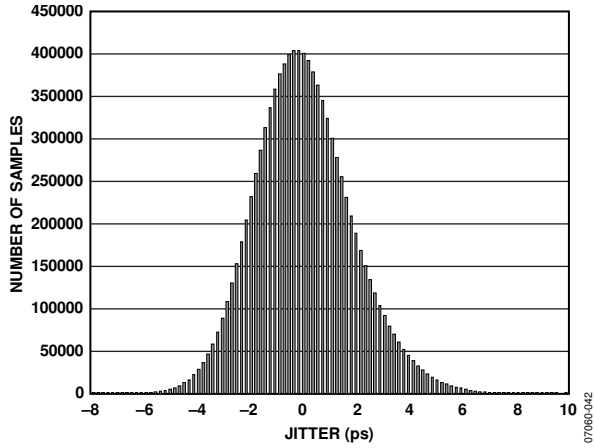


Figure 36. Random Jitter Histogram

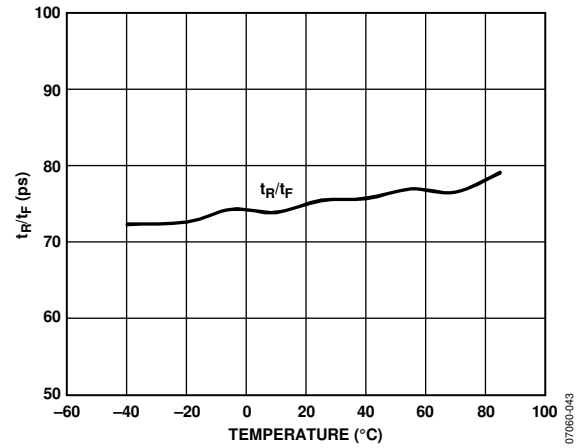


Figure 37. Rise Time (t_R)/Fall Time (t_F) vs. Temperature

THEORY OF OPERATION

INTRODUCTION

The ADN8102 is a quad, bidirectional cable and backplane equalizer that provides both input equalization and output pre-emphasis on both the line card and cable sides of the device. The device supports full loopback and through connectivity of the two unidirectional half-links, each consisting of four differential signal pairs.

The ADN8102 offers extensively programmable output levels and pre-emphasis as well as the ability to disable the output current. The receivers integrate a programmable, multizero equalizer transfer function that is optimized to compensate either typical backplane or typical cable losses.

The I/O on-chip termination resistors are terminated to user-settable supplies to support dc coupling in a wide range of logic styles. The ADN8102 supports a wide core supply range; V_{CC} can be set from 1.8 V to 3.3 V. These features, together with programmable output levels, allow for a wide range of dc- and ac-coupled I/O configurations.

The ADN8102 supports several control and configuration modes, as shown in Table 5. The pin control mode offers access to a subset of the total feature list but allows for a much simplified control scheme. The primary advantage of using the serial control interface is that it allows finer resolution in setting receive equalization, transmitter preemphasis, loss-of-signal (LOS) behavior, and output levels.

By default, the ADN8102 starts in pin control mode. Strobing the **RESET** pin sets all on-chip registers to their default values and uses pins to configure loopback, PE, and EQ levels. In

mixed mode, loopback is still controlled through the external pin. The user can override PE and EQ settings in mixed mode. In serial mode, all functions are accessed through registers, and the control pin inputs are ignored, except **RESET**.

The ADN8102 register set is controlled through a 2-wire, I²C interface. The ADN8102 acts only as an I²C slave device. The 7-bit slave address for the ADN8102 I²C interface contains the static value b10010 for the upper four bits. The lower two bits are controlled by the input pins, ADDR[1:0]

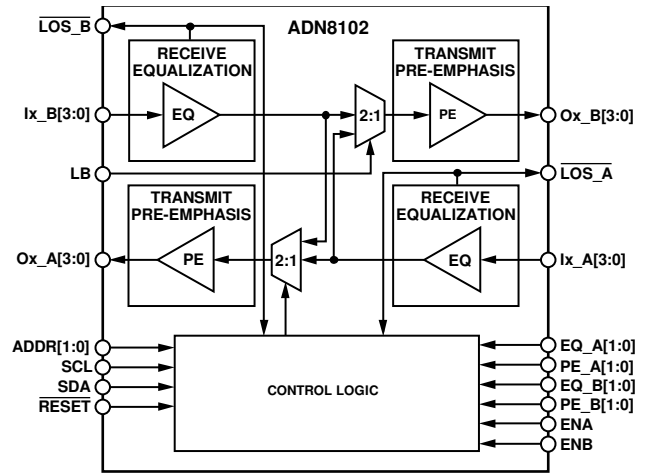


Figure 38. Simplified Functional Block Diagram

Table 5. Control Interface Mode Register

| Address | Default | Register Name | Bit | Bit Name | Functionality Description |
|---------|---------|------------------------|------------|-----------------------|--|
| 0x0F | 0x00 | Control interface mode | 7:2 1:0 | Reserved MODE[1:0] | Set to 0. 00 = toggle pin control. Asynchronous control through toggle pins only. 01 = Loopback control via toggle pins, equalization, and preemphasis via register-based control through the I ² C serial interface. 10 = Equalization and preemphasis via toggle pins and loopback control via register-based control through the I ² C serial interface. 11 = serial control. Register-based control through the I ² C serial interface. |

RECEIVERS

Input Structure and Input Levels

The ADN8102 receiver inputs incorporate 50 Ω termination resistors, ESD protection, and a multizero transfer function equalizer that can be optimized for backplane or cable operation. Each channel also provides a programmable LOS function that provides an interrupt that can be used to squelch or disable the associated output when the differential input voltage falls below the programmed threshold value. Each receive channel also provides a P/N inversion function that allows the user to swap the sign of the input signal path to eliminate the need for board-level crossovers in the receiver channel.

Table 6 illustrates some, but not all, possible combinations of input supply voltages.

Table 6. Common Input Voltage Levels

| Configuration | V _{CC} (V) | V _{TTI} (V) |
|---|---------------------|----------------------|
| Low V _{TTI} , ac-coupled input | 1.8 | 1.6 |
| Single 1.8 V supply | 1.8 | 1.8 |
| 3.3 V core | 3.3 | 1.8 |
| Single 3.3 V supply | 3.3 | 3.3 |

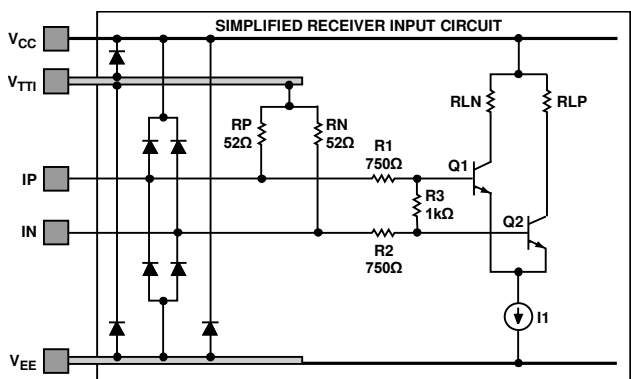


Figure 39. Simplified Input Structure

EQUALIZATION SETTINGS

The ADN8102 receiver incorporates a multizero transfer function, continuous time equalizer that provides up to 22 dB of high frequency boost at 1.875 GHz to compensate up to 30 meters of CX4 cable or 40 inches of FR4 at 3.75 Gbps. The ADN8102 allows joint control of the equalizer transfer function of the four equalizer channels in a single port through the I²C control interface. Port A and Port B equalizer transfer functions are controlled via Register 0x80 and Register 0xA0, respectively. The equalizer transfer function allows independent control of the boost in two different frequency ranges for optimal matching with the loss shape of the user’s channel (for example, skin-effect loss dominated or dielectric loss dominated). By default, the equalizer control is simplified to two independent look up tables (LUT) of basic settings that provide nine settings, each optimized for CX4 cable and FR4 to ease programming for

typical channels. The default state of the part selects the CX4 optimized equalization map for the IN_A[3:0] channels that interface with the cable and the FR4 optimized equalization map for the IN_B[3:0] channels that interface with the board. Full control of the equalizer is available via the I²C control interface by writing MODE[0] = 1 at Address 0x0F. Table 8 summarizes the high frequency boost for each of the basic control settings and the typical length of CX4 cable and FR4 trace that each setting compensates. Setting the EQBY bit of the IN_A/IN_B configuration registers high sets the equalization to 1.5 dB of boost, which compensates 0 meters to 2 meters of CX4 or 0 inches to 5 inches of FR4.

Setting the LUT SELECT bit = 1 (Bit 1 in the IN_Ax/IN_Bx FR4 control registers) allows the default map selection (CX4 or FR4 optimized) to be overwritten via the LUT FR4/CX4 bit (Bit 0) in the IN_Ax/IN_Bx FR4 control registers. Setting this bit high selects the FR4 optimized map, and setting it low selects the CX4 optimized map. These settings are set on a per channel basis (see Table 9 and Table 22).

Table 7.

| LUT SELECT | LUT FR4/CX4 | Description |
|-------------|----------------|--|
| 0 (default) | X ¹ | Port A eq optimized for CX4 cable Port B eq optimized for FR4 PCB trace |
| 1 | 0 | Eq optimized for CX4 cable |
| 1 | 1 | Eq optimized for FR4 PCB trace |

¹ X = don't care.

Advanced Equalization Settings

The user can also specify the boost in the midfrequency and high frequency ranges independently. This is done by writing to the IN_A/IN_B EQ1 control and IN_A/IN_B EQ2 control registers for the channel of interest. Each of these registers provides 32 settings of boost, with IN_A/IN_B EQ1 control setting the midfrequency boost and IN_A/IN_B EQ2 control setting the high frequency boost. The IN_A/IN_B EQx control registers are ordered such that Bit 5 is a sign bit, and midlevel boost is centered on 0x00; setting Bit 5 low and increasing the LSBs results in decreasing boost, while setting Bit 5 high and increasing the LSBs results in increasing boost. The EQ CTL SRC bit (Bit 6) in the IN_A/IN_B EQ1 control registers determines whether the equalization control for the channel of interest is selected from the optimized map or directly from the IN_A/IN_B EQx control registers (per port). Setting this bit high selects equalization control directly from the IN_A/IN_B EQx control registers, and setting it low selects equalization control from the selected optimized map.

Table 8. Receive Equalizer Boost vs. Setting (CX4 and FR4 Optimized Maps)

| EQ_A[1:0] and EQ_B[1:0] Pins | IN_Ax/IN_Bx Configuration, EQ[2:0] | EQBY | Cable Optimized | | FR4 Optimized | |
|------------------------------|------------------------------------|------|-----------------|-----------------------------------|---------------|-----------------------------------|
| | | | Boost (dB) | Typical CX4 Cable Length (Meters) | Boost (dB) | Typical FR4 Trace Length (Inches) |
| 0 | X ¹ | 1 | 1.5 | < 2 | 1.5 | < 5 |
| | 0 | 0 | 10 | 2 to 6 | 3.5 | 5 to 10 |
| | 1 | 0 | 12 | 8 to 10 | 3.9 | 10 to 15 |
| 1 | 2 | 0 | 14 | 12 to 14 | 4.25 | 15 to 20 |
| | 3 | 0 | 17 | 16 to 18 | 4.5 | 20 to 25 |
| | 4 | 0 | 19 | 20 to 22 | 4.75 | 25 to 30 |
| 2 | 5 | 0 | 20 | 24 to 26 | 5.0 | 30 to 35 |
| | 6 | 0 | 21 | 28 to 30 | 5.3 | 35 to 40 |
| 3 | 7 | 0 | 22 | 30 to 32 | 5.5 | 35 to 40 |

¹ X = Don't care

Table 9. Receive Configuration and Equalization Registers

| Name | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default |
|-------------------------|--|-------|------------|--------|--------|--------|--------|------------|-------------|---------|
| IN_A/IN_B configuration | 0x80, 0xA0 | | PNSWAP | EQBY | EN | | EQ[2] | EQ[1] | EQ[0] | 0x30 |
| IN_A/IN_B EQ1 control | 0x83, 0xA3 | | EQ CTL SRC | EQ1[5] | EQ1[4] | EQ1[3] | EQ1[2] | EQ1[1] | EQ1[0] | 0x00 |
| IN_A/IN_B EQ2 control | 0x84, 0xA4 | | | EQ2[5] | EQ2[4] | EQ2[3] | EQ2[2] | EQ2[1] | EQ2[0] | 0x00 |
| IN_Ax/IN_Bx FR4 control | 0x85, 0x8D, 0x95, 0x9D, 0xA5, 0xAD, 0xB5, 0xBD | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |

Loss of Signal/Signal Detect

An independent signal detect output is provided for all eight input ports of the device. The signal-detect function measures the low frequency amplitude of the signal at the receiver input and compares this measurement with a defined threshold level. If the measurement indicates that the input signal swing is smaller than the threshold for 250 μ s, the channel indicates a loss-of-signal event. Assertion and deassertion of the LOS signal occurs within 100 μ s of the event.

The LOS-assert and LOS-deassert levels are set on a per channel basis through the I²C control interface, by writing to the IN_A/IN_B LOS threshold and IN_A/IN_B LOS hysteresis registers, respectively. The recommended settings are IN_A/IN_B LOS threshold = 0x0C and IN_A/IN_B LOS hysteresis = 0x0D. All ports are factory tested with these settings to ensure that an LOS event is asserted for single-ended dc input swings less than 20 mV and is deasserted for single-ended dc input swings greater than 225 mV.

The LOS status for each individual channel can be accessed through the I²C control interface. The independent channel LOS status can be read from the IN_A/IN_B LOS status registers (Address 0x1F and Address 0x3F). The four LSBs of each register represent the current LOS status of each channel, with high representing an ongoing LOS event. The four MSBs of each

register represent the historical LOS status of each channel, with high representing a LOS event at any time on a specific channel. The MSBs are sticky and remain high once asserted until cleared by the user by overwriting the bits to 0.

Recommended LOS Settings

Recommended settings for LOS are as follows:

- Set IN_A/IN_B LOS threshold to 0x0C for an assert voltage of 20 mV differential (40 mV p-p differential).
- Set IN_A/IN_B LOS hysteresis to 0x0D for a deassert voltage of 225 mV differential (450 mV p-p differential).

LANE INVERSION

The input P/N inversion is a feature intended to allow the user to implement the equivalent of a board-level crossover in a much smaller area and without additional via impedance discontinuities that degrade the high frequency integrity of the signal path. The P/N inversion is available on a per port basis and is controlled through the I²C control interface. The P/N inversion is accomplished by writing to the PNSWAP bit (Bit 6) of the IN_A/IN_B configuration register (see Table 9) with low representing a noninverting configuration and high representing an inverting configuration. Note that using this feature to account for signal inversions downstream of the receiver requires additional attention when switching connectivity.

Table 10. LOS Threshold and Hysteresis Control Registers

| Name | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default |
|-----------------------------|---------------|-------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---------|
| IN_A/IN_B LOS threshold | 0x81, 0xA1 | | THRESH[6] | THRESH[5] | THRESH[4] | THRESH[3] | THRESH[2] | THRESH[1] | THRESH[0] | 0x04 |
| IN_A/IN_B LOS hysteresis | 0x82, 0xA2 | | HYST[6] | HYST[5] | HYST[4] | HYST[3] | HYST[2] | HYST[1] | HYST[0] | 0x12 |

Table 11. LOS Status Registers

| Name | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------|---------------|------------------|------------------|------------------|---------------|---------------------|---------------------|---------------------|---------------------|
| IN_A/IN_B LOS status | 0x1F, 0x3F | STICKY LOS[3] | STICKY LOS[2] | STICKY LOS[1] | STICKY LOS[0] | REAL-TIME LOS[3] | REAL-TIME LOS[2] | REAL-TIME LOS[1] | REAL-TIME LOS[0] |

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LOOPBACK

The ADN8102 provides loopback on both input ports (Port A: cable interface input, and Port B: line card interface input). The external loopback toggle pin, LB, controls the loopback of the Port B input only (board side loopback). When loopback is asserted, valid data continues to pass through the Port B link, but the Port B input signals are also shunted to the Port A output to allow testing and debugging without disrupting valid data. This loopback, as well as loopback of the Port A input (cable side loopback), can be programmed through the I²C interface. The loopbacks are controlled through the I²C interface by writing to Bit 0 and Bit 1 of the loopback control register (Register 0x02).

Bit 0 represents loopback of the Port A inputs to the Port B outputs (cable side loopback). Bit 1 represents loopback of the Port B inputs to the Port A outputs (board side loopback), with high representing loopback for both bits. Bit 1 can be overridden by the LB pin if the pin mode register is set to enable loopback via external pin as shown in Table 5. Both input ports can be looped back simultaneously (full loopback) by writing high to both Bit 0 and Bit 1, but in this case, valid data is disrupted on each channel. Figure 40 illustrates the three loopback modes.

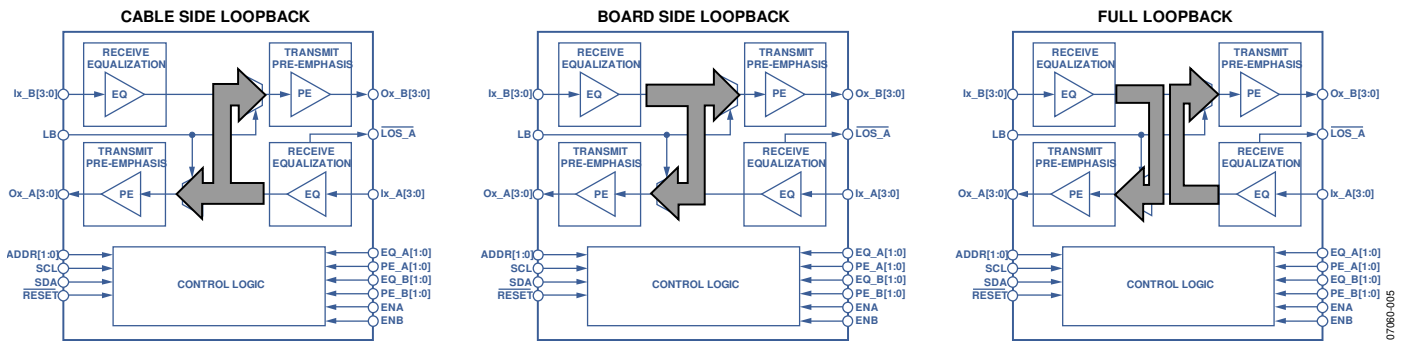


Figure 40. Loopback Modes of Operation

Table 12. Loopback Control Functionality

| Control Mode ¹ | LB Pin | LB[1] | LB[0] | Description |
|---------------------------|--------|----------------|-------|-----------------------------|
| Pin Control (00 or 01) | 0 | X ² | X | Loopback disabled |
| | 1 | X | X | Board side loopback enabled |
| Serial Control (10 or 11) | X | 0 | 0 | Loopback disabled |
| | X | 0 | 1 | Cable side loopback enabled |
| | X | 1 | 0 | Board side loopback enabled |
| | X | 1 | 1 | Full loopback enabled |

¹ Refer to Table 5 for additional information regarding control mode settings.

² X = don't care.

Table 13. Loopback Control Register

| Name | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default |
|------------------|---------|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| Loopback control | 0x02 | | | | | | | LB[1] | LB[0] | 0x00 |

TRANSMITTERS

Output Structure and Output Levels

The ADN8102 transmitter outputs incorporate 50 Ω termination resistors, ESD protection, and an output current switch. Each port provides control of both the absolute output level and the pre-emphasis output level. It should be noted that the choice of output level affects the output common-mode level. A 600 mV peak-to-peak differential output level with full pre-emphasis range requires an output termination voltage of 2.5 V or greater ($V_{TTO}, V_{CC} \geq 2.5\text{ V}$).

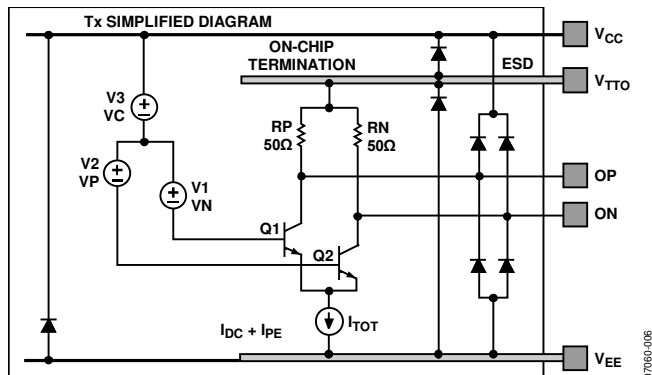


Figure 41. Simplified Output Structure

Pre-Emphasis

The total output amplitude and pre-emphasis setting space is reduced to a single map of basic settings that provide seven settings of output equalization to ease programming for typical channels. The PE_A/PE_B[1:0] pins provide selections 0, 2, 4, and 6 of the seven pre-emphasis settings through toggle pin control, covering the entire range of settings at lower resolution. The full resolution of seven settings is available through the I²C interface by writing to Bits[2:0] (PE[2:0] of the OUT_A/OUT_B configuration registers) with I²C settings overriding the toggle

pin control. Similar to the receiver settings, the ADN8102 allows joint control of all four channels in a transmit port. Table 15 summarizes the absolute output level, pre-emphasis level, and high frequency boost for each of the basic control settings and the typical length of the CX4 cable and FR4 trace that each setting compensates.

Full control of the transmit output levels is available through the I²C control interface. This full control is achieved by writing to the OUT_A/OUT_B Output Level Control[1:0] registers for the channel of interest. Table 17 shows the supported output level settings of the OUT_A/OUT_B Output Level Control[1:0] registers. Register settings not listed in Table 17 are not supported by the ADN8102.

The output equalization is optimized for less than 1.75 Gbps operation but can be optimized for higher speed applications at up to 3.75 Gbps through the I²C control interface by writing to the DATA RATE bit (Bit 4) of the OUT_A/OUT_B configuration registers, with high representing 3.75 Gbps and low representing 1.75 Gbps. The PE CTL SRC bit (Bit 7) in the OUT_A/OUT_B Output Level Control 1 register determines whether the pre-emphasis and output current controls for the channel of interest are selected from the optimized map or directly from the OUT_A/OUT_B Output Level Control[1:0] registers (per channel). Setting this bit high selects pre-emphasis control directly from the OUT_A/OUT_B Output Level Control[1:0] registers, and setting it low selects pre-emphasis control from the optimized map.

Table 14. Data Rate Select

| OUT_A/OUT_B Configuration Bit 4 | Supported Data Rates |
|---------------------------------|------------------------|
| 0 (default) | 0 Gbps to 1.75 Gbps |
| 1 | 1.75 Gbps to 3.75 Gbps |

Table 15. Transmit Pre-Emphasis Boost and Overshoot vs. Setting

| PE[2:0] Register | PE[1:0] Pins | Boost (dB) | Overshoot (%) | DC Swing (mV p-p diff) | Typical CX4 Cable Length (Meters) | Typical FR4 Trace Length (Inches) |
|------------------|----------------|------------|---------------|------------------------|-----------------------------------|-----------------------------------|
| 0 | 0 | 0 | 0 | 800 | 0 to 2.5 | 0 to 5 |
| 1 | Not applicable | 2 | 25 | 800 | 2.5 to 5 | 0 to 5 |
| 2 | 1 | 3.5 | 50 | 800 | 5 to 7.5 | 10 to 15 |
| 3 | Not applicable | 4.9 | 75 | 800 | 7.5 to 10 | 10 to 15 |
| 4 | 2 | 6 | 100 | 800 | 10 to 12.5 | 15 to 20 |
| 5 | Not applicable | 7.4 | 133 | 600 | 15 to 17.5 | 20 to 25 |
| 6 | 4 | 9.5 | 200 | 400 | 20 to 22.5 | 25 to 30 |

Table 16. Output Configuration Registers

| Name | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default | |
|------------------------------------|------------|------------|-----------------|-------|-----------|-------|-------|-------|-------|---------|------|
| OUT_A/OUT_B configuration | 0xC0, 0xE0 | | | EN | DATA RATE | | PE[2] | PE[1] | PE[0] | 0x20 | |
| OUT_A/OUT_B Output Level Control 1 | 0xC1, 0xE1 | PE CTL SRC | OUTx_OLEV1[6:0] | | | | | | | | 0x40 |
| OUT_A/OUT_B Output Level Control 0 | 0xC2, 0xE2 | | OUTx_OLEV0[6:0] | | | | | | | | 0x40 |

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Table 17. Output Level Settings

| V _{SW-DC} (mV) | V _{SW-PE} (mV) | V _{DPP-DC} (mV) | V _{DPP-PE} (mV) | PE (dB) | I _{TOT} (mA) | OUT_A/OUT_B OLEV 0 | OUT_A/OUT_B OLEV 1 |
|-------------------------|-------------------------|--------------------------|--------------------------|---------|-----------------------|--------------------|--------------------|
| 50 | 50 | 100 | 100 | 0.00 | 2 | 0x00 | 0x81 |
| 50 | 150 | 100 | 300 | 9.54 | 6 | 0x11 | 0x81 |
| 50 | 250 | 100 | 500 | 13.98 | 10 | 0x22 | 0x81 |
| 50 | 350 | 100 | 700 | 16.90 | 14 | 0x33 | 0x81 |
| 50 | 450 | 100 | 900 | 19.08 | 18 | 0x44 | 0x81 |
| 50 | 550 | 100 | 1100 | 20.83 | 22 | 0x55 | 0x81 |
| 50 | 650 | 100 | 1300 | 22.28 | 26 | 0x66 | 0x81 |
| 100 | 100 | 200 | 200 | 0.00 | 4 | 0x00 | 0x91 |
| 100 | 200 | 200 | 400 | 6.02 | 8 | 0x11 | 0x91 |
| 100 | 300 | 200 | 600 | 9.54 | 12 | 0x22 | 0x91 |
| 100 | 400 | 200 | 800 | 12.04 | 16 | 0x33 | 0x91 |
| 100 | 500 | 200 | 1000 | 13.98 | 20 | 0x44 | 0x91 |
| 100 | 600 | 200 | 1200 | 15.56 | 24 | 0x55 | 0x91 |
| 100 | 700 | 200 | 1400 | 16.90 | 28 | 0x66 | 0x91 |
| 150 | 150 | 300 | 300 | 0.00 | 6 | 0x00 | 0x92 |
| 150 | 250 | 300 | 500 | 4.44 | 10 | 0x11 | 0x92 |
| 150 | 350 | 300 | 700 | 7.36 | 14 | 0x22 | 0x92 |
| 150 | 450 | 300 | 900 | 9.54 | 18 | 0x33 | 0x92 |
| 150 | 550 | 300 | 1100 | 11.29 | 22 | 0x44 | 0x92 |
| 150 | 650 | 300 | 1300 | 12.74 | 26 | 0x55 | 0x92 |
| 150 | 750 | 300 | 1500 | 13.98 | 30 | 0x66 | 0x92 |
| 200 | 200 | 400 | 400 | 0.00 | 8 | 0x00 | 0xA2 |
| 200 | 300 | 400 | 600 | 3.52 | 12 | 0x11 | 0xA2 |
| 200 | 400 | 400 | 800 | 6.02 | 16 | 0x22 | 0xA2 |
| 200 | 500 | 400 | 1000 | 7.96 | 20 | 0x33 | 0xA2 |
| 200 | 600 | 400 | 1200 | 9.54 | 24 | 0x44 | 0xA2 |
| 200 | 700 | 400 | 1400 | 10.88 | 28 | 0x55 | 0xA2 |
| 200 | 800 | 400 | 1600 | 12.04 | 32 | 0x66 | 0xA2 |
| 250 | 250 | 500 | 500 | 0.00 | 10 | 0x00 | 0xA3 |
| 250 | 350 | 500 | 700 | 2.92 | 14 | 0x11 | 0xA3 |
| 250 | 450 | 500 | 900 | 5.11 | 18 | 0x22 | 0xA3 |
| 250 | 550 | 500 | 1100 | 6.85 | 22 | 0x33 | 0xA3 |
| 250 | 650 | 500 | 1300 | 8.30 | 26 | 0x44 | 0xA3 |
| 250 | 750 | 500 | 1500 | 9.54 | 30 | 0x55 | 0xA3 |
| 250 | 850 | 500 | 1700 | 10.63 | 34 | 0x66 | 0xA3 |
| 300 | 300 | 600 | 600 | 0.00 | 12 | 0x00 | 0xB3 |
| 300 | 400 | 600 | 800 | 2.50 | 16 | 0x11 | 0xB3 |
| 300 | 500 | 600 | 1000 | 4.44 | 20 | 0x22 | 0xB3 |
| 300 | 600 | 600 | 1200 | 6.02 | 24 | 0x33 | 0xB3 |
| 300 | 700 | 600 | 1400 | 7.36 | 28 | 0x44 | 0xB3 |
| 300 | 800 | 600 | 1600 | 8.52 | 32 | 0x55 | 0xB3 |
| 300 | 900 | 600 | 1800 | 9.54 | 36 | 0x66 | 0xB3 |
| 350 | 350 | 700 | 700 | 0.00 | 14 | 0x00 | 0xB4 |
| 350 | 450 | 700 | 900 | 2.18 | 18 | 0x11 | 0xB4 |
| 350 | 550 | 700 | 1100 | 3.93 | 22 | 0x22 | 0xB4 |
| 350 | 650 | 700 | 1300 | 5.38 | 26 | 0x33 | 0xB4 |
| 350 | 750 | 700 | 1400 | 6.62 | 30 | 0x44 | 0xB4 |
| 350 | 850 | 700 | 1700 | 7.71 | 34 | 0x55 | 0xB4 |
| 350 | 950 | 700 | 1900 | 8.67 | 38 | 0x66 | 0xB4 |
| 400 | 400 | 800 | 800 | 0.00 | 16 | 0x00 | 0xC4 |
| 400 | 500 | 800 | 1000 | 1.94 | 20 | 0x11 | 0xC4 |
| 400 | 600 | 800 | 1200 | 3.52 | 24 | 0x22 | 0xC4 |
| 400 | 700 | 800 | 1400 | 4.86 | 28 | 0x33 | 0xC4 |
| 400 | 800 | 800 | 1600 | 6.02 | 32 | 0x44 | 0xC4 |
| 400 | 900 | 800 | 1800 | 7.04 | 36 | 0x55 | 0xC4 |
| 400 | 1000 | 800 | 2000 | 7.96 | 40 | 0x66 | 0xC4 |

| V _{SW-DC} (mV) | V _{SW-PE} (mV) | V _{DPP-DC} (mV) | V _{DPP-PE} (mV) | PE (dB) | I _{TOT} (mA) | OUT_A/OUT_B OLEV 0 | OUT_A/OUT_B OLEV 1 |
|-------------------------|-------------------------|--------------------------|--------------------------|---------|-----------------------|--------------------|--------------------|
| 450 | 450 | 900 | 900 | 0.00 | 18 | 0x00 | 0xC5 |
| 450 | 550 | 900 | 1100 | 1.74 | 22 | 0x11 | 0xC5 |
| 450 | 650 | 900 | 1300 | 3.19 | 26 | 0x22 | 0xC5 |
| 450 | 750 | 900 | 1500 | 4.44 | 30 | 0x33 | 0xC5 |
| 450 | 850 | 900 | 1700 | 5.52 | 34 | 0x44 | 0xC5 |
| 450 | 950 | 900 | 1900 | 6.49 | 38 | 0x55 | 0xC5 |
| 450 | 1050 | 900 | 2100 | 7.36 | 42 | 0x66 | 0xC5 |
| 500 | 500 | 1000 | 1000 | 0.00 | 20 | 0x00 | 0xD5 |
| 500 | 600 | 1000 | 1200 | 1.58 | 24 | 0x11 | 0xD5 |
| 500 | 700 | 1000 | 1400 | 2.92 | 28 | 0x22 | 0xD5 |
| 500 | 800 | 1000 | 1600 | 4.08 | 32 | 0x33 | 0xD5 |
| 500 | 900 | 1000 | 1800 | 5.11 | 36 | 0x44 | 0xD5 |
| 500 | 1000 | 1000 | 2000 | 6.02 | 40 | 0x55 | 0xD5 |
| 500 | 1100 | 1000 | 2200 | 6.85 | 44 | 0x66 | 0xD5 |
| 550 | 550 | 1100 | 1100 | 0.00 | 22 | 0x00 | 0xD6 |
| 550 | 650 | 1100 | 1300 | 1.45 | 26 | 0x11 | 0xD6 |
| 550 | 750 | 1100 | 1500 | 2.69 | 30 | 0x22 | 0xD6 |
| 550 | 850 | 1100 | 1700 | 3.78 | 34 | 0x33 | 0xD6 |
| 550 | 950 | 1100 | 1900 | 4.75 | 38 | 0x44 | 0xD6 |
| 550 | 1050 | 1100 | 2100 | 5.62 | 42 | 0x55 | 0xD6 |
| 550 | 1150 | 1100 | 2300 | 6.41 | 46 | 0x66 | 0xD6 |
| 600 | 600 | 1200 | 1200 | 0.00 | 24 | 0x00 | 0xE6 |
| 600 | 700 | 1200 | 1400 | 1.34 | 28 | 0x11 | 0xE6 |
| 600 | 800 | 1200 | 1600 | 2.50 | 32 | 0x22 | 0xE6 |
| 600 | 900 | 1200 | 1800 | 3.52 | 36 | 0x33 | 0xE6 |
| 600 | 1000 | 1200 | 2000 | 4.44 | 40 | 0x44 | 0xE6 |
| 600 | 1100 | 1200 | 2200 | 5.26 | 44 | 0x55 | 0xE6 |
| 600 | 1200 | 1200 | 2400 | 6.02 | 48 | 0x66 | 0xE6 |
| 650 | 650 | 1300 | 1300 | 0.00 | 26 | 0x01 | 0xE6 |
| 650 | 750 | 1300 | 1500 | 1.24 | 30 | 0x12 | 0xE6 |
| 650 | 850 | 1300 | 1700 | 2.33 | 34 | 0x23 | 0xE6 |
| 650 | 950 | 1300 | 1900 | 3.30 | 38 | 0x34 | 0xE6 |
| 650 | 1050 | 1300 | 2100 | 4.17 | 42 | 0x45 | 0xE6 |
| 650 | 1150 | 1300 | 2300 | 4.96 | 46 | 0x56 | 0xE6 |
| 700 | 700 | 1400 | 1400 | 0.00 | 28 | 0x02 | 0xE6 |
| 700 | 800 | 1400 | 1600 | 1.16 | 32 | 0x13 | 0xE6 |
| 700 | 900 | 1400 | 1800 | 2.18 | 36 | 0x24 | 0xE6 |
| 700 | 1000 | 1400 | 2000 | 3.10 | 40 | 0x35 | 0xE6 |
| 700 | 1100 | 1400 | 2300 | 3.93 | 44 | 0x46 | 0xE6 |
| 750 | 750 | 1500 | 1500 | 0.00 | 30 | 0x03 | 0xE6 |
| 750 | 850 | 1500 | 1700 | 1.09 | 34 | 0x14 | 0xE6 |
| 750 | 950 | 1500 | 1900 | 2.05 | 38 | 0x25 | 0xE6 |
| 750 | 1050 | 1500 | 2100 | 2.92 | 42 | 0x36 | 0xE6 |
| 800 | 800 | 1600 | 1600 | 0.00 | 32 | 0x04 | 0xE6 |
| 800 | 900 | 1600 | 1800 | 1.02 | 36 | 0x15 | 0xE6 |
| 800 | 1000 | 1600 | 2000 | 1.94 | 40 | 0x26 | 0xE6 |
| 850 | 850 | 1700 | 1700 | 0.00 | 34 | 0x05 | 0xE6 |
| 850 | 950 | 1700 | 1900 | 0.97 | 38 | 0x16 | 0xE6 |
| 900 | 900 | 1800 | 1800 | 0.00 | 36 | 0x06 | 0xE6 |

SELECTIVE SQUELCH AND DISABLE

Each transmitter is equipped with output disable and output squelch controls. Disable is a full power-down state: the transmitter current is reduced to zero, and the output pins pull up to V_{TTO} , but there is a delay of approximately 1 μ s associated with re-enabling the transmitter. The output disable control is accessed through the EN bit (Bit 4) of the OUT_A/OUT_B configuration registers through the I²C control interface.

Squelch is not a full power-down state but a state in which only the output current is reduced to zero and the output pins pull up to V_{TTO} , and there is a much smaller delay to bring back the output current. The output squelch and the output disable control can both be accessed through the OUT_A/OUT_B squelch control registers, with the top nibble representing the squelch control for one entire output port, and the bottom nibble representing the output disable for one entire output port. The ports are disabled or squelched by writing 0s to the corresponding nibbles. The ports are enabled by writing all 1s, which is the

default setting. For example, to squelch Port A, Register 0xC3 must be set to 0x0F. The entire nibble must be written to all 0s for this functionality.

Table 18. Squelch and Disable Control Registers

| Name | Address | Data | | Default |
|---------------------------------------|---------------|--------------|--------------|---------|
| OUT_A/ OUT_B squelch control | 0xC3, 0xE3 | SQUELCH[3:0] | DISABLE[3:0] | 0xFF |

Table 19. Squelch and Disable Functionality

| SQUELCH[3:0] | DISABLE[3:0] | Output State |
|-------------------|--------------|-------------------|
| 1111 | 1111 | Enabled (default) |
| xxxx ¹ | 0000 | Disabled |
| 0000 | 1111 | Squelched |

¹ xxxx = don't care

I²C CONTROL INTERFACE

SERIAL INTERFACE GENERAL FUNCTIONALITY

The ADN8102 register set is controlled through a 2-wire I²C interface. The ADN8102 acts only as an I²C slave device. Therefore, the I²C bus in the system needs to include an I²C master to configure the ADN8102 and other I²C devices that may be on the bus. Data transfers are controlled using the two I²C wires: the SCL input clock pin and the SDA bidirectional data pin.

The ADN8102 I²C interface can be run in the standard (100 kHz) and fast (400 kHz) modes. The SDA line only changes value when the SCL pin is low with two exceptions. To indicate the beginning or continuation of a transfer, the SDA pin is driven low while the SCL pin is high, and to indicate the end of a transfer, the SDA line is driven high while the SCL line is high. Therefore, it is important to control the SCL clock to toggle only when the SDA line is stable, unless indicating a start, repeated start, or stop condition.

I²C INTERFACE DATA TRANSFERS—DATA WRITE

To write data to the ADN8102 register set, a microcontroller, or any other I²C master, needs to send the appropriate control signals to the ADN8102 slave device. The steps that need to be completed are listed as follows, where the signals are controlled by the I²C master, unless otherwise specified. A diagram of the procedure can be seen in Figure 42.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the ADN8102 part address (seven bits) whose upper five bits are the static value 10010b and whose lower two bits are controlled by the ADDR[1:0] input pins. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the ADN8102 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the ADN8102 to acknowledge the request.

7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the ADN8102 to acknowledge the request.
- 9a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.
- 9b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 in this procedure to perform another write.
- 9c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the read procedure (in the I²C Interface Data Transfers—Data Read section) to perform a read from another address.
- 9d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of the read procedure (in the I²C Interface Data Transfers—Data Read section) to perform a read from the same address set in Step 5.

Figure 42 shows the ADN8102 write process. The SCL signal is shown along with a general write operation and a specific example. In the example, Data 0x92 is written to Address 0x6D of an ADN8102 part with a part address of 0x4B. The part address is seven bits wide. The upper five bits of the ADN8102 are internally set to 10010b. The lower two bits are controlled by the ADDR[1:0] pins. In this example, the bits controlled by the ADDR[1:0] pins are set to 11b. In Figure 42, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the ADN8102 slave. As for the SDA line, the data in the shaded polygons is driven by the ADN8102, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case shown is that of Step 9a.

Note that the SDA line only changes when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, Step 1 and Step 9 in this case.

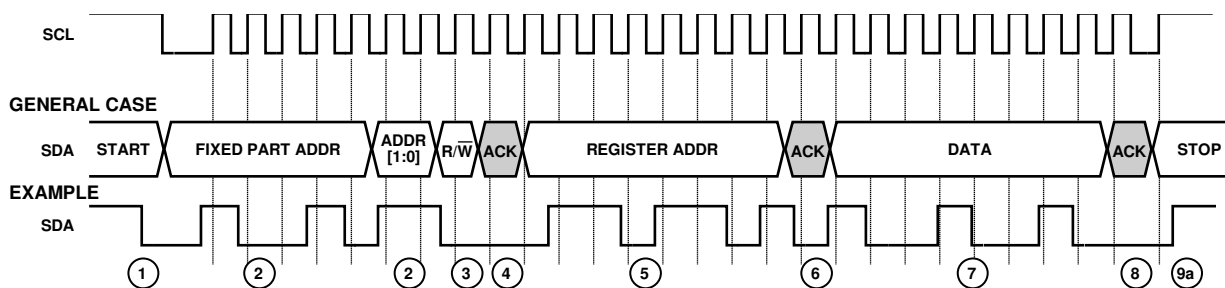


Figure 42. I²C Write Diagram

ADN8102

I²C INTERFACE DATA TRANSFERS—DATA READ

To read data from the ADN8102 register set, a microcontroller, or any other I²C master, needs to send the appropriate control signals to the ADN8102 slave device. The steps that need to be completed are listed as follows, where the signals are controlled by the I²C master, unless otherwise specified. A diagram of the procedure can be seen in Figure 43.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the ADN8102 part address (seven bits) whose upper five bits are the static value 10010b and whose lower two bits are controlled by the input pins ADDR[1:0]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the ADN8102 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first. The register address is kept in memory in the ADN8102 until the part is reset or the register address is written over with the same procedure (Step 1 to Step 6).
6. Wait for the ADN8102 to acknowledge the request.
7. Send a repeated start condition (while holding the SCL line high, pull the SDA line low).
8. Send the ADN8102 part address (seven bits) whose upper five bits are the static value 10010b and whose lower two bits are controlled by the input pins ADDR[1:0]. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the ADN8102 to acknowledge the request.
11. The ADN8102 then serially transfers the data (eight bits) held in the register indicated by the address set in Step 5.
12. Acknowledge the data.

- 13a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.
- 13b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the write procedure (in the I²C Interface Data Transfers—Data Write section) to perform a write.
- 13c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
- 13d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

Figure 43 shows the ADN8102 read process. The SCL signal is shown along with a general read operation and a specific example. In the example, Data 0x49 is read from Address 0x6D of an ADN8102 part with a part address of 0x4B. The part address is seven bits wide. The upper five bits of the ADN8102 are internally set to 10010b. The lower two bits are controlled by the ADDR[1:0] pins. In this example, the bits controlled by the ADDR[1:0] pins are set to 11b. In Figure 43, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the ADN8102 slave. As for the SDA line, the data in the shaded polygons is driven by the ADN8102, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case shown is that of Step 13a.

Note that the SDA line changes only when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, as in Step 1, Step 7, and Step 13. In Figure 43, A is the same as ACK in Figure 42. Equally, Sr represents a repeated start where the SDA line is brought high before SCL is raised. SDA is then dropped while SCL is still high.

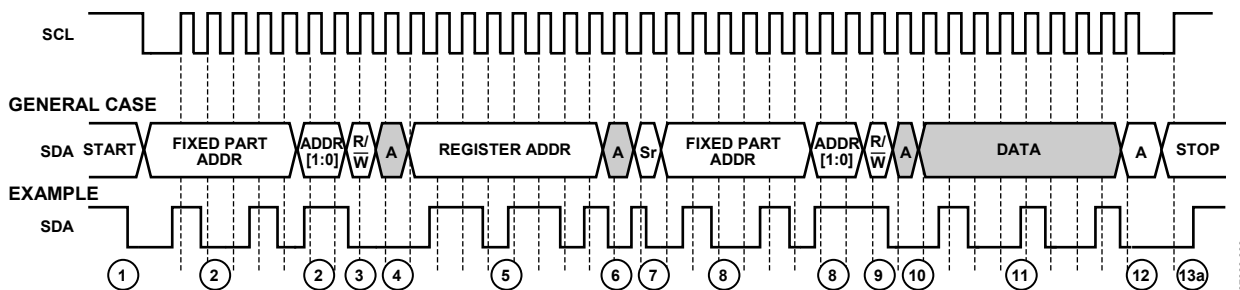


Figure 43. I²C Read Diagram

APPLICATIONS INFORMATION

OUTPUT COMPLIANCE

In low voltage applications, users must pay careful attention to both the differential and common-mode signal levels. The choice of output voltage swing, preemphasis setting, supply voltages (V_{CC} and V_{TTO}), and output coupling (ac or dc) affect peak and settled single-ended voltage swings and the common-mode shift measured across the output termination resistors. These choices also affect output current and, consequently, power consumption. For ac-coupled applications, certain combinations of supply voltage, output voltage swing, and preemphasis settings may violate the single-ended absolute output low voltage, as specified in Table 1. Under these conditions, the performance is degraded; therefore, these settings are not recommended. Table 21 includes annotations that identify these settings. In dc-coupled applications, the far-end termination voltage should be equal to V_{TTO} to allow the full list of output swing and preemphasis settings listed in Table 17.

TxHeadroom

The TxHeadroom register (Register 0x23) allows configuration of the individual transmitters for extra headroom at the output for high current applications. The bits in this register are active high (default) and are one per output (see Table 22). Setting a bit high puts the respective transmitter in a configuration for extra headroom, and setting a bit low does not provide extra headroom. The TxHeadroom bits should only be set high when required for a given output swing as listed in Table 21. Note that TxHeadroom is not available for $V_{CC} < 2.5$ V.

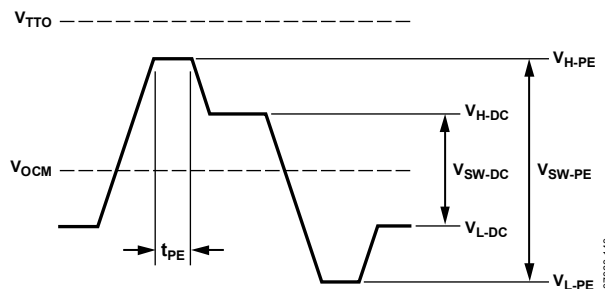


Figure 44. Simplified Output Voltage Levels Diagram

Table 20. Symbol Definitions

| Symbol | Formula | Definition |
|------------------------------|--|--|
| I_{DC} | Programmable | Output current that sets output level |
| I_{PE} | Programmable | Output current for PE delayed tap |
| I_{TTO} | $I_{DC} + I_{PE}$ | Total transmitter output current |
| V_{DPP-DC} | $25 \Omega \times I_{DC} \times 2$ | Peak-to-peak differential voltage swing of nonpreemphasized waveform |
| V_{DPP-PE} | $25 \Omega \times I_{TTO} \times 2$ | Peak-to-peak differential voltage swing of preemphasized waveform |
| V_{SW-DC} | $V_{DPP-DC}/2 = V_{H-DC} - V_{L-DC}$ | DC single-ended voltage swing |
| V_{SW-PE} | $V_{DPP-PE}/2 = V_{H-PE} - V_{L-PE}$ | Preemphasized single-ended voltage swing |
| $\Delta V_{OCM_DC-COUPLED}$ | $25 \Omega \times I_{TTO}/2$ | Output common-mode shift, dc-coupled outputs |
| $\Delta V_{OCM_AC-COUPLED}$ | $50 \Omega \times I_{TTO}/2$ | Output common-mode shift, ac-coupled outputs |
| V_{OCM} | $V_{TTO} - \Delta V_{OCM} = (V_{H-DC} + V_{L-DC})/2$ | Output common-mode voltage |
| V_{H-DC} | $V_{TTO} - \Delta V_{OCM} + V_{DPP-DC}/2$ | DC single-ended output high voltage |
| V_{L-DC} | $V_{TTO} - \Delta V_{OCM} - V_{DPP-DC}/2$ | DC single-ended output low voltage |
| V_{H-PE} | $V_{TTO} - \Delta V_{OCM} + V_{DPP-PE}/2$ | Maximum single-ended output voltage |
| V_{L-PE} | $V_{TTO} - \Delta V_{OCM} - V_{DPP-PE}/2$ | Minimum single-ended output voltage |

ADN8102

Table 21. Output Compliance for AC-Coupled Outputs

| V _{SW-DC} (mV) | V _{SW-PE} (mV) | PE (dB) | I _{TOT} (mA) | OLEV 0 | OLEV1 | V _{CC} =V _{TTO} =3.3V | V _{CC} =V _{TTO} =2.5V | V _{CC} =V _{TTO} =1.8V |
|-------------------------|-------------------------|---------|-----------------------|--------|-------|---|---|---|
| 200 | 200 | 0.00 | 8 | 0x00 | 0xA2 | Supported | Supported | Supported |
| 200 | 300 | 3.52 | 12 | 0x11 | 0xA2 | Supported | Supported | Supported |
| 200 | 400 | 6.02 | 16 | 0x22 | 0xA2 | Supported | Supported | Supported |
| 200 | 500 | 7.96 | 20 | 0x33 | 0xA2 | Supported | Supported | Supported |
| 200 | 600 | 9.54 | 24 | 0x44 | 0xA2 | Supported | Supported | Supported |
| 200 | 700 | 10.88 | 28 | 0x55 | 0xA2 | Supported | Supported | Not Supported |
| 200 | 800 | 12.04 | 32 | 0x66 | 0xA2 | Use TX_HDRM = 1 | Use TX_HDRM = 1 | Not Supported |
| 300 | 300 | 0.00 | 12 | 0x00 | 0xB3 | Supported | Supported | Supported |
| 300 | 400 | 2.50 | 16 | 0x11 | 0xB3 | Supported | Supported | Supported |
| 300 | 500 | 4.44 | 20 | 0x22 | 0xB3 | Supported | Supported | Supported |
| 300 | 600 | 6.02 | 24 | 0x33 | 0xB3 | Supported | Supported | Supported |
| 300 | 700 | 7.36 | 28 | 0x44 | 0xB3 | Supported | Supported | Supported |
| 300 | 800 | 8.52 | 32 | 0x55 | 0xB3 | Use TX_HDRM = 1 | Use TX_HDRM = 1 | Not Supported |
| 300 | 900 | 9.54 | 36 | 0x66 | 0xB3 | Not Supported | Not Supported | Not Supported |
| 400 | 400 | 0.00 | 16 | 0x00 | 0xC4 | Supported | Supported | Supported |
| 400 | 500 | 1.94 | 20 | 0x11 | 0xC4 | Supported | Supported | Supported |
| 400 | 600 | 3.52 | 24 | 0x22 | 0xC4 | Supported | Supported | Supported |
| 400 | 700 | 4.86 | 28 | 0x33 | 0xC4 | Supported | Supported | Supported |
| 400 | 800 | 6.02 | 32 | 0x44 | 0xC4 | Use TX_HDRM = 1 | Use TX_HDRM = 1 | Not Supported |
| 400 | 900 | 7.04 | 36 | 0x55 | 0xC4 | Not Supported | Not Supported | Not Supported |
| 400 | 1000 | 7.96 | 40 | 0x66 | 0xC4 | Not Supported | Not Supported | Not Supported |
| 600 | 600 | 0.00 | 24 | 0x00 | 0xE6 | Supported | Supported | Supported |
| 600 | 700 | 1.34 | 28 | 0x11 | 0xE6 | Supported | Supported | Supported |
| 600 | 800 | 2.50 | 32 | 0x22 | 0xE6 | Use TX_HDRM = 1 | Use TX_HDRM = 1 | Not Supported |
| 600 | 900 | 3.52 | 36 | 0x33 | 0xE6 | Not Supported | Not Supported | Not Supported |
| 600 | 1000 | 4.44 | 40 | 0x44 | 0xE6 | Not Supported | Not Supported | Not Supported |
| 600 | 1100 | 5.26 | 44 | 0x55 | 0xE6 | Not Supported | Not Supported | Not Supported |
| 600 | 1200 | 6.02 | 48 | 0x66 | 0xE6 | Not Supported | Not Supported | Not Supported |

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

The high speed differential inputs and outputs should be routed with $100\ \Omega$ controlled impedance, differential transmission lines. The transmission lines, either microstrip or stripline, should be referenced to a solid low impedance reference plane. An example of a PCB cross-section is shown in Figure 45. The trace width (W), differential spacing (S), height above reference plane (H), and dielectric constant of the PCB material determine the characteristic impedance. Adjacent channels should be kept apart by a distance greater than $3W$ to minimize crosstalk.

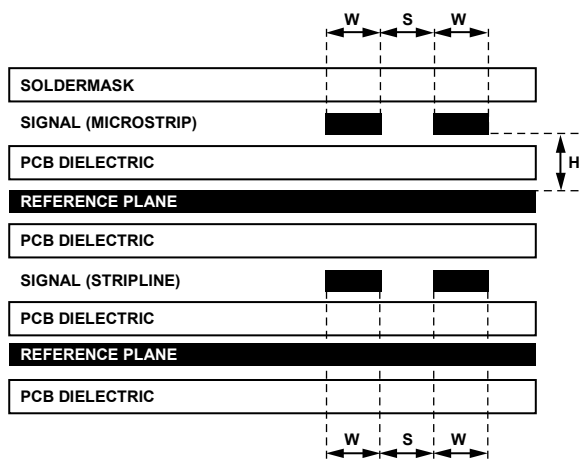


Figure 45. Example of a PCB Cross-Section

Power Supply Connections and Ground Planes

Use of one low impedance ground plane is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance. The exposed pad should be connected to the VEE plane using plugged vias so that solder does not leak through the vias during reflow.

Use of a $10\ \mu\text{F}$ electrolytic capacitor between VCC and VEE is recommended at the location where the $3.3\ \text{V}$ supply enters the printed circuit board (PCB). It is recommended that $0.1\ \mu\text{F}$ and $1\ \text{nF}$ ceramic chip capacitors be placed in parallel at each supply pin for high frequency, power supply decoupling. When using $0.1\ \mu\text{F}$ and $1\ \text{nF}$ ceramic chip capacitors, they should be placed between the IC power supply pins (VCC, VTTI, and VTTO) and VEE, as close as possible to the supply pins.

By using adjacent power supply and GND planes, excellent high frequency decoupling can be realized by using close spacing between the planes. This capacitance is given by

$$C_{\text{PLANE}} = 0.88\epsilon_r \times A/d \text{ (pF)}$$

where:

ϵ_r is the dielectric constant of the PCB material.

A is the area of the overlap of power and GND planes (cm^2).

d is the separation between planes (mm).

For FR4, $\epsilon_r = 4.4$ and $0.25\ \text{mm}$ spacing, $C \approx 15\ \text{pF}/\text{cm}^2$.

Supply Sequencing

Ideally, all power supplies should be brought up to the appropriate levels simultaneously (power supply requirements are set by the supply limits in Table 1 and the absolute maximum ratings listed in Table 3). In the event that the power supplies to the ADN8102 are brought up separately, the supply power-up sequence is as follows: DV_{CC} is powered first, followed by V_{CC} , and lastly V_{TTI} and V_{TTO} . The power-down sequence is reversed, with V_{TTI} and V_{TTO} being powered off first.

V_{TTI} and V_{TTO} contain ESD protection diodes to the V_{CC} power domain (see Figure 39 and Figure 41). To avoid a sustained high current condition in these devices ($I_{\text{SUSTAINED}} < 64\ \text{mA}$), the V_{TTI} and V_{TTO} supplies should be powered on after V_{CC} and should be powered off before V_{CC} .

If the system power supplies have a high impedance in the powered off state, then supply sequencing is not required provided the following limits are observed:

- Peak current from V_{TTI} or V_{TTO} to $V_{\text{CC}} < 200\ \text{mA}$.
- Sustained current from V_{TTI} or V_{TTO} to $V_{\text{CC}} < 64\ \text{mA}$.

Thermal Paddle Design

The LFCSP is designed with an exposed thermal paddle to conduct heat away from the package and into the PCB. By incorporating thermal vias into the PCB thermal paddle, heat is dissipated more effectively into the inner metal layers of the PCB. To ensure device performance at elevated temperatures, it is important to have a sufficient number of thermal vias incorporated into the design. An insufficient number of thermal vias results in a θ_{JA} value larger than specified in Table 1. Additional PCB footprint and assembly guidelines are described in the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

It is recommended that a via array of 4×4 or 5×5 with a diameter of $0.3\ \text{mm}$ to $0.33\ \text{mm}$ be used to set a pitch between $1.0\ \text{mm}$ and $1.2\ \text{mm}$. A representative of these arrays is shown in Figure 46.

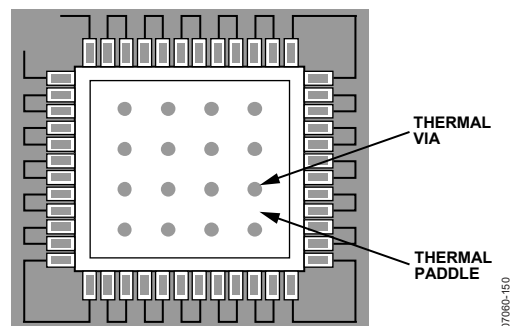


Figure 46. PCB Thermal Paddle and Via

Stencil Design for the Thermal Paddle

To effectively remove heat from the package and to enhance electrical performance, the thermal paddle must be soldered (bonded) to the PCB thermal paddle, preferably with minimum voids. However, eliminating voids may not be possible because of the presence of thermal vias and the large size of the thermal paddle for larger size packages. Also, outgassing during the reflow process may cause defects (splatter, solder balling) if the solder paste coverage is too big. It is recommended that smaller multiple openings in the stencil be used instead of one big opening for printing solder paste on the thermal paddle region. This typically results in 50% to 80% solder paste coverage. Figure 47 shows how to achieve these levels of coverage.

Voids within solder joints under the exposed paddle can have an adverse effect on high speed and RF applications, as well as on thermal performance. Because the LFCSP package incorporates a large center paddle, controlling solder voiding within this region can be difficult. Voids within this ground plane can increase the current path of the circuit. The maximum size for a void should be less than via pitch within the plane. This assures that any one via is not rendered ineffectual when any void increases the current path beyond the distance to the next available via.

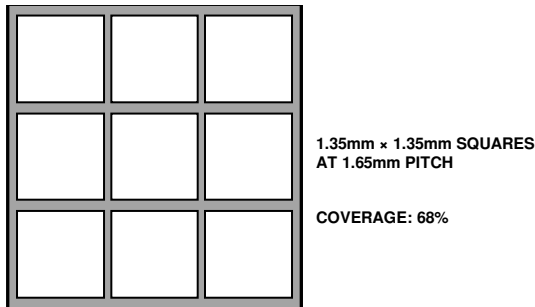


Figure 47. Typical Thermal Paddle Stencil Design

Large voids in the thermal paddle area should be avoided. To control voids in the thermal paddle area, solder masking may be required for thermal vias to prevent solder wicking inside the via during reflow, thus displacing the solder away from the interface between the package thermal paddle and thermal paddle land on the PCB. There are several methods employed for this purpose, such as via tenting (top or bottom side), using dry film solder mask; via plugging with liquid photo-imagible (LPI) solder mask from the bottom side; or via encroaching. These options are depicted in Figure 48. In case of via tenting, the solder mask diameter should be 100 microns larger than the via diameter.

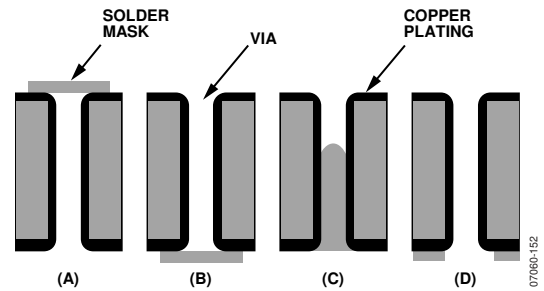


Figure 48. Solder Mask Options for Thermal Vias: (a) Via Tenting from the Top; (b) Via Tenting from the Bottom; (c) Via Plugging, Bottom; and (d) Via Encroaching, Bottom

A stencil thickness of 0.125 mm is recommended for 0.4 mm and 0.5 mm pitch parts. The stencil thickness can be increased to 0.15 mm to 0.2 mm for coarser pitch parts. A laser-cut, stainless steel stencil is recommended with electropolished trapezoidal walls to improve the paste release. Because not enough space is available underneath the part after reflow, it is recommended that no clean Type 3 paste be used for mounting the LFCSP. Inert atmosphere is also recommended during reflow.

REGISTER MAP

Table 22. I²C Register Definitions

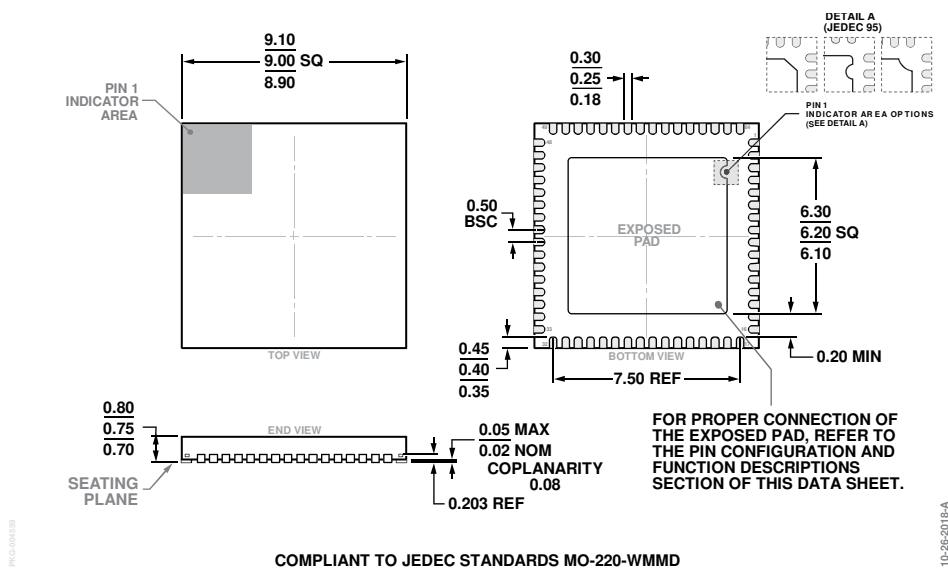
| Name | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default |
|------------------------------|---------|---------------|---------------|---------------|---------------|------------------|------------------|------------------|------------------|---------|
| Reset | 0x00 | | | | | | | | RESET | |
| Loopback control | 0x02 | | | | | | | LB[1] | LB[0] | 0x00 |
| Control interface mode | 0x0F | | | | | | | MODE[1] | MODE[0] | 0x00 |
| TxHeadroom | 0x23 | TxH_B3 | TxH_B2 | TxH_B1 | TxH_B0 | TxH_A3 | TxH_A2 | TxH_A1 | TxH_A0 | 0x00 |
| IN_A configuration | 0x80 | | PNSWAP | EQBY | EN | | EQ[2] | EQ[1] | EQ[0] | 0x30 |
| IN_A LOS threshold | 0x81 | | THRESH[6] | THRESH[5] | THRESH[4] | THRESH[3] | THRESH[2] | THRESH[1] | THRESH[0] | 0x04 |
| IN_A LOS hysteresis | 0x82 | | HYST[6] | HYST[5] | HYST[4] | HYST[3] | HYST[2] | HYST[1] | HYST[0] | 0x12 |
| IN_A LOS status ¹ | 0x1F | STICKY LOS[3] | STICKY LOS[2] | STICKY LOS[1] | STICKY LOS[0] | REAL-TIME LOS[3] | REAL-TIME LOS[2] | REAL-TIME LOS[1] | REAL-TIME LOS[0] | |
| IN_A EQ1 control | 0x83 | | EQ CTL SRC | EQ1[5] | EQ1[4] | EQ1[3] | EQ1[2] | EQ1[1] | EQ1[0] | 0x00 |
| IN_A EQ2 control | 0x84 | | | EQ2[5] | EQ2[4] | EQ2[3] | EQ2[2] | EQ2[1] | EQ2[0] | 0x00 |
| IN_A0 FR4 control | 0x85 | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |
| IN_A1 FR4 control | 0x8D | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |
| IN_A2 FR4 control | 0x95 | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |
| IN_A3 FR4 control | 0x9D | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |
| IN_B configuration | 0xA0 | | PNSWAP | EQBY | EN | | EQ[2] | EQ[1] | EQ[0] | 0x30 |
| IN_B LOS threshold | 0xA1 | | THRESH[6] | THRESH[5] | THRESH[4] | THRESH[3] | THRESH[2] | THRESH[1] | THRESH[0] | 0x04 |
| IN_B LOS hysteresis | 0xA2 | | HYST[6] | HYST[5] | HYST[4] | HYST[3] | HYST[2] | HYST[1] | HYST[0] | 0x12 |
| IN_B LOS Status ¹ | 0x3F | STICKY LOS[3] | STICKY LOS[2] | STICKY LOS[1] | STICKY LOS[0] | REAL-TIME LOS[3] | REAL-TIME LOS[2] | REAL-TIME LOS[1] | REAL-TIME LOS[0] | |
| IN_B EQ1 control | 0xA3 | | EQ CTL SRC | EQ1[5] | EQ1[4] | EQ1[3] | EQ1[2] | EQ1[1] | EQ1[0] | 0x00 |
| IN_B EQ2 control | 0xA4 | | | EQ2[5] | EQ2[4] | EQ2[3] | EQ2[2] | EQ2[1] | EQ2[0] | 0x00 |
| IN_B3 FR4 control | 0xA5 | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |
| IN_B2 FR4 Control | 0xAD | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |
| IN_B1 FR4 control | 0xB5 | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |
| IN_B0 FR4 control | 0xBD | | | | | | | LUT SELECT | LUT FR4/CX4 | 0x00 |

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| Name | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default |
|------------------------------|---------|--------------|-----------------|-------|-----------|--------------|-------|-------|-------|---------|
| OUT_A configuration | 0xC0 | | | EN | DATA RATE | | PE[2] | PE[1] | PE[0] | 0x20 |
| OUT_A Output Level Control 1 | 0xC1 | PE CTL SRC | OUTA_OLEV1[6:0] | | | | | | | 0x40 |
| OUT_A Output Level Control 0 | 0xC2 | | OUTA_OLEV0[6:0] | | | | | | | 0x40 |
| OUT_A squelch control | 0xC3 | SQUELCH[3:0] | | | | DISABLE[3:0] | | | | 0xFF |
| OUT_B configuration | 0xE0 | | | EN | DATA RATE | | PE[2] | PE[1] | PE[0] | 0x20 |
| OUT_B Output Level Control 1 | 0xE1 | PE CTL SRC | OUTB_OLEV1[6:0] | | | | | | | 0x40 |
| OUT_B Output Level Control 0 | 0xE2 | | OUTB_OLEV0[6:0] | | | | | | | 0x40 |
| OUT_B squelch control | 0xE3 | SQUELCH[3:0] | | | | DISABLE[3:0] | | | | 0xFF |

¹ Read-only register.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WMMD

Figure 49. 64-Lead Lead Frame Chip Scale Package [LFCSP]
 9 mm × 9 mm Body and 0.75 mm Package Height
 (CP-64-17)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADN8102ACPZ | -40°C to +85°C | 64-Lead Lead Frame Chip Scale Package [LFCSP] | CP-64-17 |
| ADN8102ACPZ-R7 | -40°C to +85°C | 64-Lead Lead Frame Chip Scale Package [LFCSP] | CP-64-17 |
| ADN8102-EVALZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

ADN8102

NOTES

NOTES

ADN8102

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).