IS61WV51232ALL/ALS
IS61WV51232BLL/BLS
IS64WV51232BLL/BLS

512K x 32 HIGH-SPEED ASYNCHRONOUS CMOS STATIC RAM WITH 3.3V SUPPLY

JUNE 2016

FEATURES

- High-speed access times:
  - 8, 10, 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single power supply
  - V_{DD} 1.65V to 2.2V (IS61WV51232Axx)
  - speed = 20ns for V_{DD} 1.65V to 2.2V
  - V_{DD} 2.4V to 3.6V (IS61/64WV51232Bxx)
  - speed = 10ns for V_{DD} 2.4V to 3.6V
  - speed = 8ns for V_{DD} 3.3V $\pm$ 5%
- Packages available:
  - 90-ball miniBGA (8mm x 13mm)
- Industrial and Automotive Temperature Support
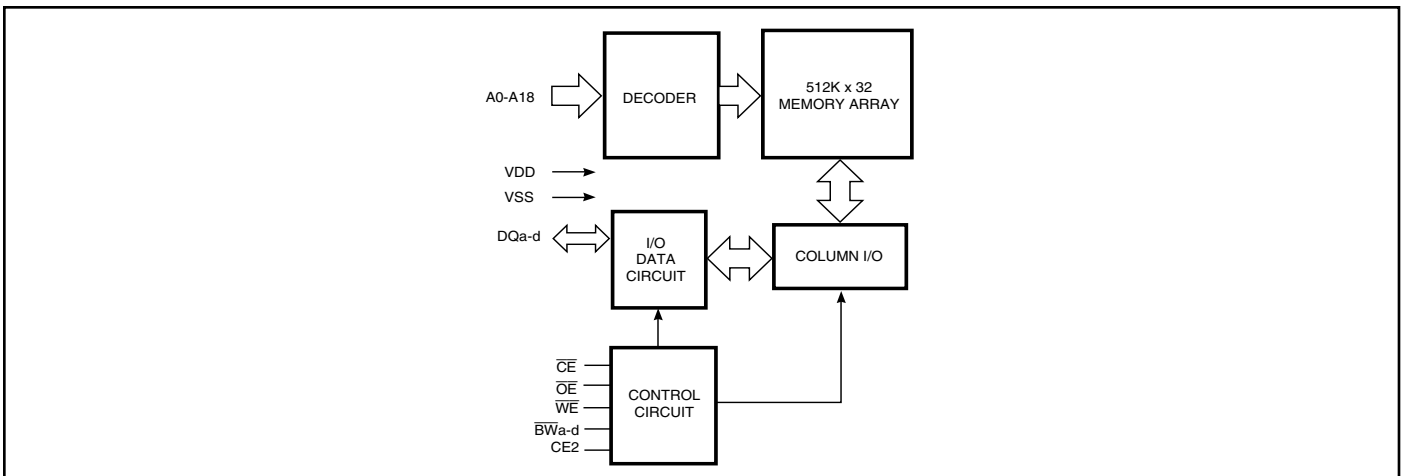- Lead-free available

DESCRIPTION

The *ISSI* IS61WV51232Axx/Bxx and IS64WV51232Bxx are high-speed, 16M-bit static RAMs organized as 512K words by 32 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The device is packaged in the JEDEC standard 90-ball BGA (8mm x 13mm).
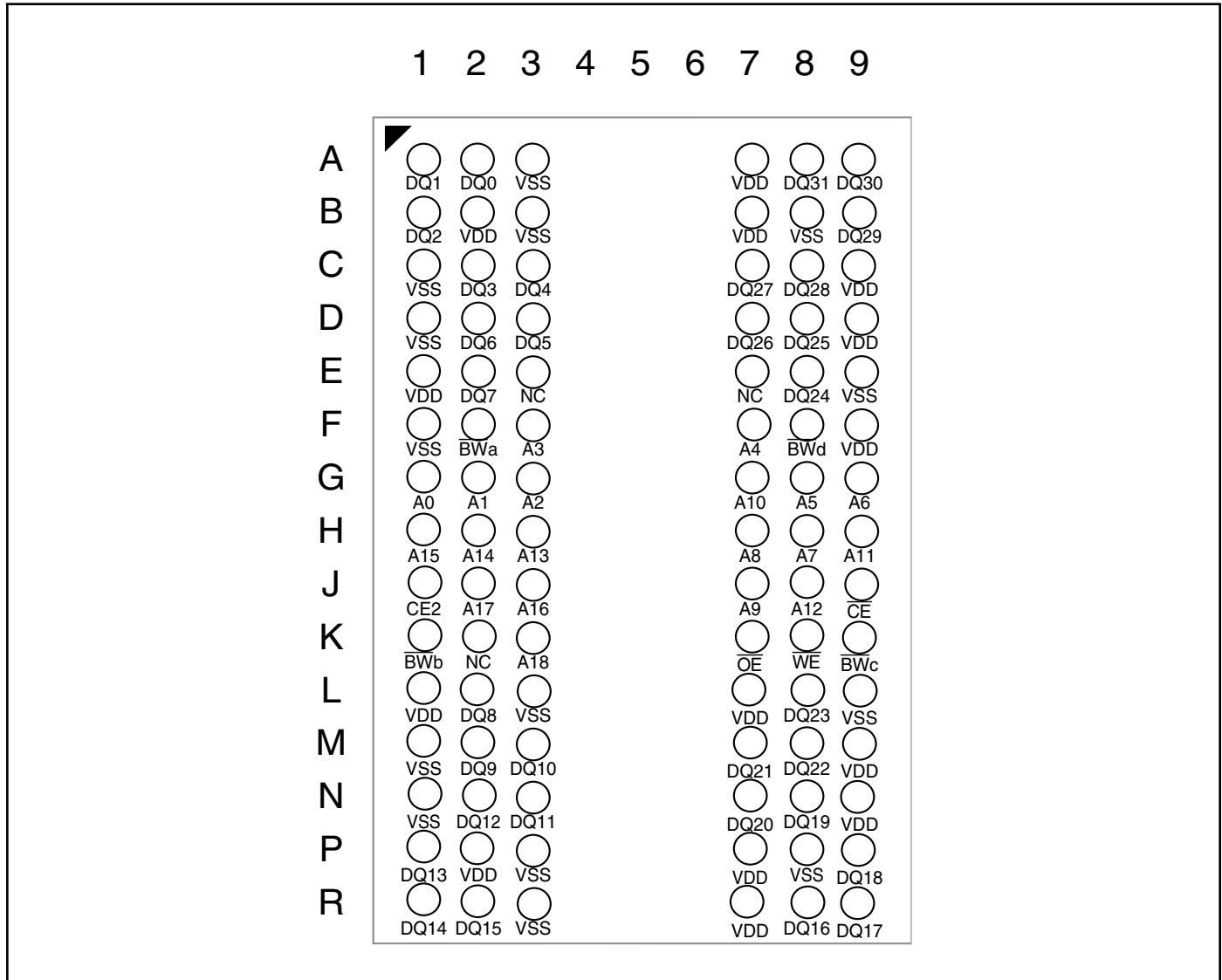
FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

PACKAGE CODE: B 90 BALL FBGA (Top View) (8.00 mm x 13.00 mm Body, 0.8 mm Ball Pitch)

	1	2	3	4	5	6	7	8	9
A	DQ1	DQ0	VSS				VDD	DQ31	DQ30
B	DQ2	VDD	VSS				VDD	VSS	DQ29
C	VSS	DQ3	DQ4				DQ27	DQ28	VDD
D	VSS	DQ6	DQ5				DQ26	DQ25	VDD
E	VDD	DQ7	NC				NC	DQ24	VSS
F	VSS	BWa	A3				A4	BWd	VDD
G	A0	A1	A2				A10	A5	A6
H	A15	A14	A13				A8	A7	A11
J	CE2	A17	A16				A9	A12	CE
K	BWb	NC	A18				OE	WE	BWc
L	VDD	DQ8	VSS				VDD	DQ23	VSS
M	VSS	DQ9	DQ10				DQ21	DQ22	VDD
N	VSS	DQ12	DQ11				DQ20	DQ19	VDD
P	DQ13	VDD	VSS				VDD	VSS	DQ18
R	DQ14	DQ15	VSS				VDD	DQ16	DQ17

PIN DESCRIPTIONS

A0-A18	Address Inputs
DQx	Data I/O
$\overline{CE}$, CE2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{BW}$x (x=a-d)	Byte Write Control
V_{DD}	Power
Vss	Ground
NC	No Connection

TRUTH TABLE

$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	DQ_{0-7}	DQ_{8-15}	DQ_{16-23}	DQ_{24-31}	Mode	Power
H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
X	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
L	H	L	H	L	L	L	L	Data Out	Data Out	Data Out	Data Out	Read All Bits	(I_{CC})
L	H	L	H	L	H	H	H	Data Out	High-Z	High-Z	High-Z	Read Byte a Bits Only	(I_{CC})
L	H	L	H	H	L	H	H	High-Z	Data Out	High-Z	High-Z	Read Byte b Bits Only	(I_{CC})
L	H	L	H	H	H	L	H	High-Z	High-Z	Data Out	High-Z	Read Byte c Bits Only	(I_{CC})
L	H	L	H	H	H	H	L	High-Z	High-Z	High-Z	Data Out	Read Byte d Bits Only	(I_{CC})
L	H	X	L	L	L	L	L	Data In	Data In	Data In	Data In	Write All Bits	(I_{CC})
L	H	X	L	L	H	H	H	Data In	High-Z	High-Z	High-Z	Write Byte a Bits Only	(I_{CC})
L	H	X	L	H	L	H	H	High-Z	Data In	High-Z	High-Z	Write Byte b Bits Only	(I_{CC})
L	H	X	L	H	H	L	H	High-Z	High-Z	Data In	High-Z	Write Byte c Bits Only	(I_{CC})
L	H	X	L	H	H	H	L	High-Z	High-Z	High-Z	Data In	Write Byte d Bits Only	(I_{CC})
L	H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I_{CC})

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to V_{DD} + 0.5	V
V_{DD}	V_{DD} Relates to GND	−0.3 to 4.0	V
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V $\pm$ 5%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND $\leq V_{IN} \leq V_{DD}$	–1	1	µA
I_{LO}	Output Leakage	GND $\leq V_{OUT} \leq V_{DD}$, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND $\leq V_{IN} \leq V_{DD}$	–1	1	µA
I_{LO}	Output Leakage	GND $\leq V_{OUT} \leq V_{DD}$, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
I_{LI}	Input Leakage	GND $\leq V_{IN} \leq V_{DD}$		–1	1	µA
I_{LO}	Output Leakage	GND $\leq V_{OUT} \leq V_{DD}$, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width -2.0ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width -2.0ns). Not 100% tested.

HIGH SPEED

OPERATING RANGE (V$_{DD}$) (IS61WV51232ALL)

Range	Ambient Temperature	V$_{DD}$	Speed
Commercial	0°C to +70°C	1.65V-2.2V	20ns
Industrial	−40°C to +85°C	1.65V-2.2V	20ns
Automotive	−40°C to +125°C	1.65V-2.2V	20ns

OPERATING RANGE (V$_{DD}$) (IS61WV51232BLL)[1]

Range	Ambient Temperature	V$_{DD}$ (8 ns)[1]	V$_{DD}$ (10 ns)[1]
Commercial	0°C to +70°C	3.3V $\pm$ 5%	2.4V-3.6V
Industrial	−40°C to +85°C	3.3V $\pm$ 5%	2.4V-3.6V

Note:

1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V $\pm$ 5%, the device meets 8ns.

OPERATING RANGE (V$_{DD}$) (IS64WV51232BLL)

Range	Ambient Temperature	V$_{DD}$ (10 ns)
Automotive	−40°C to +125°C	2.4V-3.6V

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 Min.	-8 Max.	-10 Min.	-10 Max.	-20 Min.	-20 Max.	Unit
I$_{CC}$	V$_{DD}$ Dynamic Operating Supply Current	V$_{DD}$ = Max., I$_{OUT}$ = 0 mA, f = f$_{MAX}$	Com.	—	110	—	90	—	50	mA
			Ind.	—	115	—	95	—	60	
			Auto.	—	—	—	140	—	100	
			typ.[2]			60				
I$_{CC1}$	Operating Supply Current	V$_{DD}$ = Max., I$_{OUT}$ = 0 mA, f = 0	Com.	—	85	—	85	—	45	mA
			Ind.	—	90	—	90	—	55	
			Auto.	—	—	—	110	—	90	
I$_{SB1}$	TTL Standby Current (TTL Inputs)	V$_{DD}$ = Max., V$_{IN}$ = V$_{IH}$ or V$_{IL}$ $\overline{CE}$ ≥ V$_{IH}$, f = 0	Com.	—	30	—	30	—	30	mA
			Ind.	—	35	—	35	—	35	
			Auto.	—	—	—	70	—	70	
I$_{SB2}$	CMOS Standby Current (CMOS Inputs)	V$_{DD}$ = Max., $\overline{CE}$ ≥ V$_{DD}$ – 0.2V, V$_{IN}$ ≥ V$_{DD}$ – 0.2V, or V$_{IN}$ ≤ 0.2V, f = 0	Com.	—	20	—	20	—	20	mA
			Ind.	—	25	—	25	—	25	
			Auto.	—	—	—	60	—	60	
			typ.[2]			4				

Note:

1. At f = f$_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

2. Typical values are measured at V$_{DD}$ = 3.0V, T$_A$ = 25°C and not 100% tested.

LOW POWER

OPERATING RANGE (V$_{DD}$) (IS61WV51232ALS)

Range	Ambient Temperature	V$_{DD}$	Speed
Commercial	0°C to +70°C	1.65V-2.2V	35ns
Industrial	−40°C to +85°C	1.65V-2.2V	35ns
Automotive	−40°C to +125°C	1.65V-2.2V	35ns

OPERATING RANGE (V$_{DD}$) (IS61WV51232BLS)[1]

Range	Ambient Temperature	V$_{DD}$ (25 ns)[1]
Commercial	0°C to +70°C	2.4V-3.6V
Industrial	−40°C to +85°C	2.4V-3.6V

Note:

1. When operated in the range of 2.4V-3.6V, the device meets 25ns. When operated in the range of 3.3V $\pm$ 5%, the device meets 20ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
I$_{CC}$	V$_{DD}$ Dynamic Operating Supply Current	V$_{DD}$ = Max., I$_{OUT}$ = 0 mA, f = f$_{MAX}$	Com.	—	30	—	25	mA
			Ind.	—	35	—	30	
			Auto.	—	60	—	60	
			typ.[2]	25				
I$_{CC}$1	Operating Supply Current	V$_{DD}$ = Max., I$_{OUT}$ = 0 mA, f = 0	Com.	—	20	—	20	mA
			Ind.	—	30	—	30	
			Auto.	—	50	—	50	
I$_{SB1}$	TTL Standby Current (TTL Inputs)	V$_{DD}$ = Max., V$_{IN}$ = V$_{IH}$ or V$_{IL}$ $\overline{CE}$ ≥ V$_{IH}$, f = 0	Com.	—	15	—	15	mA
			Ind.	—	20	—	20	
			Auto.	—	40	—	40	
I$_{SB2}$	CMOS Standby Current (CMOS Inputs)	V$_{DD}$ = Max., $\overline{CE}$ ≥ V$_{DD}$ – 0.2V, V$_{IN}$ ≥ V$_{DD}$ – 0.2V, or V$_{IN}$ ≤ 0.2V, f = 0	Com.	—	0.8	—	0.8	mA
			Ind.	—	1.2	—	1.2	
			Auto.	—	2	—	2	
			typ.[2]	0.1		0.1		

Note:

1. At f = f$_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

2. Typical values are measured at V$_{DD}$ = 3.0V, T$_A$ = 25°C and not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

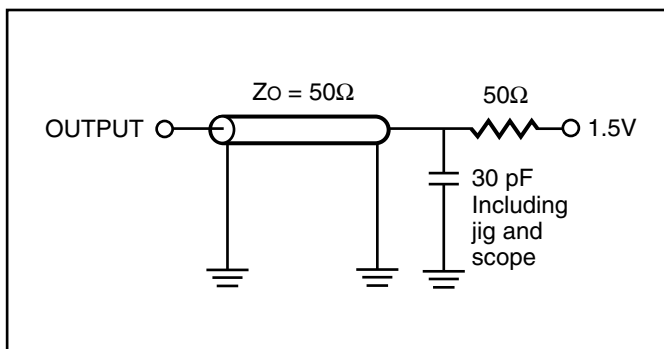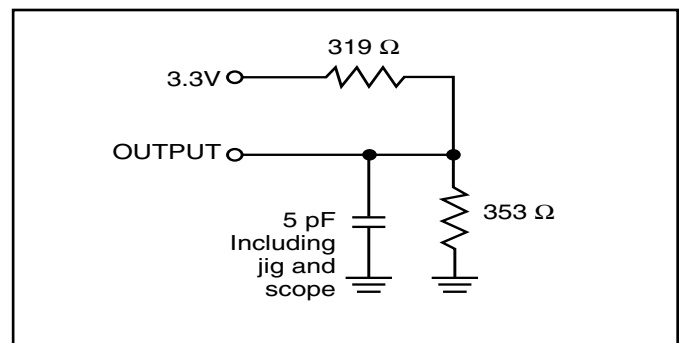| Parameter	Unit (2.4V-3.6V)	Unit (3.3V $\pm$ 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.2V
Input Rise and Fall Times	1.5ns	1.5ns	1.5ns
Input and Output Timing and Reference Level (V_{Ref})	V_{DD}/2	V_{DD}/2 + 0.05	V_{DD}/2
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2

AC TEST LOADS

Figure 1.

Figure 2.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	ns
t_{AA}	Address Access Time	—	8	—	10	ns
t_{OHA}	Output Hold Time	2.5	—	2.5	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5.5	—	6.5	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	3	—	4	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	3	0	4	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{BA}	Byte Enable to Data Valid	—	5.5	—	6.5	ns
t_{LZB}	Byte Enable to Low-Z	0	—	0	—	ns
t_{HZB}	Byte Enable to High-Z	0	3	0	3	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

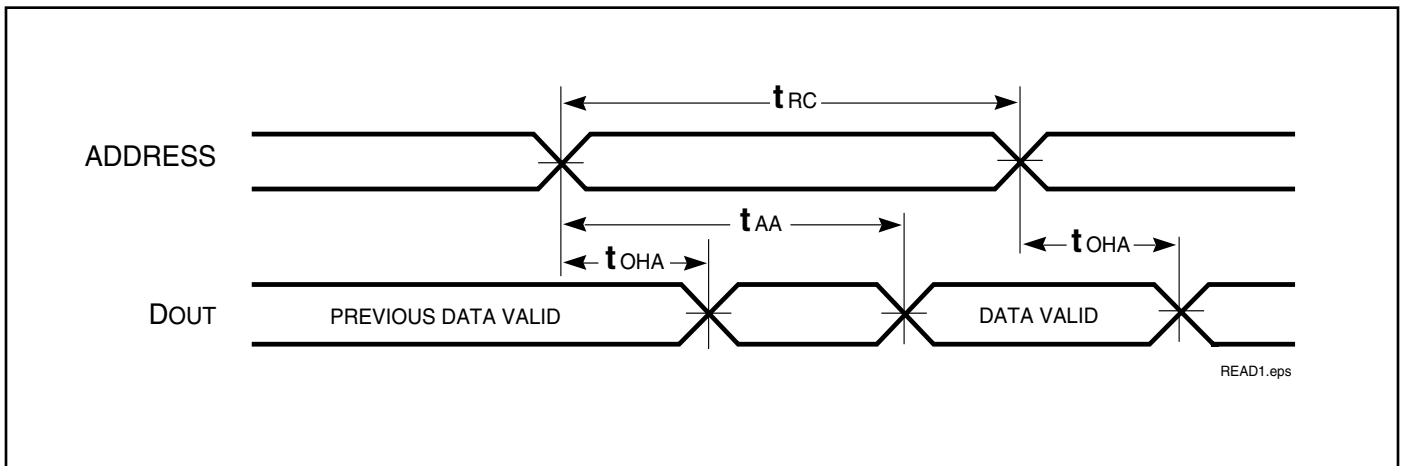## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol	Parameter	-20 ns Min.	Max.	Unit
t_{RC}	Read Cycle Time	20	—	ns
t_{AA}	Address Access Time	—	20	ns
t_{OHA}	Output Hold Time	2.5	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	8	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	ns
t_{BA}	Byte Enable to Data Valid	—	8	ns
t_{LZB}	Byte Enable to Low-Z	0	—	ns
t_{HZB}	Byte Enable to High-Z	0	3	ns

Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V$_{DD}$-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS
READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)

READ1.eps

READ CYCLE NO. 2[1,3] ($\overline{CE}$ and $\overline{OE}$ Controlled)

CE_RD2.eps
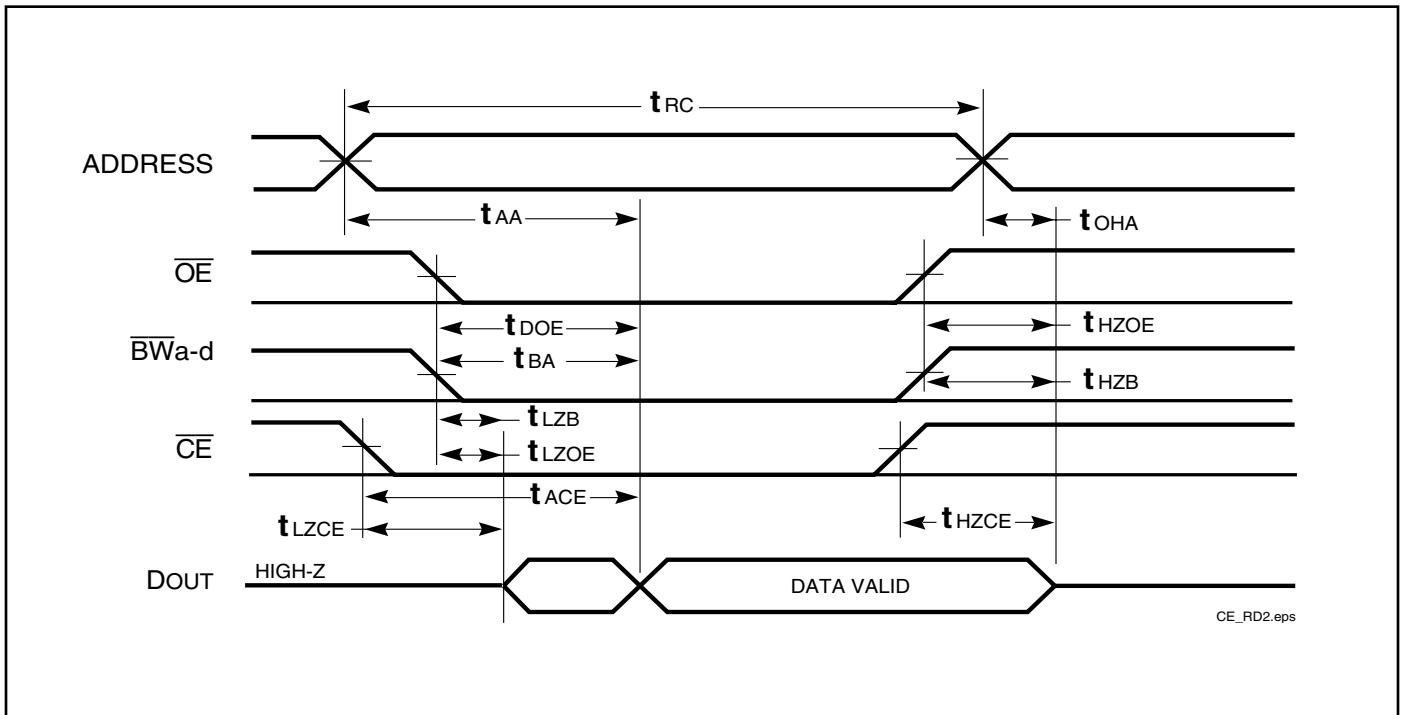
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	ns
t_{SCE}	$\overline{CE}$ to Write End	6.5	—	8	—	ns
t_{AW}	Address Setup Time to Write End	6.5	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{BW}$a-d Valid to End of Write	6.5	—	8	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width	6.5	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	8.0	—	10	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

## WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-20 ns		Unit
		Min.	Max.	
t_{WC}	Write Cycle Time	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	12	—	ns
t_{AW}	Address Setup Time to Write End	12	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWB}	$\overline{BW}$a-d Valid to End of Write	12	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	12	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	17	—	ns
t_{SD}	Data Setup to Write End	9	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	9	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	3	—	ns

Notes:
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
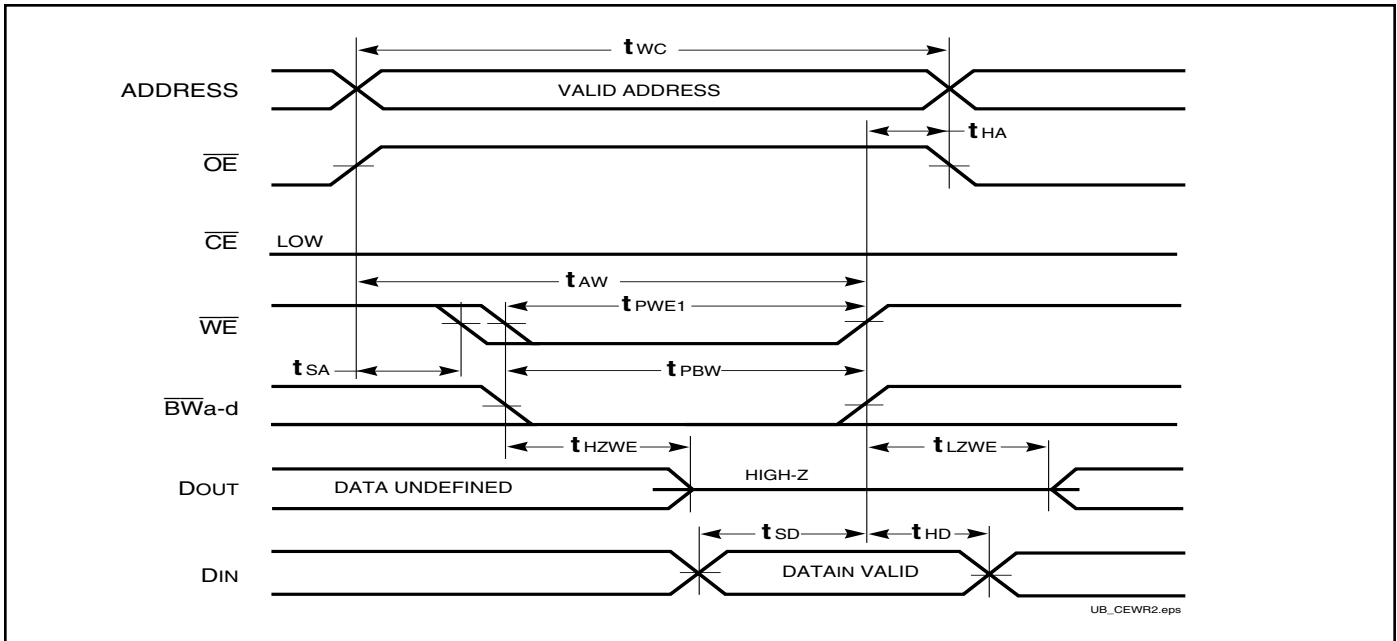
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)
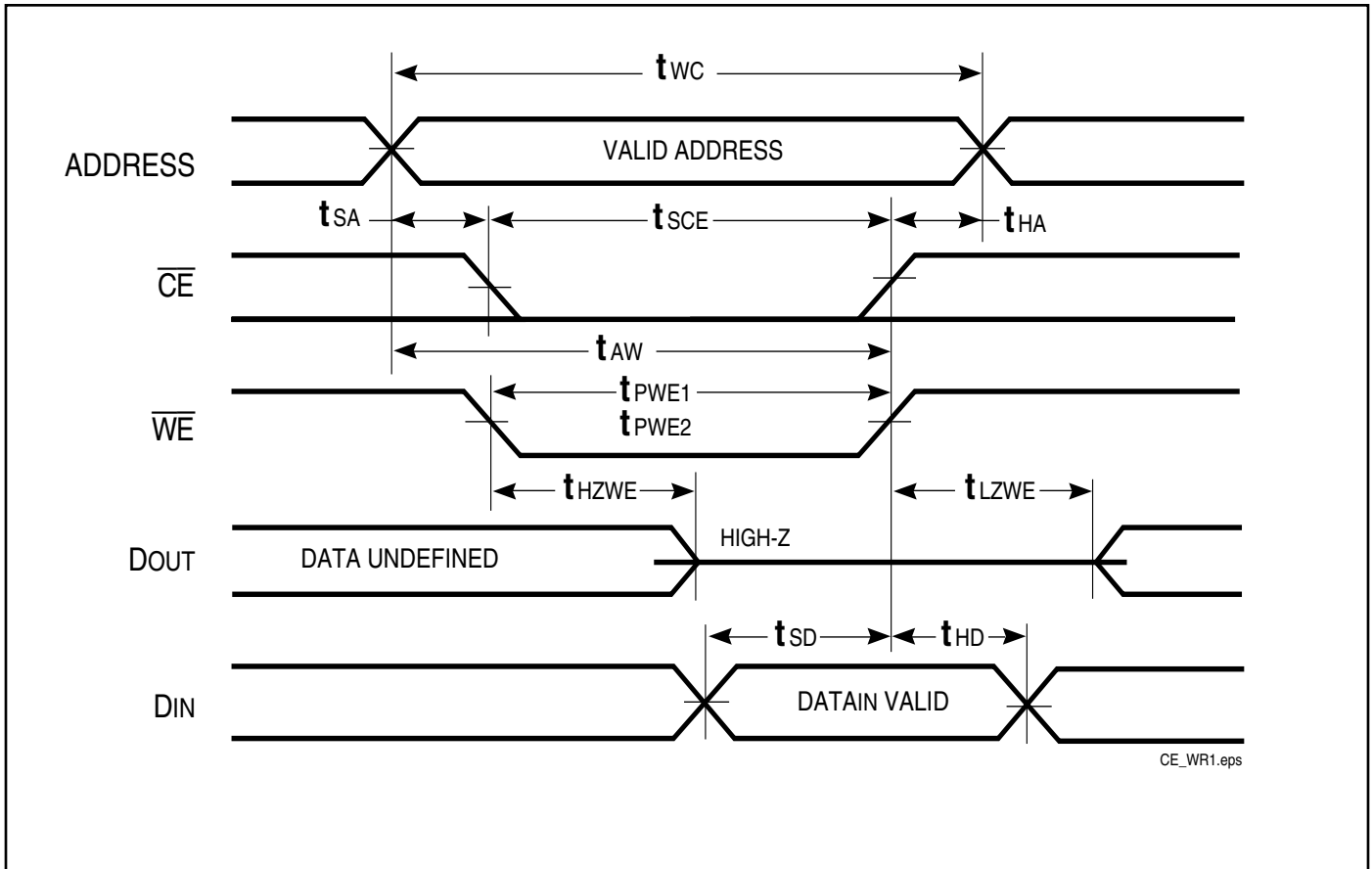
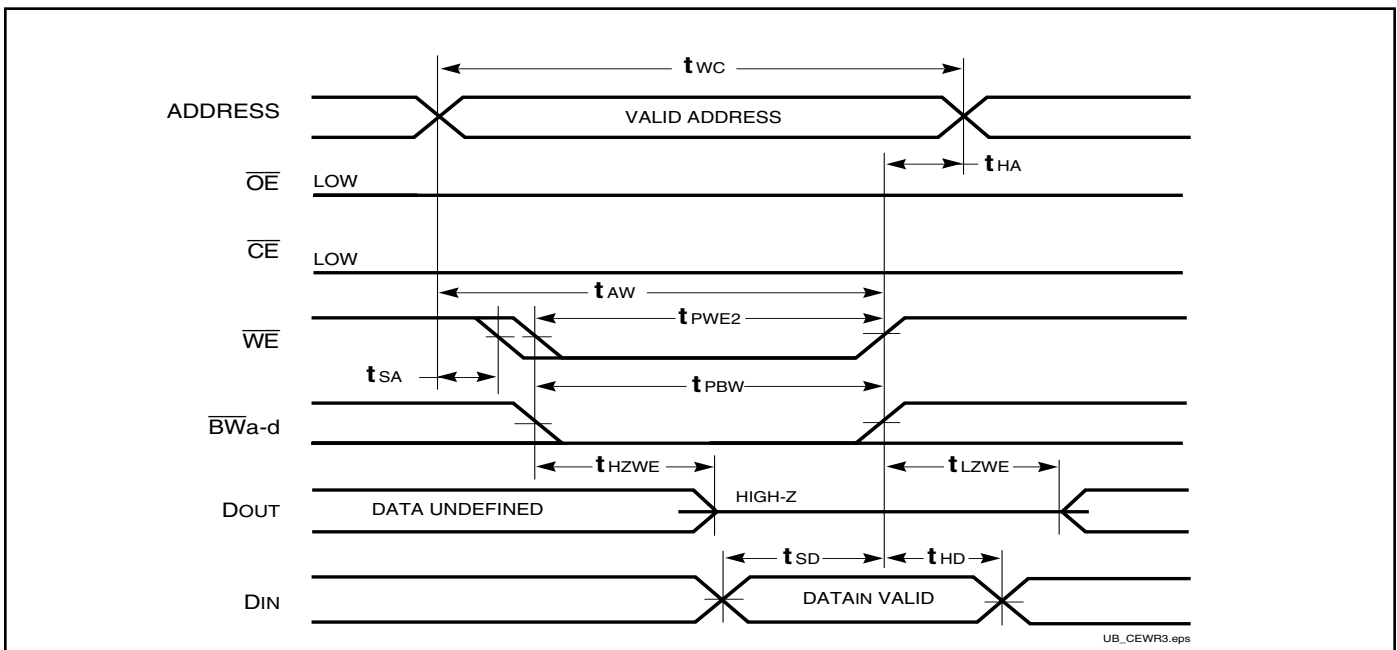## AC WAVEFORMS

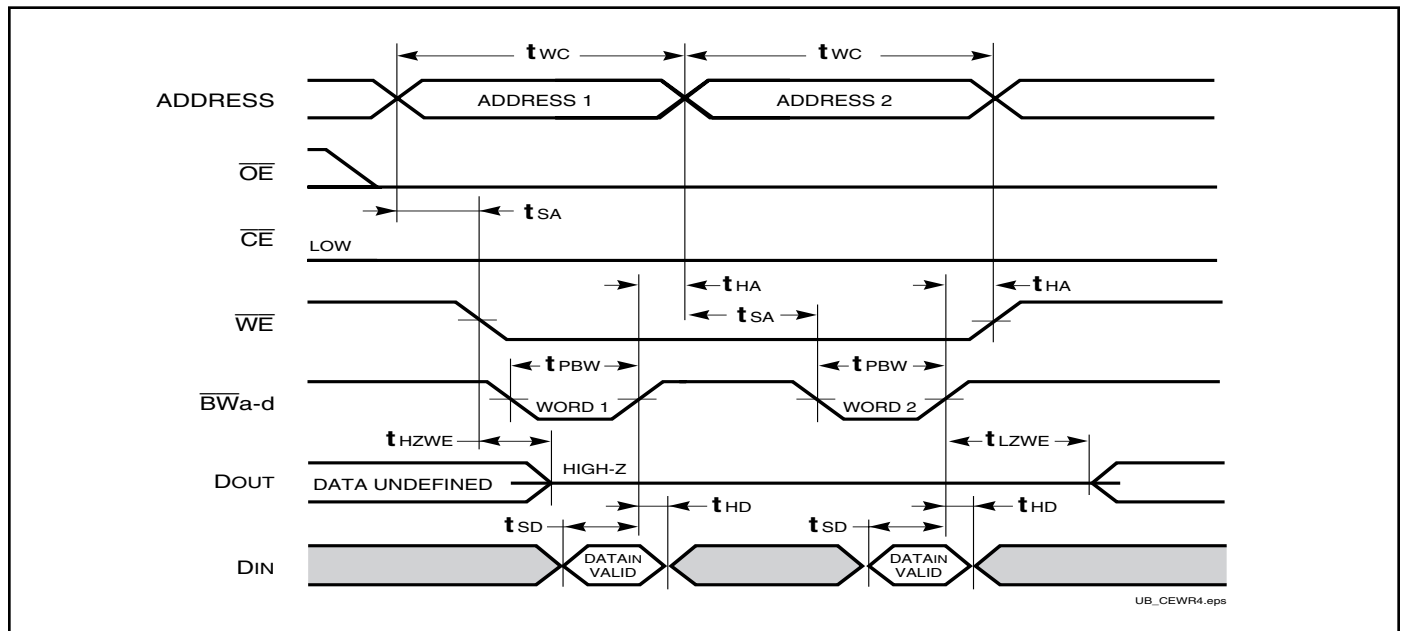### WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled. $\overline{OE}$ is HIGH During Write Cycle) [1,2]

UB_CEWR2.eps

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled. $\overline{OE}$ is LOW During Write Cycle) [1]

UB_CEWR3.eps

AC WAVEFORMS

WRITE CYCLE NO. 4 (Byte Controlled, Back-to-Back Write) [1,3]

UB_CEWR4.eps

Notes:
1. The internal Write time is defined by the overlap of and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA}, t_{HA}, t_{SD}, and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place the I/O in a HIGH-Z state.
3. $\overline{WE}$ may be held LOW across many address cycles and the $\overline{BW}$a-d pins can be used to control the Write function.

DATA RETENTION SWITCHING CHARACTERISTICS (HIGH SPEED) (IS61WV51232ALL/BLL)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V$, $\overline{CE} \geq V_{DD} - 0.2V$	Ind.	—	25	mA
			Auto.	—	60	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)

Integrated Silicon Solution, Inc. — www.issi.com

DATA RETENTION SWITCHING CHARACTERISTICS (LOW POWER) (IS61WV51232ALS/BLS)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_DR	V_DD for Data Retention	See Data Retention Waveform		1.2	3.6	V
I_DR	Data Retention Current	V_DD = 1.2V, $\overline{CE}$ ≥ V_DD – 0.2V	Ind. Auto.	— —	1.2 2	mA
t_SDR	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_RDR	Recovery Time	See Data Retention Waveform		t_RC	—	ns

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8[1])	IS61WV51232BLL-10BI	90-ball BGA (8mm x 13mm)
	IS61WV51232BLL-10BLI	90-ball BGA (8mm x 13mm), Lead-free

Note:
1. Speed = 8ns for V_{DD} = 3.3V $\pm$ 5%. Speed = 10ns for V_{DD} = 2.4V - 3.6V

Industrial Range: -40°C to +85°C

Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV51232ALL-20BI	90-ball BGA (8mm x 13mm)
	IS61WV51232ALL-20BLI	90-ball BGA (8mm x 13mm), Lead-free

Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS64WV51232BLL-10BA3	90-ball BGA (8mm x 13mm)

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.25	0.40	0.40	0.010	0.016	0.016
Øb	0.40	0.45	0.50	0.016	0.018	0.020
D	12.90	13.00	13.10	0.508	0.512	0.516
D1		11.20 BSC.			0.441 BSC.	
E	7.90	8.00	8.10	0.311	0.315	0.319
E1		6.40 BSC.			0.252 BSC.	
e		0.80 BSC.			0.031 BSC.	
ZD		0.9 REF.			0.035 REF.	
ZE		0.8 REF.			0.032 REF.	
y		0.10			0.004	

NOTE :

1. CONTROLLING DIMENSION : MM.
2. Reference document : JEDEC MO-207

BOTTOM VIEW

TOP VIEW

A1 CORNER

SEATING PLANE

Ball Diameter : 0.45

Ball Pitch : 0.80

TITLE	90L 8x13mm TF-BGA Package Outline	REV.	C
		DATE	11/24/2014