Vishay Semiconductors

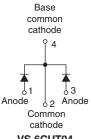
High Performance Schottky Generation 5.0, 2 x 3 A

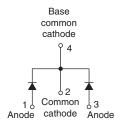




I-PAK (TO-251AA)

D-PAK (TO-252AA)





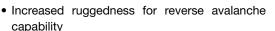
VS-6CUT04

VS-6CWT04FN

PRODUCT SUMMARY				
Package	D-PAK (TO-252AA), I-PAK (TO-251AA)			
I _{F(AV)}	2 x 3 A			
V_{R}	45 V			
V _F at I _F	0.54 V			
I _{RM} max.	3 mA at 125 °C			
T _J max.	175 °C			
Diode variation	Common cathode			
E _{AS}	14 mJ			

FEATURES

- 175 °C high performance Schottky diode
- · Very low forward voltage drop
- Extremely low reverse leakage
- Optimized V_F vs. I_R trade off for high efficiency



- RBSOA available
- · Negligible switching losses
- Submicron trench technology
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Specific for PV cells pybass diode
- High efficiency SMPS
- · High frequency switching
- Output rectification
- · Reverse battery protection
- Freewheeling
- DC/DC systems
- Increased power density systems

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VALUES	UNITS		
V _{RRM}		45	V		
V _F	3 Apk, T _J = 125 °C (typical, per leg)	0.46	V		
T _J	Range	- 55 to 175	°C		

VOLTAGE RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VS-6CUT04 VS-6CWT04FN	UNITS
Maximum DC reverse voltage	V_{R}	T _J = 25 °C	45	V

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ABSOLUTE MAXIMUM RATINGS							
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS		
Maximum average per le		50 % duty cycle at T _C = 166 °C, rectangular waveform		50.0/ duty quals at T 166.0C vactor gular years form		3	^
forward current per device	e I _{F(AV)}			6	Α		
Maximum peak one cycle		5 μs sine or 3 μs rect. pulse Following any rated load condition and with rated		440) A		
non-repetitive surge current per le	I IFSM	10 ms sine or 6 ms rect. pulse	V _{RRM} applied	70	A		
Non-repetitive avalanche energy per leg	E _{AS}	T _J = 25 °C, I _{AS} = 1.3 A, L = 16 mH		14	mJ		
Repetitive avalanche current per le	g l _{AR}	Limited by frequency of operation and time pulse duration so that $T_J < T_J max$. I_{AS} at $T_J max$. as a function of time pulse (see fig. 8)		I _{AS} at T _J max.	А		

ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Forward voltage drop per leg	V _{FM} ⁽¹⁾	3 A	T _J = 25 °C	0.535	0.600	V
		6 A		0.615	0.680	
		3 A	T _J = 125 °C	0.485	0.540	
		6 A		0.570	0.640	
Reverse leakage current per leg	I _{RM} ⁽¹⁾	T _J = 25 °C	V _R = Rated V _R	-	25	μΑ
		T _J = 125 °C		=	3	mA
Junction capacitance per leg	C _T	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz), 25 °C		240	-	pF
Series inductance per leg	L _S	Measured lead to lead 5 mm from package body		8.0	-	nΗ
Maximum voltage rate of change	dV/dt	Rated V _R		-	10 000	V/µs

Note

 $^{^{(1)}\,}$ Pulse width < 300 $\mu s,$ duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	MBOL TEST CONDITIONS		UNITS
Maximum junction and storage temperature range	T_J , T_{Stg}		- 55 to 175	°C
Maximum thermal resistance, junction to case per leg	В	DC operation	4.7	
Maximum thermal resistance, junction to case per device	R _{thJC}		2.35	°C/W
Typical thermal resistance, case to heatsink	R _{thCS}		0.3	
Approximate weight			0.3	g
			0.01	OZ.
Made at the		Case style I-PAK	6CL	JT04
Marking device		Case style D-PAK	6CWT	04FN

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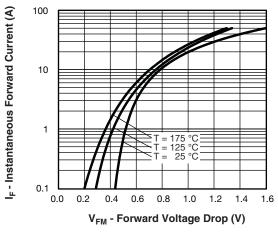


Fig. 1 - Maximum Forward Voltage Drop Characteristics

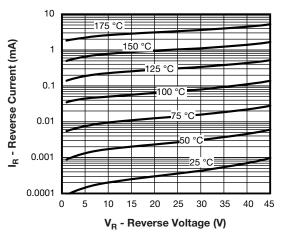


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

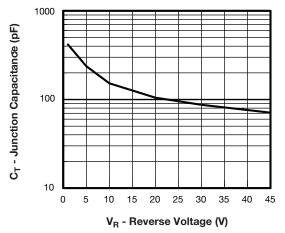


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

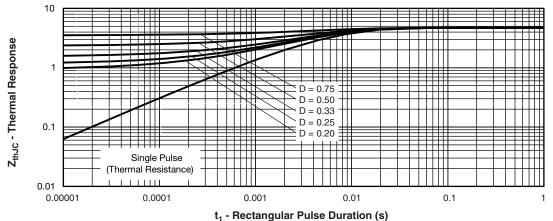


Fig. 4 - Maximum Thermal Impedance Z_{th,IC} Characteristics

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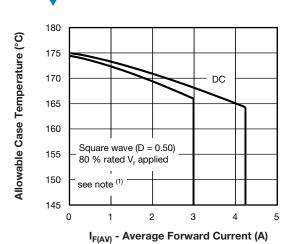


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

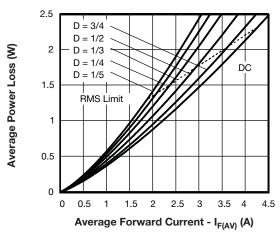


Fig. 6 - Forward Power Loss Characteristics

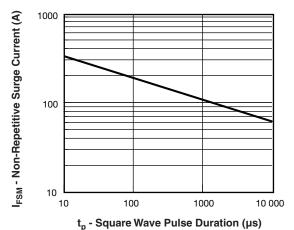


Fig. 7 - Maximum Non-Repetitive Surge Current

Note

⁽¹⁾ Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$; Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6); Pd_{REV} = Inverse power loss = $V_{R1} \times I_R$ (1 - D); I_R at V_{R1} = 80 % rated V_R www.vishay.com

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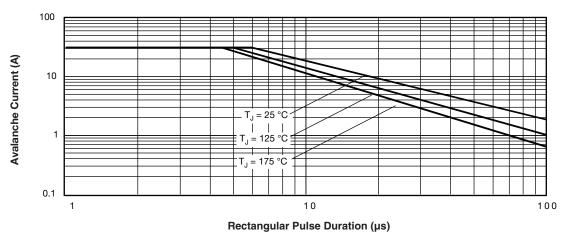


Fig. 8 - Reverse Bias Safe Operating Area (Avalanche Current vs. Rectangular Pulse Duration)

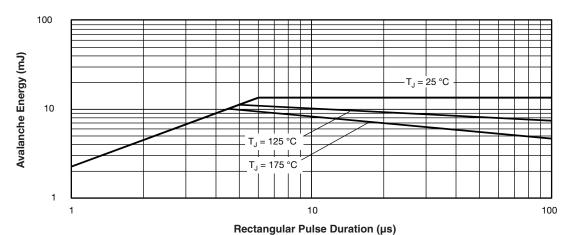
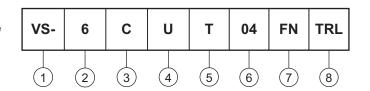


Fig. 9 - Reverse Bias Safe Operating Area (Avalanche Energy vs. Rectangular Pulse Duration)

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ORDERING INFORMATION TABLE

Device code



Vishay Semiconductors product

Current rating (6 A)

- Circuit configuration:

C = Common cathode

4 - Package:

• U = I-PAK

•W=D-PAK

5 - T = Trench

6 - Voltage rating (04 = 45 V)

TO-252AA (D-PAK)

8 - D-PAK, I-PAK:

None = Tube (75 pieces)

D-PAK only:

• TR = Tape and reel

• TRL = Tape and reel (left oriented)

• TRR = Tape and reel (right oriented)

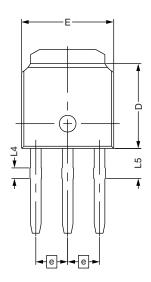
LINKS TO RELATED DOCUMENTS				
Dimensions	I-PAK (TO-251AA)	www.vishay.com/doc?95024		
Dimensions	D-PAK (TO-252AA)	www.vishay.com/doc?95448		
Part marking information	I-PAK (TO-251AA)	www.vishay.com/doc?95025		
	D-PAK (TO-252AA)	www.vishay.com/doc?95059		
Packaging information		www.vishay.com/doc?95033		
SPICE model		www.vishay.com/doc?95038		

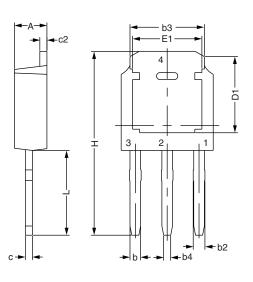


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I-PAK - S

DIMENSIONS FOR I-PAK - S in millimeters





SYMBOL	DIMENSIONAL REQUIREMENTS			
STIMBOL	MIN.	NOM.	MAX.	
E	6.40	6.60	6.70	
L	3.98	4.13	4.28	
L4	0.66	0.76	0.86	
L5	1.96	2.16	2.36	
D	6.00	6.10	6.20	
Н	11.05	11.25	11.45	
b	0.64	0.76	0.88	
b2	0.77	0.84	1.14	
b3	5.21	5.34	5.46	
b4	0.41	0.51	0.61	
е	2.286 BSC			
А	2.20	2.30	2.38	
С	0.40	0.50	0.60	
c2	0.40	0.50	0.60	
D1	5.30	-	-	
E1	4.40	-	-	



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