# CAT130xx

# Voltage Supervisor with Microwire Serial CMOS EEPROM

## Description

The CAT130xx (see table below) are memory and supervisory solutions for microcontroller based systems. A CMOS serial EEPROM memory and a system power supervisor with brown−out protection are integrated together. Memory interface is via Microwire serial protocol.

The CAT130xx provides a precision $V_{CC}$ sense circuit with two reset output options: CMOS active low output or CMOS active high. The RESET output is active whenever $V_{CC}$ is below the reset threshold or falls below the reset threshold voltage.

The power supply monitor and reset circuit protect system controllers during power up/down and against brownout conditions. Seven reset threshold voltages support 5 V, 3.3 V, 3 V and 2.5 V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 240 ms after the supply voltage exceeds the reset threshold level.

## Features

- Precision Power Supply Voltage Monitor
  - ♦ 5 V, 3.3 V, 3 V and 2.5 V Systems
  - ♦ 7 Threshold Voltage Options
- Active High or Low Reset
  - ♦ Valid Reset Guaranteed at $V_{CC} = 1$ V
- High Speed Operation
- Selectable x8 or x16 Memory Organization
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial Temperature Range
- RoHS−Compliant 8−Pin SOIC Package
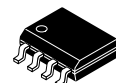- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

## THRESHOLD SUFFIX SELECTOR

| Nominal Threshold Voltage | Threshold Suffix Designation |
|---|---|
| 4.63 V | L |
| 4.38 V | M |
| 4.00 V | J |
| 3.08 V | T |
| 2.93 V | S |
| 2.63 V | R |
| 2.32 V | Z |

## ON Semiconductor®

**SOIC−8**
**CASE 751BD**

## PIN CONFIGURATION

SOIC (W)

| | | | |
|---|---|---|---|
| CS | 1 | 8 | $V_{CC}$ |
| SK | 2 | 7 | RST/$\overline{RST}$ |
| DI | 3 | 6 | ORG |
| DO | 4 | 5 | GND |
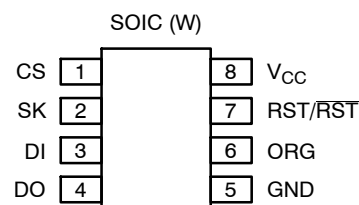
## PIN FUNCTION

| Pin Name | Function |
|---|---|
| CS | Chip Select |
| SK | Clock Input |
| DI | Serial Data Input |
| DO | Serial Data Output |
| GND | Ground |
| ORG | Memory Organization |
| RST/$\overline{RST}$ | Reset Output |
| $V_{CC}$ | Power Supply |

NOTE:
When the ORG pin is connected to $V_{CC}$, the x16 organization is selected. When it is connected to ground, the x8 pin is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.
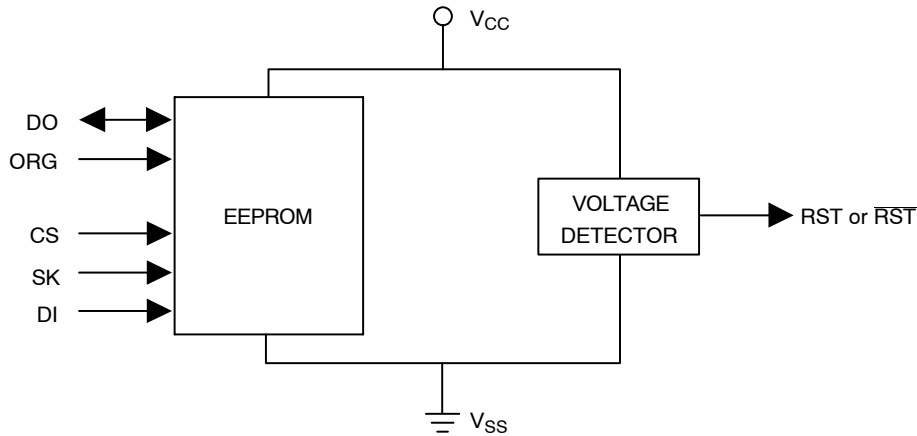
## MEMORY SIZE SELECTOR

| Product | Memory Density |
|---|---|
| 13001 | 1−Kbit |
| 13004 | 4−Kbit |
| 13008 | 8−Kbit |
| 13016 | 16−Kbit |

## ORDERING INFORMATION

**November, 2011 – Rev. 3**

# CAT130xx

## BLOCK DIAGRAM



## SPECIFICATIONS

### Table 1. ABSOLUTE MAXIMUM RATINGS

| Parameters | Ratings | Units |
|---|---|---|
| Storage Temperature | −65 to +150 | °C |
| Voltage on Any Pin with Respect to Ground (Note 1) | −0.5 to +6.5 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than $V_{CC}$ + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than $V_{CC}$ + 1.5 V, for periods of less than 20 ns.

### Table 2. RELIABILITY CHARACTERISTICS (Note 2)

| Symbol | Parameter | Min | Units |
|---|---|---|---|
| NEND (Note 3) | Endurance | 1,000,000 | Program/ Erase Cycles |
| TDR | Data Retention | 100 | Years |

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Block Mode, $V_{CC}$ = 5 V, 25°C

### Table 3. D.C. OPERATING CHARACTERISTICS

$V_{CC}$ = +2.5 V to +5.5 V, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply Current | Read or Write at 1 MHz | | | 3 | mA |
| $I_{SB}$ | Standby Current | $V_{CC}$ < 5.5 V; All I/O Pins at $V_{SS}$ or $V_{CC}$ | | 12 | 25 | μA |
| | | $V_{CC}$ < 3.6 V; All I/O Pins at $V_{SS}$ or $V_{CC}$ | | 10 | 20 | |
| $I_L$ | I/O Pin Leakage | Pin at GND or $V_{CC}$ | | | 2 | μA |
| $V_{IL}$ | Input Low Voltage | | −0.5 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $V_{CC} \geq$ 2.5 V, $I_{OL}$ = 2.1 mA | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $V_{CC} \geq$ 4.5 V, $I_{OL}$ = −0.4 mA | 2.4 | | | V |

### Table 4. A.C. CHARACTERISTICS (MEMORY) (Note 1)

$V_{CC}$ = +2.5 V to 5.5 V, $T_A$ = −40°C to 85°C, unless otherwise specified.

| Symbol | Parameter | Min | Max | Units |
|:---:|:---|:---:|:---:|:---:|
| $f_{SK}$ | Clock Frequency | DC | 2000 | kHz |
| $t_{CSS}$ | CS Setup Time | 50 | | ns |
| $t_{CSH}$ | CS Hold Time | 0 | | ns |
| $t_{CSMIN}$ | Minimum CS Low Time | 0.25 | | μs |
| $t_{SKHI}$ | Minimum SK High Time | 0.25 | | μs |
| $t_{SKLOW}$ | Minimum SK Low Time | 0.25 | | μs |
| $t_{DIS}$ | DI Setup Time | 100 | | ns |
| $t_{DIH}$ | DI Hold Time | 100 | | ns |
| $t_{PD1}$ | Output Delay to 1 | | 0.25 | μs |
| $t_{PD0}$ | Output Delay to 0 | | 0.25 | μs |
| $t_{HZ}$ (Note 1) | Output Delay to High−Z | | 100 | ns |
| $t_{SV}$ | Output Delay to Status Valid | | 0.25 | μs |
| $t_{EW}$ | Program/Erase Pulse Width | | 5 | ms |
| $t_{PU}$ (Notes 2 & 3) | Power−up to Ready Mode | | 1 | ms |

1. Test conditions according to "A.C. Test Conditions" table.
2. Tested initially and after a design or process change that affects this parameter.
3. $t_{PU}$ is the delay between the time $V_{CC}$ is stable and the device is ready to accept commands.

### Table 5. A.C. TEST CONDITIONS

| Parameter | Test Conditions |
|:---|:---:|
| Input Rise and Fall Times | ≤50 ns |
| Input Levels | 0.4 V to 2.4 V (4.5 V < $V_{CC}$ < 5.5 V) |
| Input Levels | 0.2 $V_{CC}$ to 0.7 $V_{CC}$ (2.5 V < $V_{CC}$ < 4.5 V) |
| Timing Reference Levels | 0.8 V, 2.0 V (4.5 V < $V_{CC}$ < 5.5 V) |
| Timing Reference Levels | 0.5 $V_{CC}$ (2.5 V < $V_{CC}$ < 4.5 V) |
| Output Load | Current Source: $I_{OL\ max}$ / $I_{OH\ max}$; $C_L$ = 100 pF |

**Table 6. ELECTRICAL CHARACTERISTICS (SUPERVISORY FUNCTION)**

$V_{CC}$ = Full range, $T_A$ = −40°C to +85°C unless otherwise noted. Typical values at $T_A$ = +25°C and $V_{CC}$ = 5 V for L/M/J versions, $V_{CC}$ = 3.3 V for T/S versions, $V_{CC}$ = 3 V for R version and $V_{CC}$ = 2.5 V for Z version.

| Symbol | Parameter | Threshold | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{TH}$ | Reset Threshold Voltage | L | $T_A$ = +25°C | 4.56 | 4.63 | 4.70 | V |
| | | | $T_A$ = −40°C to +85°C | 4.50 | | 4.75 | |
| | | M | $T_A$ = +25°C | 4.31 | 4.38 | 4.45 | |
| | | | $T_A$ = −40°C to +85°C | 4.25 | | 4.50 | |
| | | J | $T_A$ = +25°C | 3.93 | 4.00 | 4.06 | |
| | | | $T_A$ = −40°C to +85°C | 3.89 | | 4.10 | |
| | | T | $T_A$ = +25°C | 3.04 | 3.08 | 3.11 | |
| | | | $T_A$ = −40°C to +85°C | 3.00 | | 3.15 | |
| | | S | $T_A$ = +25°C | 2.89 | 2.93 | 2.96 | |
| | | | $T_A$ = −40°C to +85°C | 2.85 | | 3.00 | |
| | | R | $T_A$ = +25°C | 2.59 | 2.63 | 2.66 | |
| | | | $T_A$ = −40°C to +85°C | 2.55 | | 2.70 | |
| | | Z | $T_A$ = +25°C | 2.28 | 2.32 | 2.35 | |
| | | | $T_A$ = −40°C to +85°C | 2.25 | | 2.38 | |

| Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|
| | Reset Threshold Tempco | | | 30 | | ppm/°C |
| $t_{RPD}$ | $V_{CC}$ to Reset Delay (Note 2) | $V_{CC}$ = $V_{TH}$ to ($V_{TH}$ −100 mV) | | 20 | | μs |
| $t_{PURST}$ | Reset Active Timeout Period | $T_A$ = −40°C to +85°C | 140 | 240 | 460 | ms |
| $V_{OL}$ | $\overline{\text{RESET}}$ Output Voltage Low (Push−pull, Active LOW, CAT130xx9) | $V_{CC}$ = $V_{TH}$ min, $I_{SINK}$ = 1.2 mA R/S/T/Z | | | 0.3 | V |
| | | $V_{CC}$ = $V_{TH}$ min, $I_{SINK}$ = 3.2 mA J/L/M | | | 0.4 | |
| | | $V_{CC}$ > 1.0 V, $I_{SINK}$ = 50 μA | | | 0.3 | |
| $V_{OH}$ | $\overline{\text{RESET}}$ Output Voltage High (Push−pull, Active LOW, CAT130xx9) | $V_{CC}$ = $V_{TH}$ max, $I_{SOURCE}$ = −500 μA R/S/T/Z | 0.8 $V_{CC}$ | | | V |
| | | $V_{CC}$ = $V_{TH}$ max, $I_{SOURCE}$ = −800 μA J/L/M | $V_{CC}$ − 1.5 | | | |
| $V_{OL}$ | RESET Output Voltage Low (Push−pull, Active HIGH, CAT130xx1) | $V_{CC}$ > $V_{TH}$ max, $I_{SINK}$ = 1.2 mA R/S/T/Z | | | 0.3 | V |
| | | $V_{CC}$ > $V_{TH}$ max, $I_{SINK}$ = 3.2 mA J/L/M | | | 0.4 | |
| $V_{OH}$ | RESET Output Voltage High (Push−pull, Active HIGH, CAT130xx1) | 1.8 V < $V_{CC}$ ≤ $V_{TH}$ min, $I_{SOURCE}$ = −150 μA | 0.8 $V_{CC}$ | | | V |

1. Production testing done at $T_A$ = +25°C; limits over temperature guaranteed by design only.
2. $\overline{\text{RESET}}$ output for the CAT130xx9; RESET output for the CAT130xx1.

# CAT130xx

## PIN DESCRIPTION

**RESET**/$\overline{\text{RESET}}$: The reset output is available in two versions: CMOS Active Low (CAT130xx9) and CMOS Active High (CAT130xx1). Both versions are push−pull outputs for high efficiency.

**DI**: The serial data input pin accepts op−codes, addresses and data. The input data is latched on the rising edge of the SK clock input.

**SK**: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and CAT130xx device.

**CS**: The chip select input pin is used to enable/disable the CAT130xx. When CS is high, the device is selected and accepts op−codes, addresses and data. Upon receiving a Write or Erase instruction, the falling edge of CS will start the internal write cycle to the selected memory location.

**ORG**: The memory organization input selects the memory configuration as either register of 16 bits (ORG tied to $V_{CC}$ or floating) or 8 bits (ORG connected to GND).

## DEVICE OPERATION

The CAT130xx products combine the accurate voltage monitoring capabilities of a standalone voltage supervisor with the high quality and reliability of standard EEPROMs from ON Semiconductor.

### Reset Controller Description

The reset signal is asserted LOW for the CAT130xx9 and HIGH for the CAT130xx1 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140 ms ($t_{PURST}$) after the power supply voltage has risen above the threshold. Reset output timing is shown in Figure 2.

The CAT130xx devices protect μPs against brownout failure. Short duration $V_{CC}$ transients of 4 μsec or less and 100 mV amplitude typically do not generate a Reset pulse.

Figure 1 shows the maximum pulse duration of negative−going $V_{CC}$ transients that do not cause a reset condition. As the amplitude of the transient goes further below the threshold (increasing $V_{TH} − V_{CC}$), the maximum pulse duration decreases. In this test, the $V_{CC}$ starts from an

initial voltage of 0.5 V above the threshold and drops below it by the amplitude of the overdrive voltage ($V_{TH} − V_{CC}$).
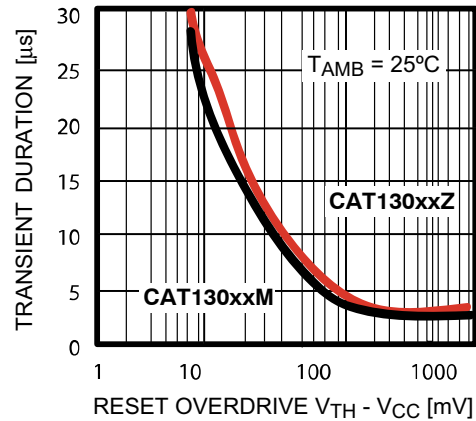


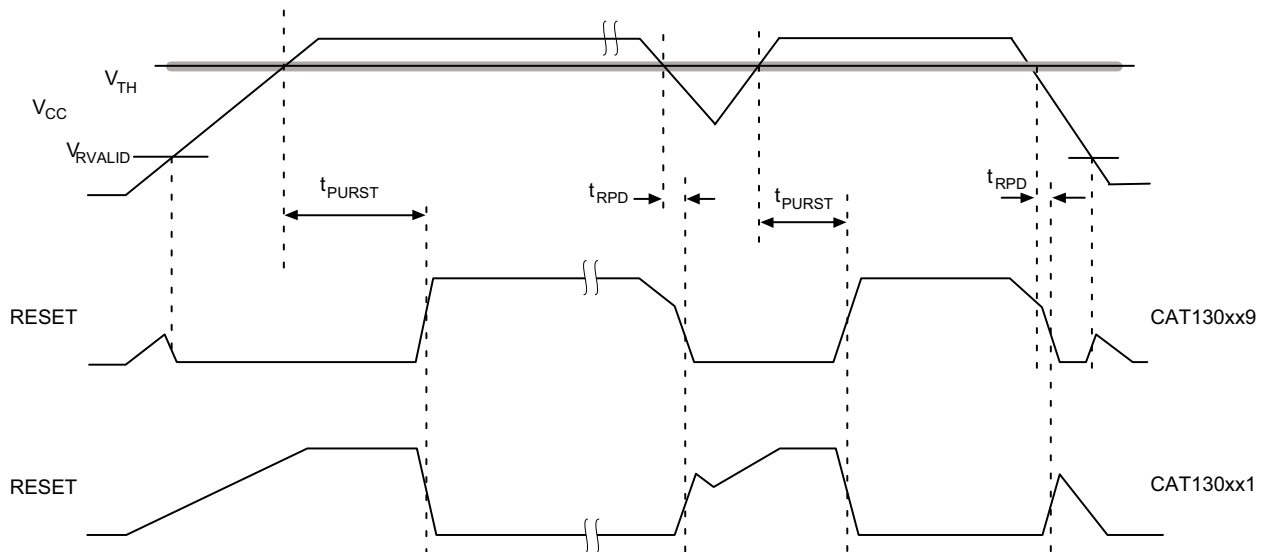**Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Overdrive Voltage**



**Figure 2. RESET Output Timing**

## EMBEDDED EEPROM OPERATION

The CAT130xx has a nonvolatile embedded memory intended for use with industry standard microprocessors. The memory can be organized as either registers of 16 bits or 8 bits. The CAT130xx operates on a single power supply and will generate on chip the high voltage required during any write operation.

The format for all instructions sent to the device is a logical "1" start bit, a 2−bit (or 4−bit) opcode, 6−bit (13001) / 8−bit (13004) / 9−bit (13008) / 10−bit (13016) address (an additional bit when organized as x8) and for write operations a 16−bit data field (8−bit for x8 organization). The instruction format is shown in Instruction Set Table.

**Table 7. INSTRUCTION SET**

| Instruction | Device | Start Bit | Opcode | Address x 8 | Address x 16 | Data x 8 | Data x 16 | Comments |
|---|---|---|---|---|---|---|---|---|
| READ | 13001 | 1 | 10 | A6−A0 | A5−A0 | | | Read Address AN−A0 |
| | 13004 | 1 | 10 | A8−A0 | A7−A0 | | | |
| | 13008 | 1 | 10 | A9−A0 | A8−A0 | | | |
| | 13016 | 1 | 10 | A10−A0 | A9−A0 | | | |
| ERASE | 13001 | 1 | 11 | A6−A0 | A5−A0 | | | Clear Address AN−A0 |
| | 13004 | 1 | 11 | A8−A0 | A7−A0 | | | |
| | 13008 | 1 | 11 | A9−A0 | A8−A0 | | | |
| | 13016 | 1 | 11 | A10−A0 | A9−A0 | | | |
| WRITE | 13001 | 1 | 01 | A6−A0 | A5−A0 | D7−D0 | D15−D0 | Write Address AN−A0 |
| | 13004 | 1 | 01 | A8−A0 | A7−A0 | D7−D0 | D15−D0 | |
| | 13008 | 1 | 01 | A9−A0 | A8−A0 | D7−D0 | D15−D0 | |
| | 13016 | 1 | 01 | A10−A0 | A9−A0 | D7−D0 | D15−D0 | |
| EWEN | 13001 | 1 | 00 | 11xxxxx | 11xxxx | | | Write Enable |
| | 13004 | 1 | 00 | 11xxxxxxx | 11xxxxxx | | | |
| | 13008 | 1 | 00 | 11xxxxxxxx | 11xxxxxxx | | | |
| | 13016 | 1 | 00 | 11xxxxxxxxx | 11xxxxxxxx | | | |
| EWDS | 13001 | 1 | 00 | 00xxxxx | 00xxxx | | | Write Disable |
| | 13004 | 1 | 00 | 00xxxxxxx | 00xxxxxx | | | |
| | 13008 | 1 | 00 | 00xxxxxxxx | 00xxxxxxx | | | |
| | 13016 | 1 | 00 | 00xxxxxxxxx | 00xxxxxxxx | | | |
| ERAL | 13001 | 1 | 00 | 10xxxxx | 10xxxx | | | Clear All Addresses |
| | 13004 | 1 | 00 | 10xxxxxxx | 10xxxxxx | | | |
| | 13008 | 1 | 00 | 10xxxxxxxx | 10xxxxxxx | | | |
| | 13016 | 1 | 00 | 10xxxxxxxxx | 10xxxxxxxx | | | |
| WRAL | 13001 | 1 | 00 | 01xxxxx | 01xxxx | D7−D0 | D15−D0 | Write All Address |
| | 13004 | 1 | 00 | 01xxxxxxx | 01xxxxxx | D7−D0 | D15−D0 | |
| | 13008 | 1 | 00 | 01xxxxxxxx | 01xxxxxxx | D7−D0 | D15−D0 | |
| | 13016 | 1 | 00 | 01xxxxxxxxx | 01xxxxxxxx | D7−D0 | D15−D0 | |

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status during a write operation. The serial communication protocol follows the timing shown in Figure 3.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The Ready/Busy flag can be disabled only in Ready state; no change is allowed in Busy state.

**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT130xx will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ($t_{PD0}$ or $t_{PD1}$). The READ instruction timing is illustrated in Figure 4.

For the CAT13004/08/16, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.
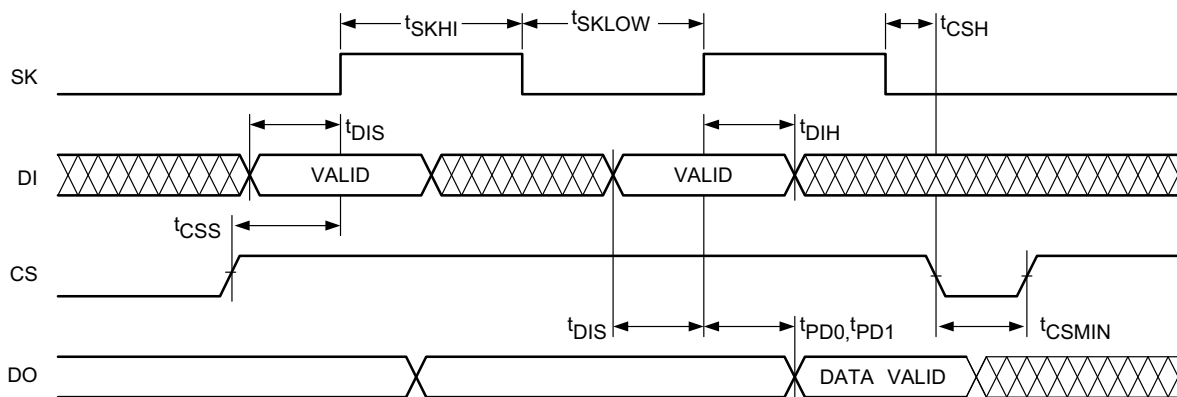


**Figure 3. Synchronous Data Timing**
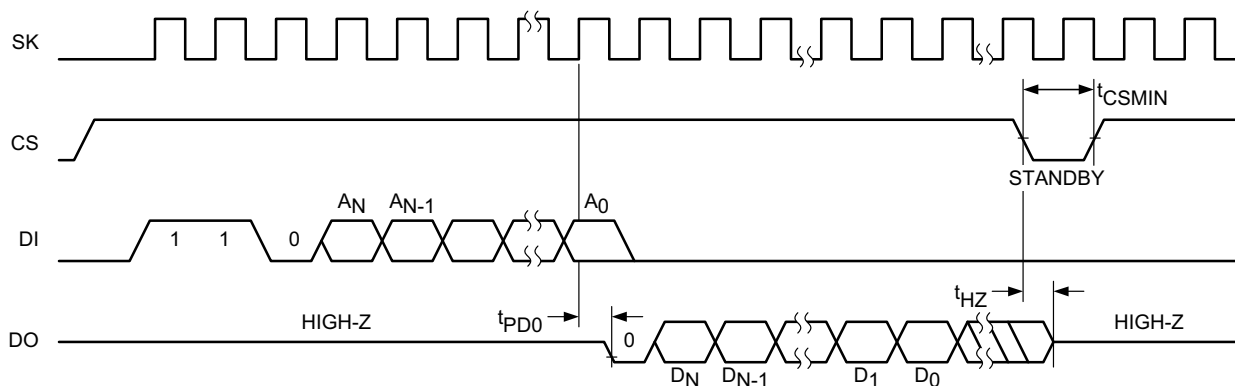


**Figure 4. Read Instruction Timing**

# CAT130xx

**Erase/Write Enable and Disable**

The CAT130xx powers up in the write disable state. Any writing after power−up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT130xx write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 5.

**Write**

After receiving a WRITE command (Figure 6), address and the data, the CS (Chip Select) pin must be deselected for a minimum of $t_{CSMIN}$. The falling edge of CS will start the self clocking for auto−clear and data store cycles on the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT130xx can be determined by selecting the device and polling the DO pin. Since this device features Auto−Clear before write, it is NOT necessary to erase a memory location before it is written into.
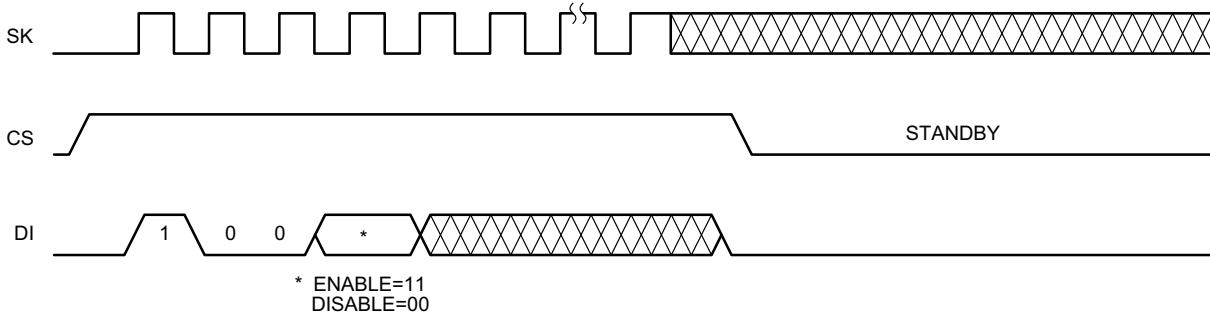
**Figure 5. EWEN/EWDS Instruction Timing**
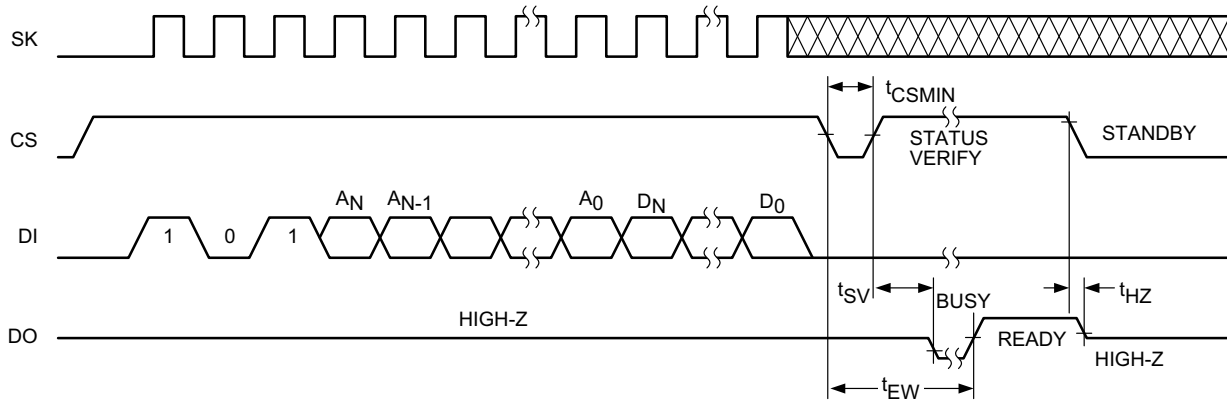
**Figure 6. Write Instruction Timing**

## Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of $t_{CSMIN}$ (Figure 7). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT130xx can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

## Erase All

Upon receiving an ERAL command (Figure 8), the CS (Chip Select) pin must be deselected for a minimum of $t_{CSMIN}$. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT130xx can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.
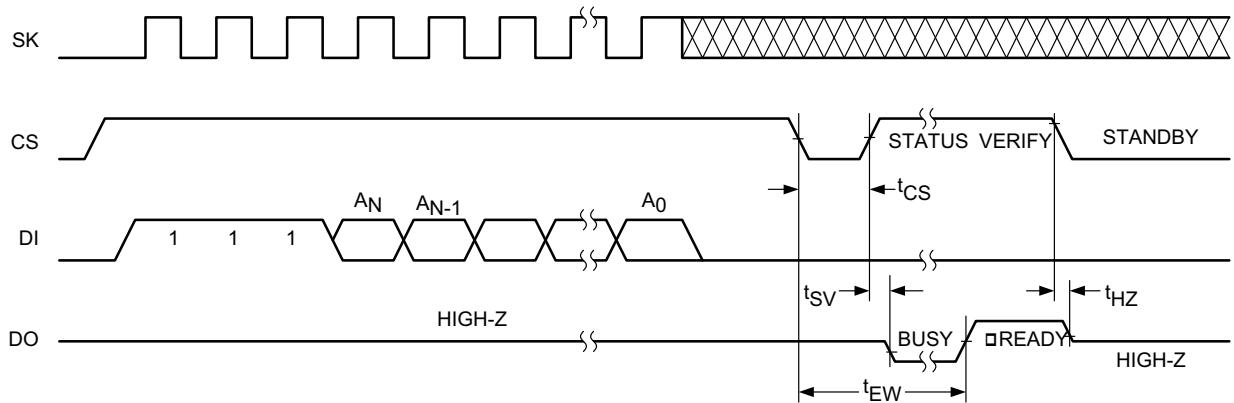


**Figure 7. Erase Instruction Timing**
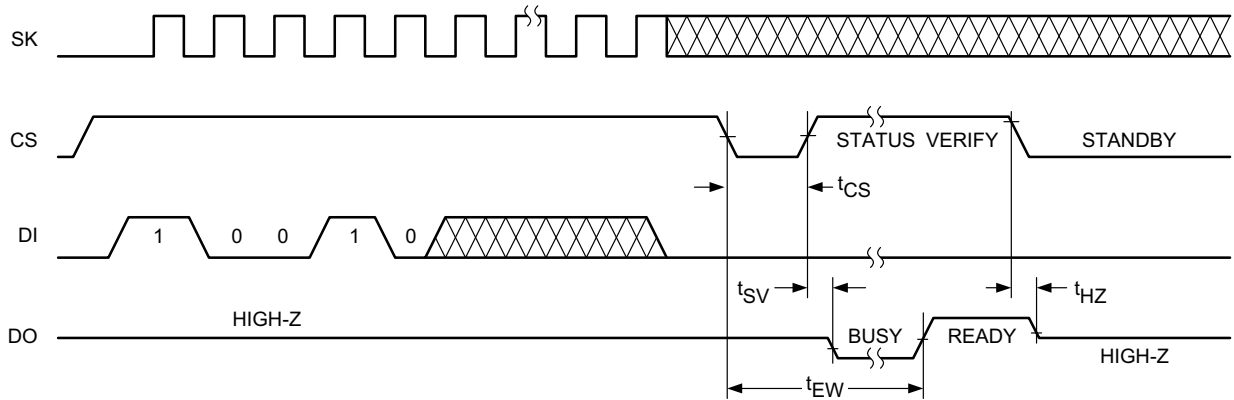


**Figure 8. ERAL Instruction Timing**

# CAT130xx

**Write All**

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of $t_{CSMIN}$ (Figure 9). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode.

The ready/busy status of the CAT130xx can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.
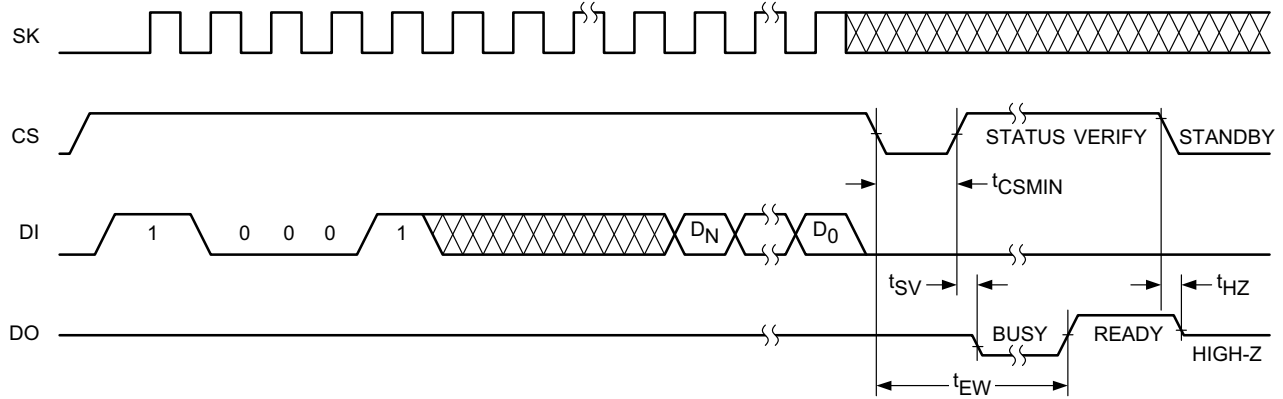


**Figure 9. WRAL Instruction Timing**

## ORDERING INFORMATION

| Orderable Part Numbers – CAT130xx Series (See Notes 1 – 5) | | | |
|---|---|---|---|
| Device | Reset Threshold Voltage | Package–Pins | Shipping |
| CAT130019SWI–GT3 | 2.85 to 3.00 V | SOIC–8 | 3000 Tape & Reel |
| CAT130019TWI–GT3 | 3.00 to 3.15 V | | |
| CAT130019SWI–G | 2.85 to 3.00 V | | 100 Tube |

1. All packages are RoHS–compliant (Lead–free, Halogen–free).
2. The standard lead finish is NiPdAu.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
4. For 8–Kb and 16–Kb embedded EEPROM option availability please contact your nearest ON Semiconductor Sales office.
5. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

# CAT130xx

## PACKAGE DIMENSIONS

**SOIC 8, 150 mils**
CASE 751BD–01
ISSUE O



**TOP VIEW**

PIN # 1
IDENTIFICATION
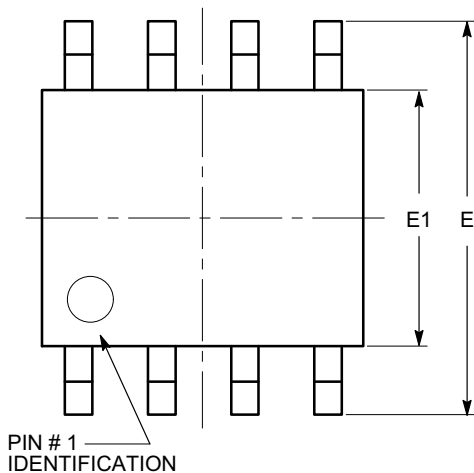
| SYMBOL | MIN | NOM | MAX |
|--------|-----|-----|-----|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0° | | 8° |
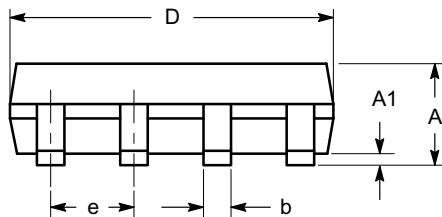


**SIDE VIEW**
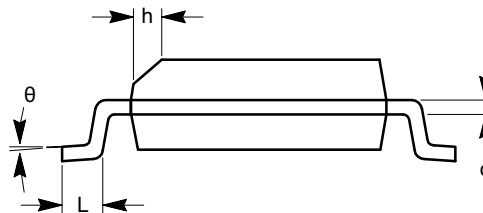


**END VIEW**

**Notes:**

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

**CAT13001/D**