Le71HR0021
Le58QL021/Le79R79
Line Module Reference Design Guide

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February 27, 2003

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ZARLINK
SEMICONDUCTOR

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CHAPTER

1 OVERVIEW

1.1 INTRODUCTION

This document describes one of the series of Zarlink line module reference designs. Each Zarlink line module is a complete standalone line card solution applicable to specific target market segments. When used with the Zarlink's VoicePath software and the VoicePath™ demo board, this module provides a complete voice solution requiring only a power supply to operate.

This line module demonstrates all of the powerful features of the Zarlink Le58QL021 QLSLAC and the Le79R79 devices. The QLSLAC device includes A-law/µ-law and linear coding. Transmit and receive gain, two-wire AC port impedance, transhybrid balance, equalization, and hybrid balance. The Le79R79 SLIC device provides internal ring generation and ring trip detection, battery switching, programmable open circuit voltage, and a programmable loop detect threshold. Together, these devices form a complete line card solution.

1.2 SCOPE

This document describes the Le71HR0021 line module only. For information regarding the VoicePath software, the WinSLAC™ software, or the VP demo board please see their respective user's guides.

1.3 REFERENCES

The following documents are referred to in this document and may be helpful.

- *Le79R79 Data Sheet*, document ID# 080125
- *Le58QL021 Data Sheet*, document ID# 080753
- *Le79R79 Ringing SLIC Device User's Guide*, document ID# 080194
- *VoicePath Demo Board User's Guide*, document ID# 080756
- *Mini-PBX Demo Application User's Guide*, document ID# 080722

CHAPTER

2 LINE MODULE DESCRIPTION

2.1 OVERVIEW

This chapter describes the features of the Le71HR0021 line module.

2.2 INTERFACE CONNECTORS

Zarlink line modules have three connectors to interface the QLSLAC device and SLIC devices to a customer's main board or the Zarlink's VP demo board. These connectors are mounted on the bottom of the Line Module PCB. In this implementation, the larger connector (J3) interfaces the Tip and Ring leads of each line to the VP demo board. This connector also provides a means of supplying external battery supplies to the line module SLIC devices. To use external batteries, it is necessary to break off the on board DC-DC converter so that contention does not occur.

The two smaller connectors are used to interface the low-level digital signals and the low voltage power sources to the Line Module (+3.3 V, +5 V, and +12 V). These are deliberately spaced apart from the SLIC device area where higher voltages and lightning surges are possible. The MPI and power connector (J2) provide connections for the control interface (MPI Bus) and the 3.3 VDC power to the QLSLAC device, and the +12 V for an on-board switching power supply.

The PCM and power connector (J1) provides the interface to the PCM highway, and the master clock for the QLSLAC device. In addition, the SLIC device 5-V VCC supply enters the line module through this connector. The MPI and PCM signals are split on separate connectors deliberately. The PCM connector has extra ground connections to isolate critical clock signals on the connector.

2.3 ON BOARD POWER CONVERTER

The on board DC-DC power converter is used to create the required SLIC device battery voltages. In the case of the Le79R79 device, two battery voltages are required. On this line module, a –63 V, and a –21 V supply are created with the on board DC-DC converter. These voltages were chosen so that the On-Hook Tip/Ring voltage would not exceed the UL1950 requirement of 56 V. The on board converter is capable of delivering up to approximately 9 W total to the SLIC devices. This provides enough power to ring 5 REN at 0 loop length on all four lines simultaneously.

2.4 LINE INTERFACE CIRCUITS

The line interface circuit consists of a fuse for each of Tip and Ring, a sidactor for shunting over-voltages on Tip and Ring to ground, and 50-Ω current limiting fuse resistors. See Chapter 3 *Surge Protection*, on page 7 for more information regarding the line protection circuits.

2.5 TRANSMISSION

2.5.1 Two-Wire Impedance

The QLSLAC device can modify the two-wire "desired" port impedance (Z_D) by programming the AISN and the Z-filter of the SLAC device and/or by changing the Line impedance setting resistor RTX. All complex impedance subscriber line terminations such as those found in China, Europe, Middle East, Africa, South America and North America can be achieved. The achievable two-wire return loss for these terminations is higher than any country's required value for subscriber lines. The Zarlink VoicePath Mini-PBX application provides a 600-Ω resistive, 900-Ω resistive, and German Complex impedance for demonstration purposes. Other line impedances can be supported in the Mini-PBX application by downloading the WinSLAC coefficient file generated by the WinSLAC coefficient generation software. For more information on downloading custom coefficient files see the Mini-PBX User's Guide. For this line module the two-wire impedance is nominally set to be 600 Ω.

2.5.2 Four-Wire Return Loss or Transhybrid Balance Impedance

The QLSLAC device can modify the four-wire port balance or line impedance (Z_L) by programming the B-filter. All of the complex balance impedance for subscriber lines from areas like China, Europe, Middle East, Africa, South America and North America can be achieved with no hardware changes. The achievable four-wire return loss for these terminations is higher than any country's required value for subscriber lines. The Zarlink VoicePath Mini-PBX software provides a 600-Ω resistive, 900-Ω resistive, and German Complex impedance for demonstration purposes. Other line impedances can be supported in the Mini-PBX application by downloading the WinSLAC coefficient file generated by the WinSLAC coefficient generation software. For more information on downloading custom coefficient files see the Mini-PBX User's Guide.

2.5.3 Equalization

The QLSLAC device is capable of applying equalization to either the transmit direction (into the PSTN) or the receive direction (from the PSTN). The equalization can provide compensation for attenuation distortion caused by the line. The equalization for attenuation distortion caused by complex two-wire port impedance is automatically done in the Zarlink WinSLAC software. Other equalization can be applied with the WinSLAC software if special needs exist. See the *WinSLAC User's Guide* for information on the WinSLAC Software.

2.5.4 Transmit Gain (AX/GX)

The transmit gain of the SLIC/SLAC device system is determined by the two-to-four-wire gain through the SLIC device (G_{24}) and the gain of the QLSLAC device in the transmit direction. For the Le79R79 device, G_{24} is equal to –6.02 dB and the QLSLAC transmit gain can be adjusted from 0 dB to +18 dB. It is important to point out that with the QLSLAC transmit gain set to unity, a 0.5 VRMS signal presented to its analog input will produce a 0 dBm0 on the PCM highway (A-Law). When using the QSLAC device, or if the internal attenuator of the QLSLAC device is enabled a 0.775 VRMS signal at the analog input will produce a 0 dBm0 signal on the PCM highway. As an example, suppose a system gain of 0 dB is desired and that the SLIC device presents a 600-Ω termination to the line. This implies that a 0 dBm signal on the two wire side of the SLIC device will have a voltage of 0.775 VRMS. Since the voltage gain through the SLIC device is -6.02 dB, the voltage presented to the SLAC device's analog input will be 0.388 VRMS. This voltage will give a -6 dBm0 signal on the PCM highway if the internal attenuator is enabled. Therefore it is necessary to set the QLSLAC device gain to +6 dB to achieve the desired 0 dBm0 signal on the PCM highway. The system transmit gain is set in the WinSLAC program. For more information on setting the transmit gain, please refer to the *Le79R79 Ringing SLIC User's Guide* and the *QLSLAC Data Sheet*.

2.5.5 Receive Gain (AR/GR)

The system receive gain is determined by the QLSLAC device receive gain, and the four-to-two-wire gain (G_{42}) through the SLIC device. The QLSLAC device receive gain ranges from 0 dB to –18 dB. The magnitude of G_{42}, the gain through the SLIC device, is determined by the RTX and RRX resistors. For this line module, G_{42} has be set to unity when the load presented to the SLIC device is 600 Ω. It is important to note that G_{42} is a function of the load presented to the SLIC device. For more information on setting the receive gain, please refer to the *Le79R79 Ringing SLIC User's Guide* and the *QLSLAC Data Sheet*.

2.5.6 Longitudinal Balance

This reference design hardware utilizes 1% 50-Ω resistors for current limiting in the surge protection circuit. The longitudinal balance is determined by how well these resistors are matched.

2.6 SIGNALING

2.6.1 Loop Supervision

The switch hook detect is accomplished by comparing the loop resistance to a loop threshold programming resistor R_D. When the loop resistance is less than the programmed resistance set by R_D, the loop detect pin of the SLIC device is pulled Low to indicate an off-hook condition. In the Active and OHT states loop threshold resistance is set to 5.4 kΩ when operating from of low battery (V_{BAT2}) or 6.0 kΩ when operating off of high battery (VBAT1). In the Standby state the threshold

resistance is set to 3.5 kΩ These loop thresholds include 50-Ω fuse resistors and any line resistance. For more information on setting the loop detect threshold, refer to the *Le79R79 Ringing SLIC User's Guide*.

2.6.2 Ring Trip

The line module is set up for short loop ring trip detection (no DC offset) and uses AC detection of the ring trip condition. Ring trip is detected by sensing the AC resistance of the line. A threshold resistance is set using an external resistor. When the AC impedance drops below the threshold resistance, ring trip occurs. Since this line module is designed to ring a 5REN load at zero loop length, a threshold resistance of less then 1400 Ω must be selected. For this application the ring trip threshold resistance is set to approximately 650 Ω. For complete details on setting the ring trip threshold, refer to the *Le79R79 Ringing SLIC User's Guide*.

2.7 DC FEED

The DC feed curve for the Le79R79 device consists of an amplifier anti-saturation region and a constant current region. Under normal short loop conditions, the Le79R79 device generally operates as constant current source in the Off-hook state. As the loop length increases so does the loop resistance, thereby requiring a higher Tip/Ring voltage to maintain a constant current. At a given Tip/Ring threshold voltage the device switches into its anti-saturation region to prevent saturation and clipping of the amplifiers. For the Le79R79 device, this threshold voltage is set to 12.5 V when operating from V_{BAT2} (low battery) and 44 V when operating from V_{BAT1} (high battery). The anti-saturation region for the Le79R79 device looks like a voltage feed with a fairly high series feed resistance. For this application, the feed resistance in the anti-saturation region is about 168 Ω.

2.7.1 Loop Range

The loop range is determined by the apparent Tip/Ring voltage at zero loop current (V_{APP}), the line impedance, and the current requirements of the CPE equipment. The maximum loop length is achieved when running from V_{BAT1} where V_{APP} is equal to 48.2 V. For example, if we assume a 250-Ω phone, a minimum loop current of 18 mA, 26 AWG wire (24.5 ft/Ω), and two 50-Ω fuse resistors, then the line resistance (Tip + Ring) can be as high as 2159 Ω when running from the -63 V (V_{BAT1}). This is equivalent to about a 26 kft loop. Ringing, of course, will not accommodate out to this distance. When running from the –21 V supply (V_{BAT2}) this feed range drops to about 5 kft. Note that fully serviceable loop length is dictated by the ringing range. See below for a discussion of the ringing range.

2.7.2 Loop Current Range

The loop current of this design is limited to 25 mA.

2.7.3 Power Supplies

The most negative power supply for this design was selected such that the UL1950 requirements for the maximum voltage of an open circuit loop would be met. This specification requires that no open circuit voltage greater than 56.5 V shall be present. This requirement does not apply during ringing. In the Le79R79 device, the magnitude of the open circuit voltage at tip and ring is between 8 V and 10 V less than the magnitude of V_{BAT1} when in the Standby state. To meet the UL1950 specification V_{BAT1} was chosen to be 63 V, thus giving an open circuit voltage of about 55 V. The topology of the power supply used on this reference design dictated that V_{BAT2} be 1/3 of V_{BAT1} or 21 V.

2.7.4 Ringing Range

The ringing range is set by five factors: the number of Ringer Equivalences desired to ring per line, the ringing waveform, the available battery voltage, the required ringing voltage presented to the ringer, and the ring source series resistance. REN, or Ringer Equivalence Number, is a measure of ringer load or how many standard electro-mechanical ringers can be rung. One REN is generally thought to be about 6800 Ω at a 20-Hz ringer frequency. The required ringer voltage should be about 40 VRMS at the CPE.

This design uses trapezoidal ringing waveform with a crest factor (CF) equal to 1.21, and a ring source series resistance of 187 Ω. The Le79R79 device generates a ringing voltage equal to

(V_{BAT1} – 2.5) VPK or approximately 50 VRMS when V_{BAT1} is set to 63 V and the crest factor is set to 1.21. For this design, 5 REN can be rung at 0 loop and 2.5 REN can be rung out to approximately 3.9 kft. The design's loop range is limited by the ringing capability.

CHAPTER

3 SURGE PROTECTION

3.1 CURRENT AND VOLTAGE LIMITING

This line module design has series current limiting and shunt voltage limiting for lightning and surge protection. The protection design utilizes a Teccor F1250T fuse device in series with 50-Ω fuse resistors on tip and ring to limit surge current.

Voltage limiting in the line circuit is provided by a Teccor PO641SC Sidactor. This device is a solid state crowbar device that is designed to protect the line circuit during dangerous transient conditions. These devices are triggered upon application of a voltage that exceeds its triggering voltage. For the PO641SC, a voltage greater than 58 V will trigger the device. Once the device has been triggered, it will appear as a short circuit to ground until a minimum holding current is reached. When this holding current is reached the device will reset and return to its transparent open circuit state. In the triggered state, the voltage across it will not exceed 5 V. These devices also contain an integrated diode that will clamp any positive going voltages presented on tip or ring. There are two devices used for each line circuit, one for the tip and one for ring. Current limiting into the tip and ring leads of the Le79R79 device is accomplished by the 50-Ω series resistors.

CHAPTER

4 LINE CIRCUIT IDENTIFICATION MEMORY

4.1 ID EEPROM

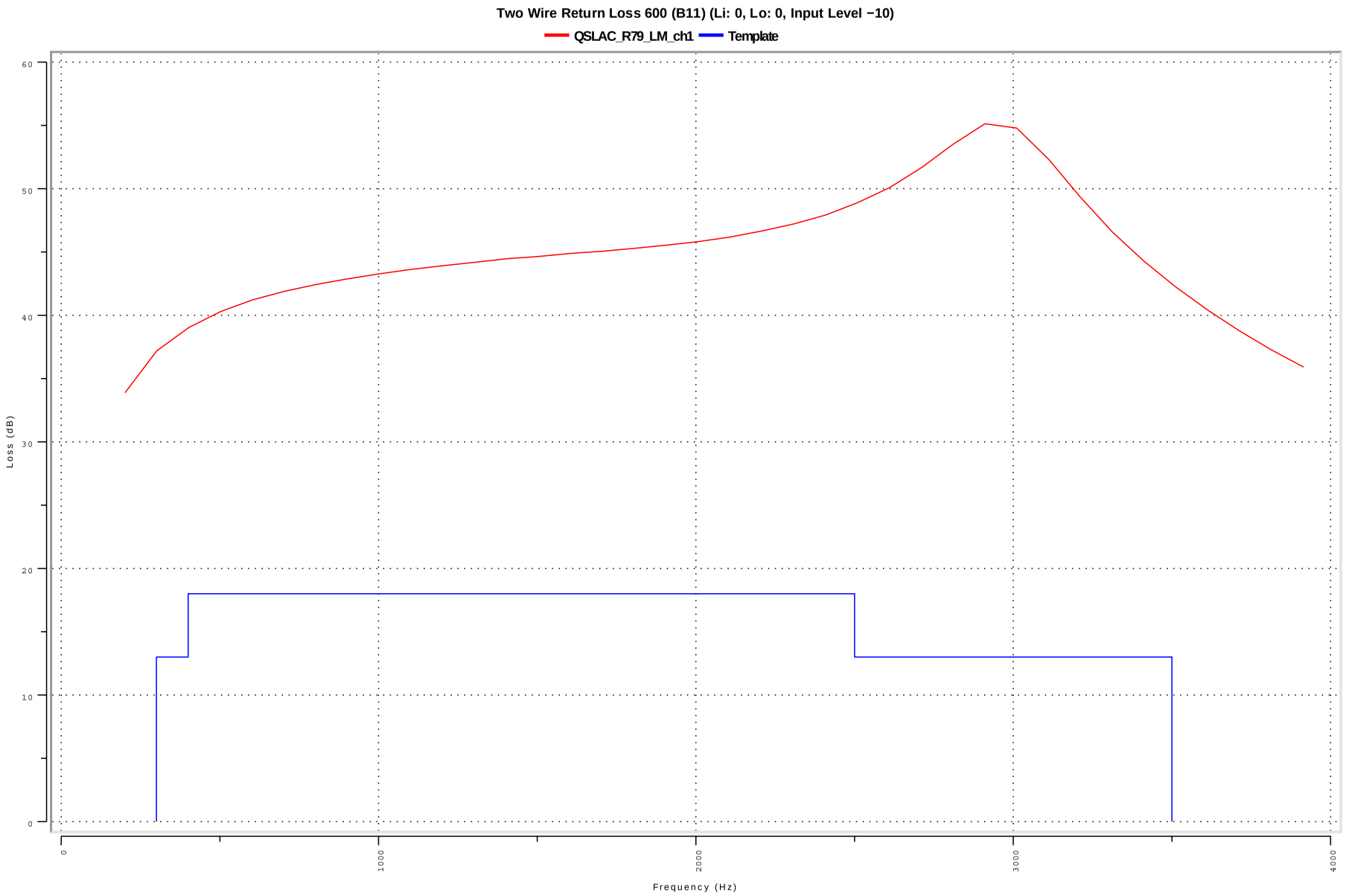
The line module has a Dallas Semiconductor DS2433 EEPROM on the PCB. This is a 4 kbit one-wire EEPROM memory which, while not crucial to module operation, is essential to the demonstration system. This memory is factory loaded with a line module design identification, a serial number, and various control coefficient sets. These coefficient sets provide the user with differing AC transmission characteristics for this market segment. Of course a user is not limited to these coefficient sets. Zarlink provides a tool chain to enable the line module user to program their own desired coefficient set. The line module user can remove the ID EEPROM from their custom design by using their own coefficients contained in their own software code. This ID EEPROM might be replaced by a smaller EEPROM in the user design. This could contain the recommended or required Telecordia "CLEI" code information.

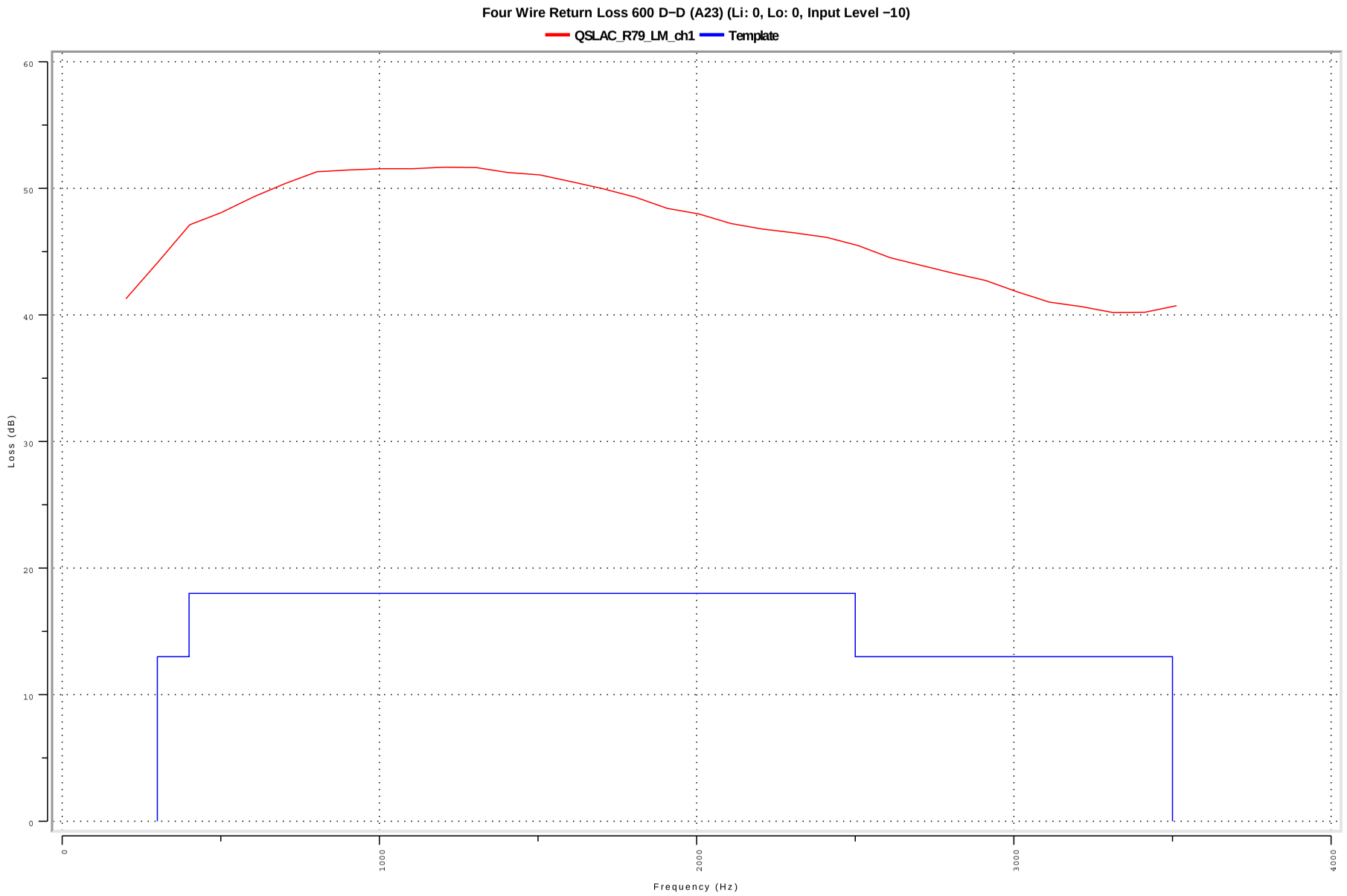
CHAPTER

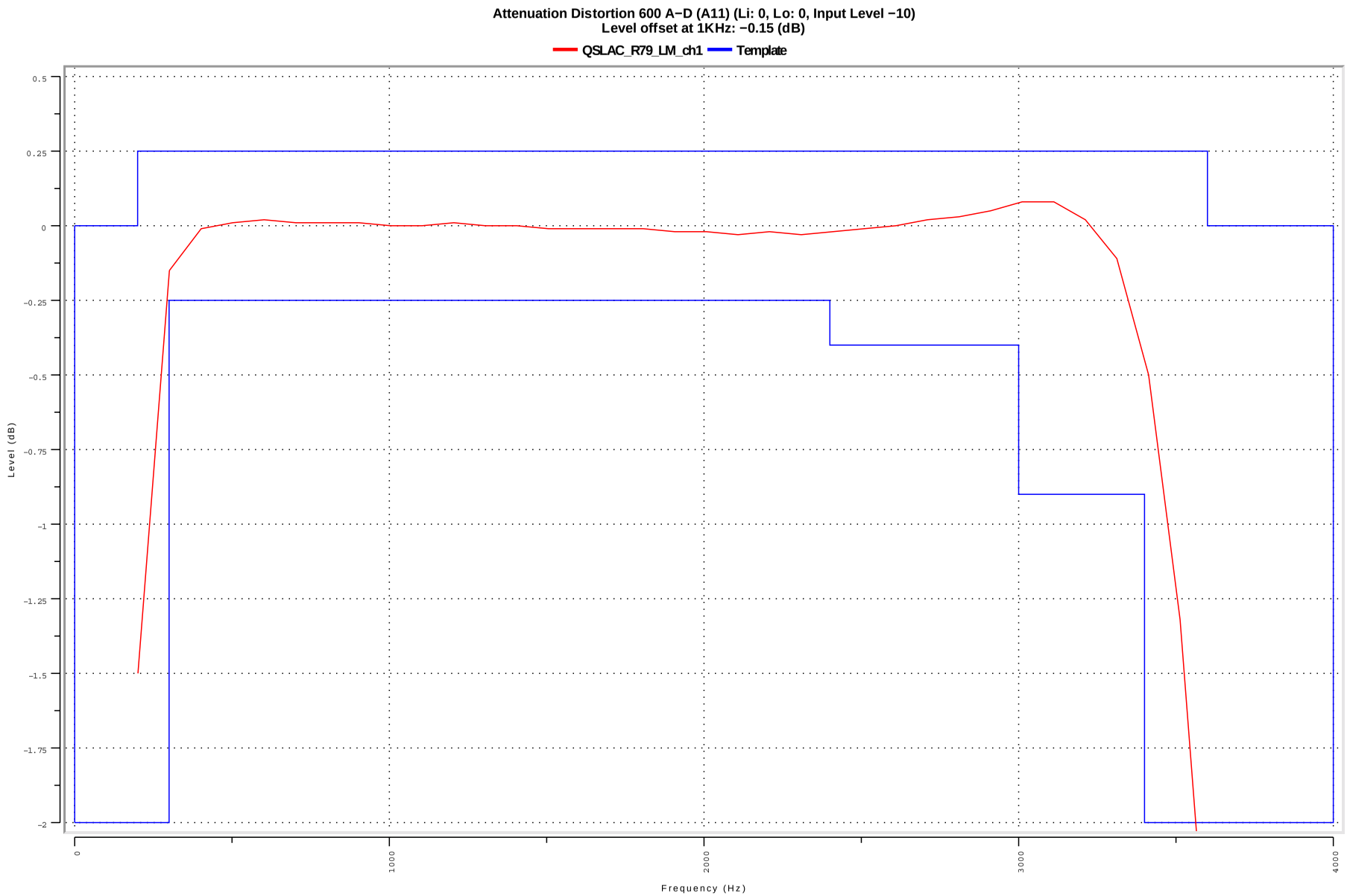
5 LINE MODULE PERFORMANCE DATA

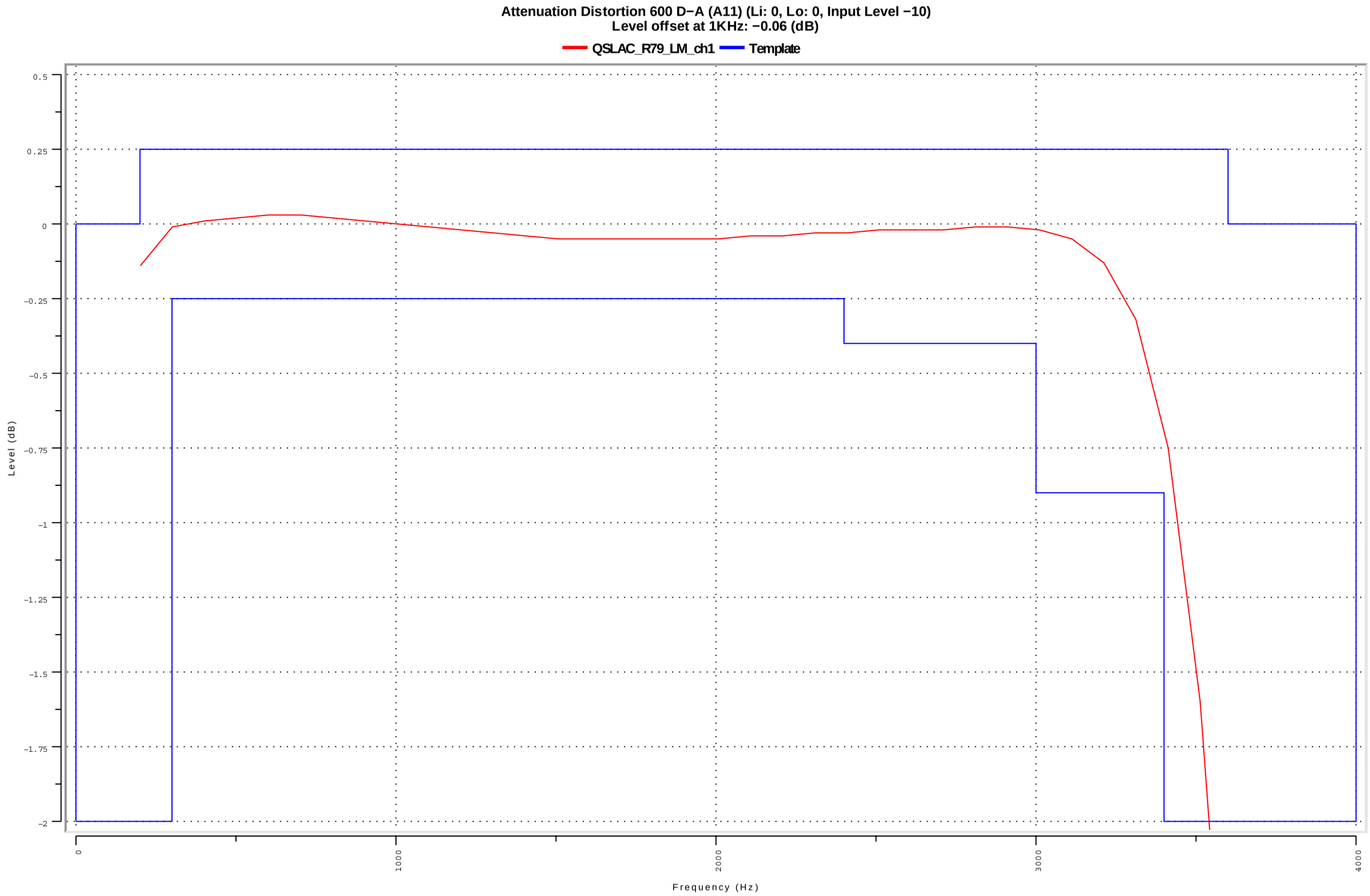
5.1 PERFORMANCE DATA GRAPHS

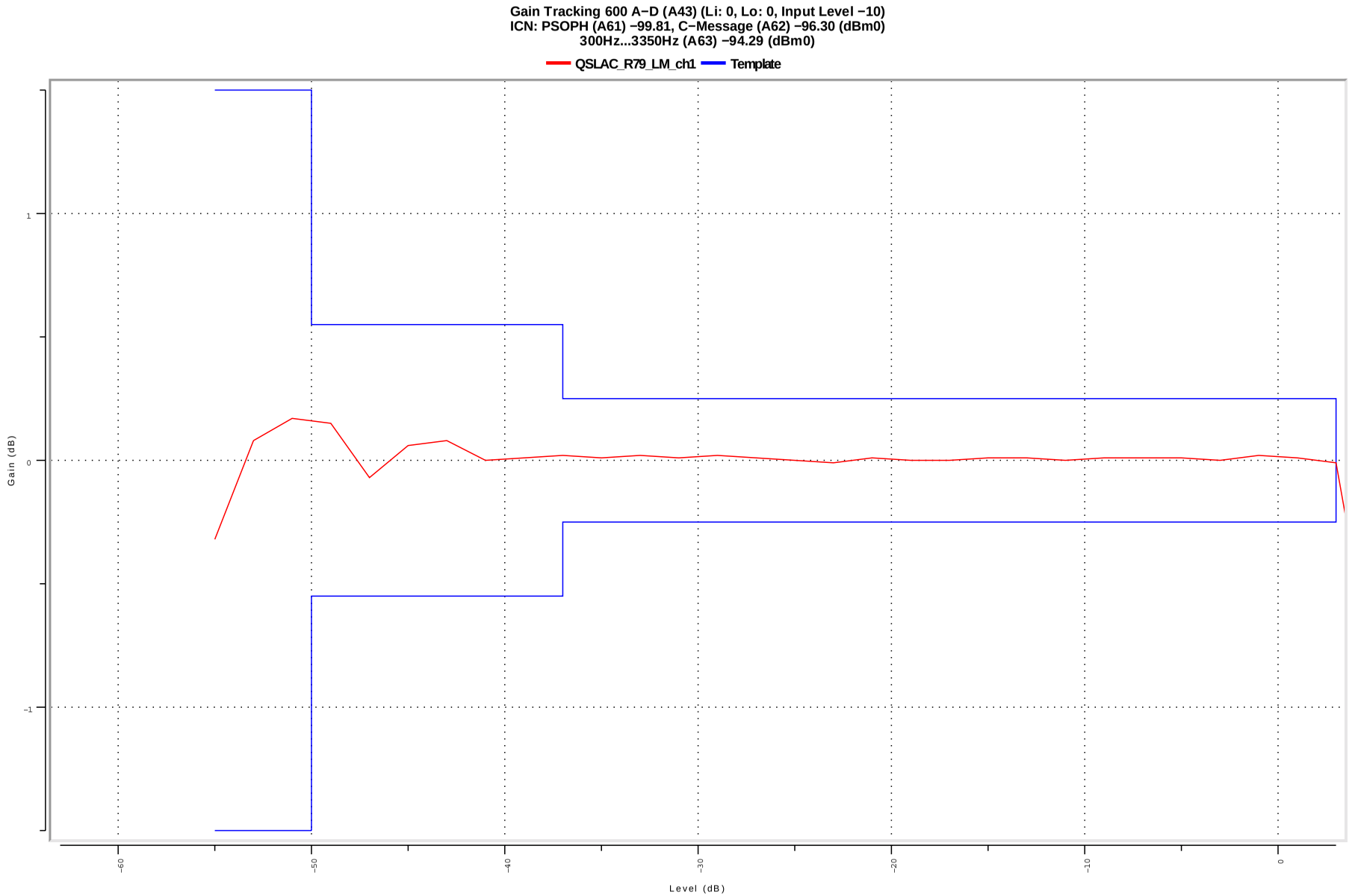
The graphs on the following pages provide typical performance data for this line module.

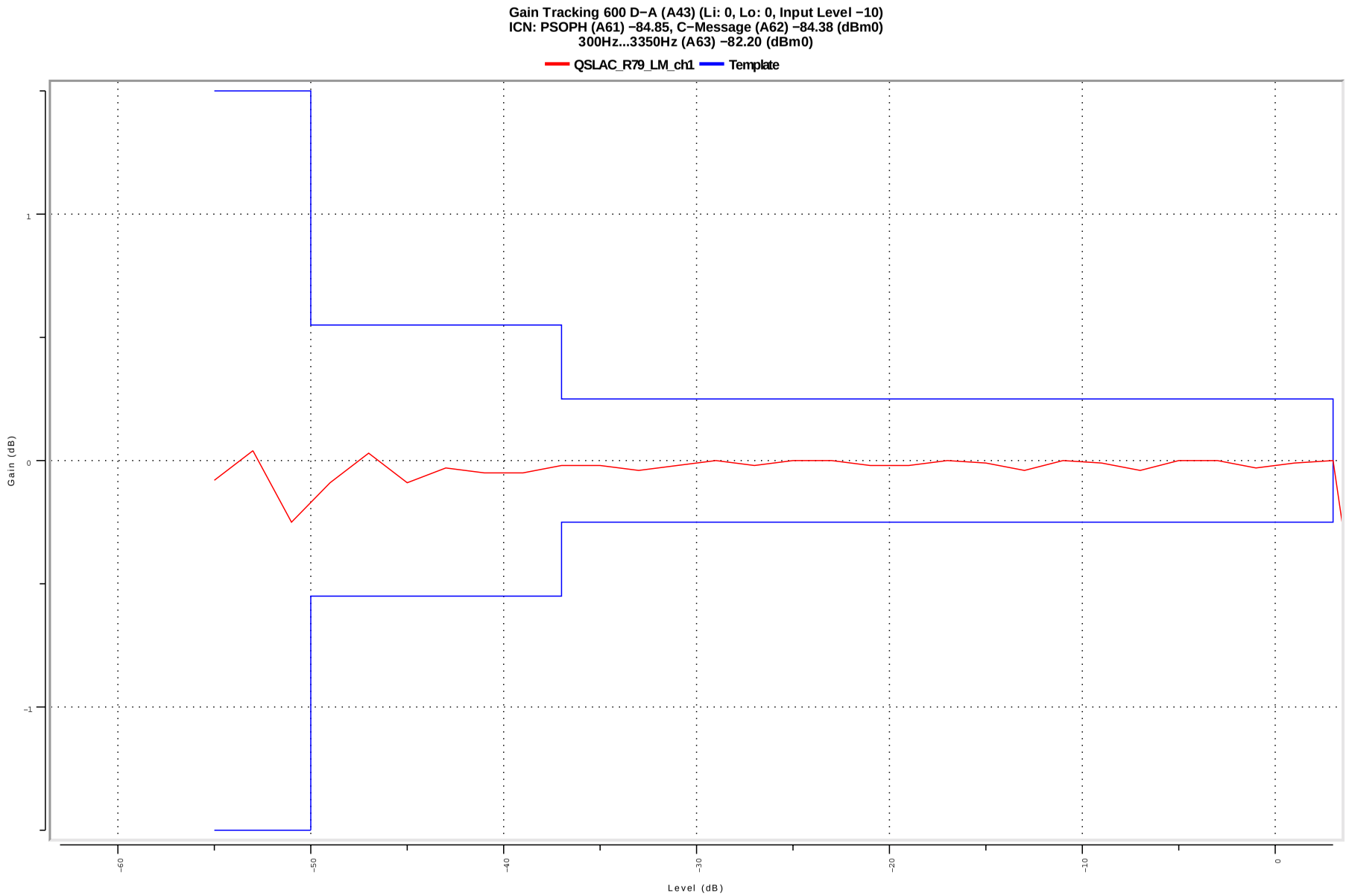

Two Wire Return Loss 600 (B11) (Li: 0, Lo: 0, Input Level −10)
QSLAC_R79_LM_ch1
Template
Loss (dB)
60
50
40
30
20
10
0
0
1000
2000
3000
4000
Frequency (Hz)

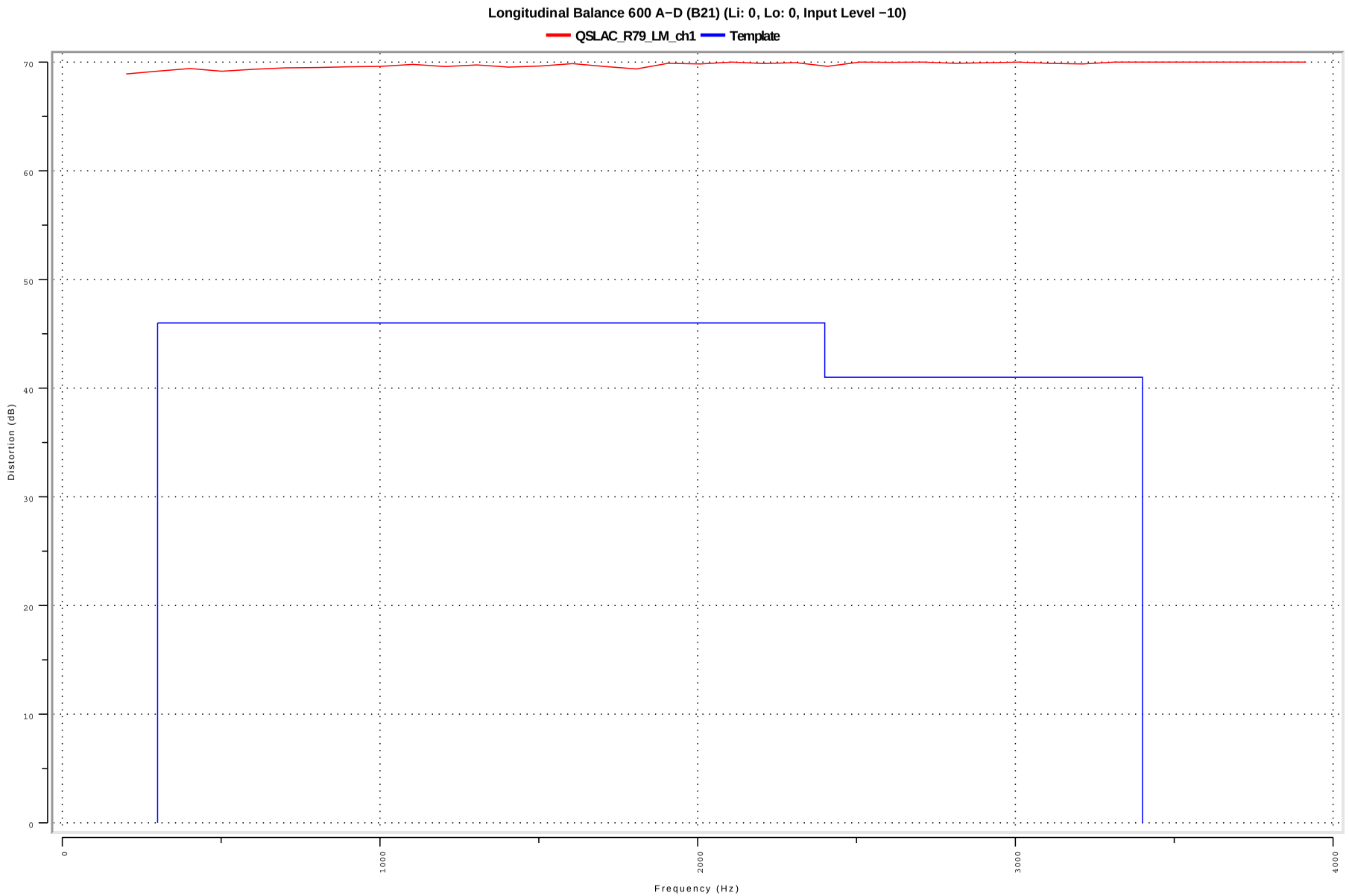

Four Wire Return Loss 600 D−D (A23) (Li: 0, Lo: 0, Input Level −10)
QSLAC_R79_LM_ch1
Template
Loss (dB)
60
50
40
30
20
10
0
0
1000
2000
3000
4000
Frequency (Hz)

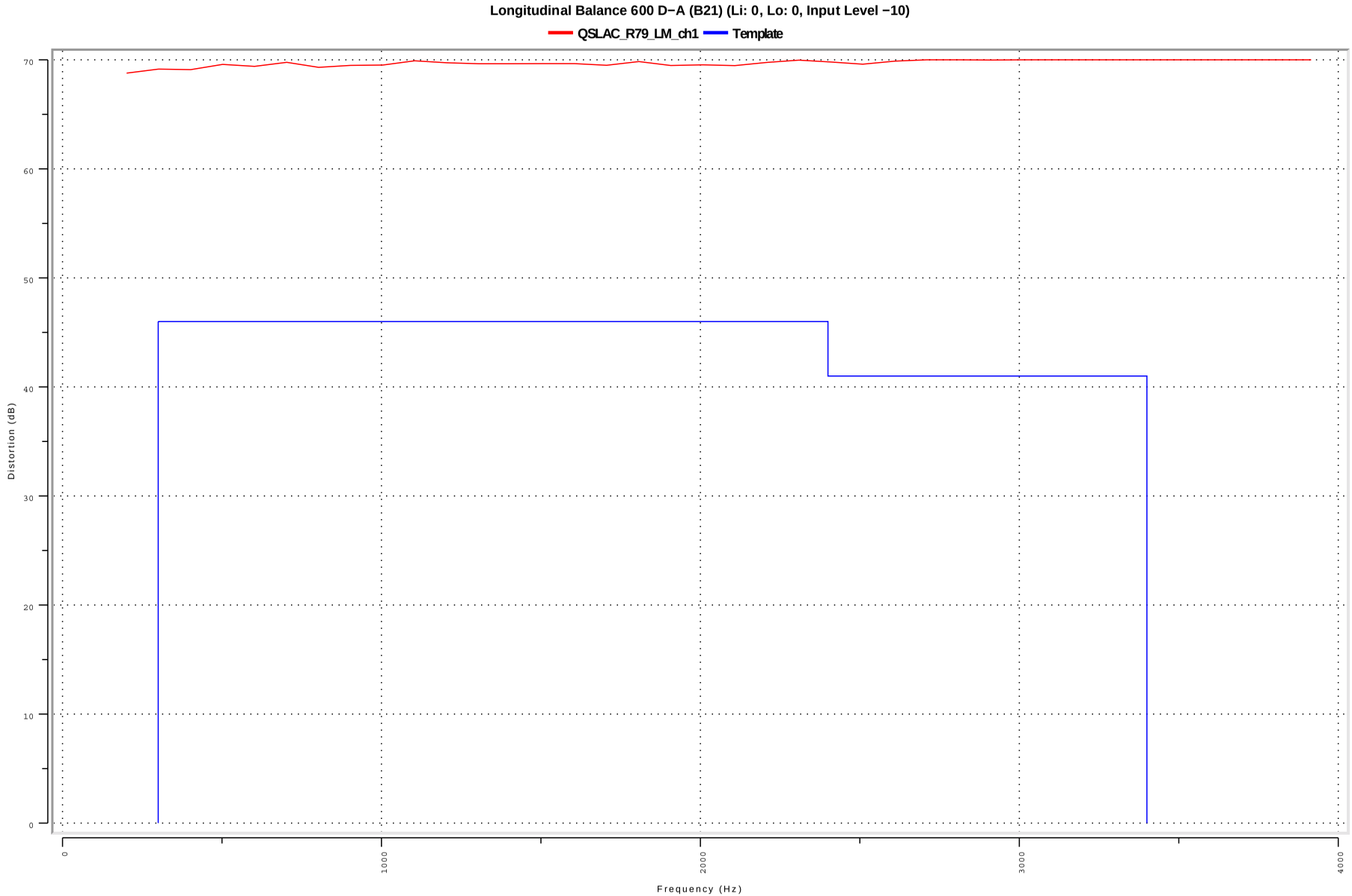

Attenuation Distortion 600 A−D (A11) (Li: 0, Lo: 0, Input Level −10)
Level offset at 1KHz: −0.15 (dB)
QSLAC_R79_LM_ch1
Template
0.5
0.25
0
−0.25
−0.5
−0.75
−1
−1.25
−1.5
−1.75
−2
Level (dB)
0
1000
2000
3000
4000
Frequency (Hz)

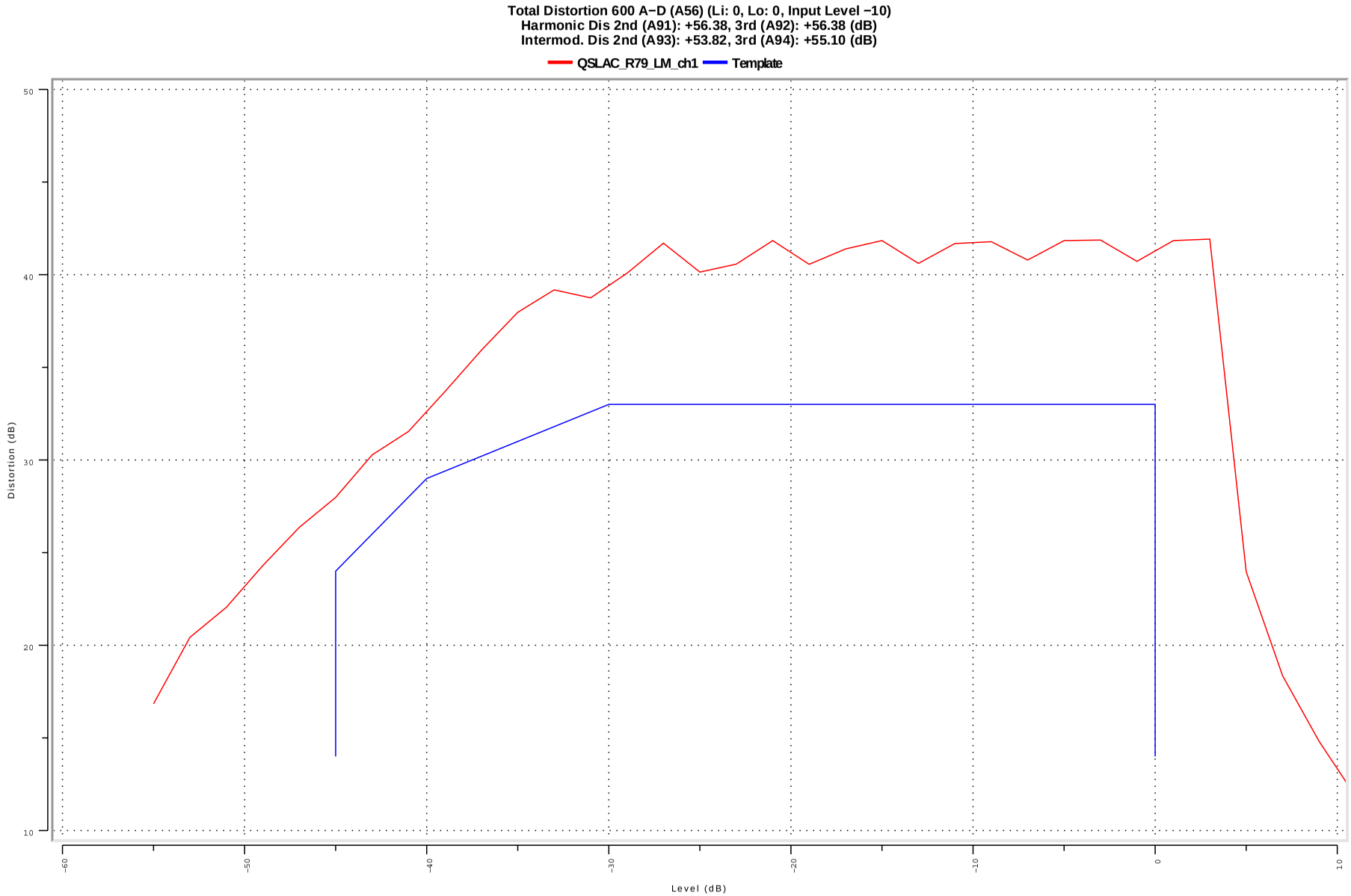

Attenuation Distortion 600 D−A (A11) (Li: 0, Lo: 0, Input Level −10)
Level offset at 1KHz: −0.06 (dB)
QSLAC_R79_LM_ch1
Template
0.5
0.25
0
−0.25
−0.5
−0.75
−1
−1.25
−1.5
−1.75
−2
Level (dB)
0
1000
2000
3000
4000
Frequency (Hz)

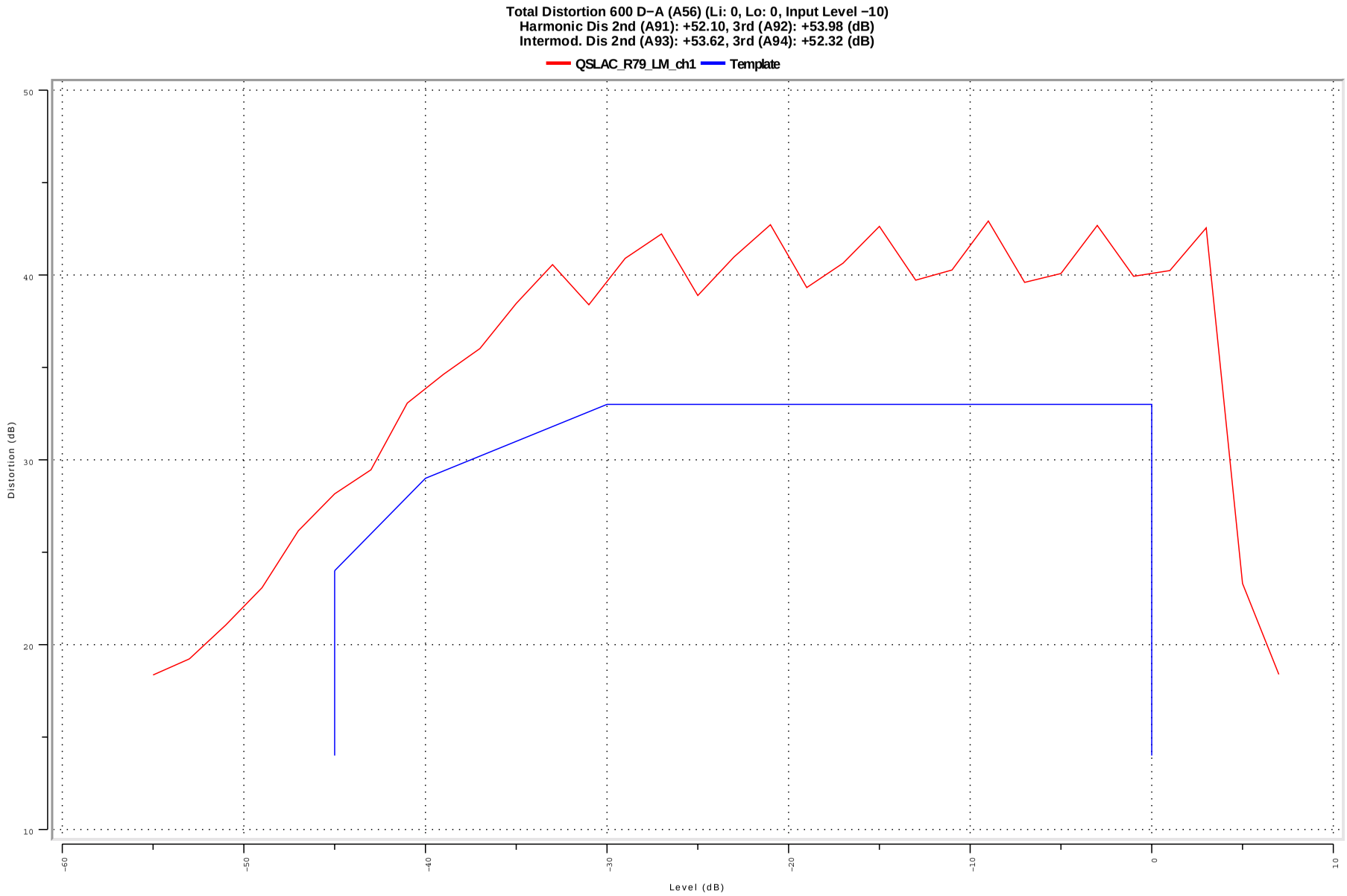

Gain Tracking 600 A−D (A43) (Li: 0, Lo: 0, Input Level −10)
ICN: PSOPH (A61) −99.81, C−Message (A62) −96.30 (dBm0)
300Hz...3350Hz (A63) −94.29 (dBm0)
QSLAC_R79_LM_ch1
Template
Gain (dB)
1
0
−1
−60
−50
−40
−30
−20
−10
0
Level (dB)


Gain Tracking 600 D−A (A43) (Li: 0, Lo: 0, Input Level −10)
ICN: PSOPH (A61) −84.85, C−Message (A62) −84.38 (dBm0)
300Hz...3350Hz (A63) −82.20 (dBm0)
QSLAC_R79_LM_ch1
Template
Gain (dB)
1
0
−1
−60
−50
−40
−30
−20
−10
0
Level (dB)


Longitudinal Balance 600 A−D (B21) (Li: 0, Lo: 0, Input Level −10)
QSLAC_R79_LM_ch1
Template
Distortion (dB)
70
60
50
40
30
20
10
0
0
1000
2000
3000
4000
Frequency (Hz)


Longitudinal Balance 600 D−A (B21) (Li: 0, Lo: 0, Input Level −10)
QSLAC_R79_LM_ch1
Template
Distortion (dB)
70
60
50
40
30
20
10
0
0
1000
2000
3000
4000
Frequency (Hz)


Total Distortion 600 A−D (A56) (Li: 0, Lo: 0, Input Level −10)
Harmonic Dis 2nd (A91): +56.38, 3rd (A92): +56.38 (dB)
Intermod. Dis 2nd (A93): +53.82, 3rd (A94): +55.10 (dB)
QSLAC_R79_LM_ch1
Template
Distortion (dB)
50
40
30
20
10
−60
−50
−40
−30
−20
−10
0
10
Level (dB)


Total Distortion 600 D−A (A56) (Li: 0, Lo: 0, Input Level −10)
Harmonic Dis 2nd (A91): +52.10, 3rd (A92): +53.98 (dB)
Intermod. Dis 2nd (A93): +53.62, 3rd (A94): +52.32 (dB)
QSLAC_R79_LM_ch1
Template
Distortion (dB)
50
40
30
20
10
−60
−50
−40
−30
−20
−10
0
10
Level (dB)

CHAPTER

6 LINE MODULE SCHEMATICS AND BILL OF MATERIALS

6.1 SCHEMATICS

See the Le71HR0021 line module schematics on the following attached pages.

Zarlink's Four Channel xDSL Reference Design

UL1950 Compliant and GR1089 Lightning Compliant

Loop current set to 25 mA
Loop resistance optimized for 600 ohm

Title	Zarlink 79Q021 / 79R79 Reference Design	
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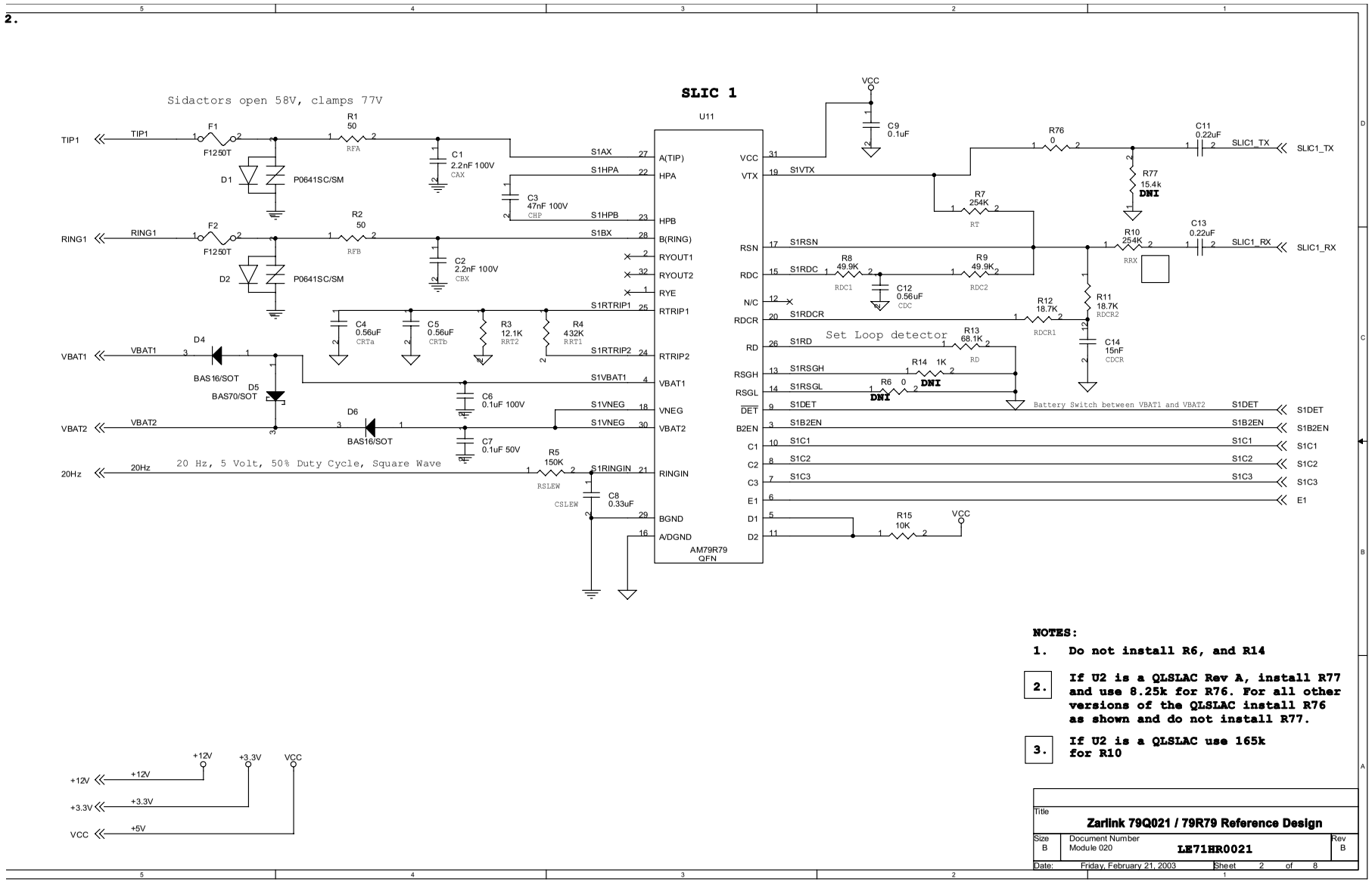
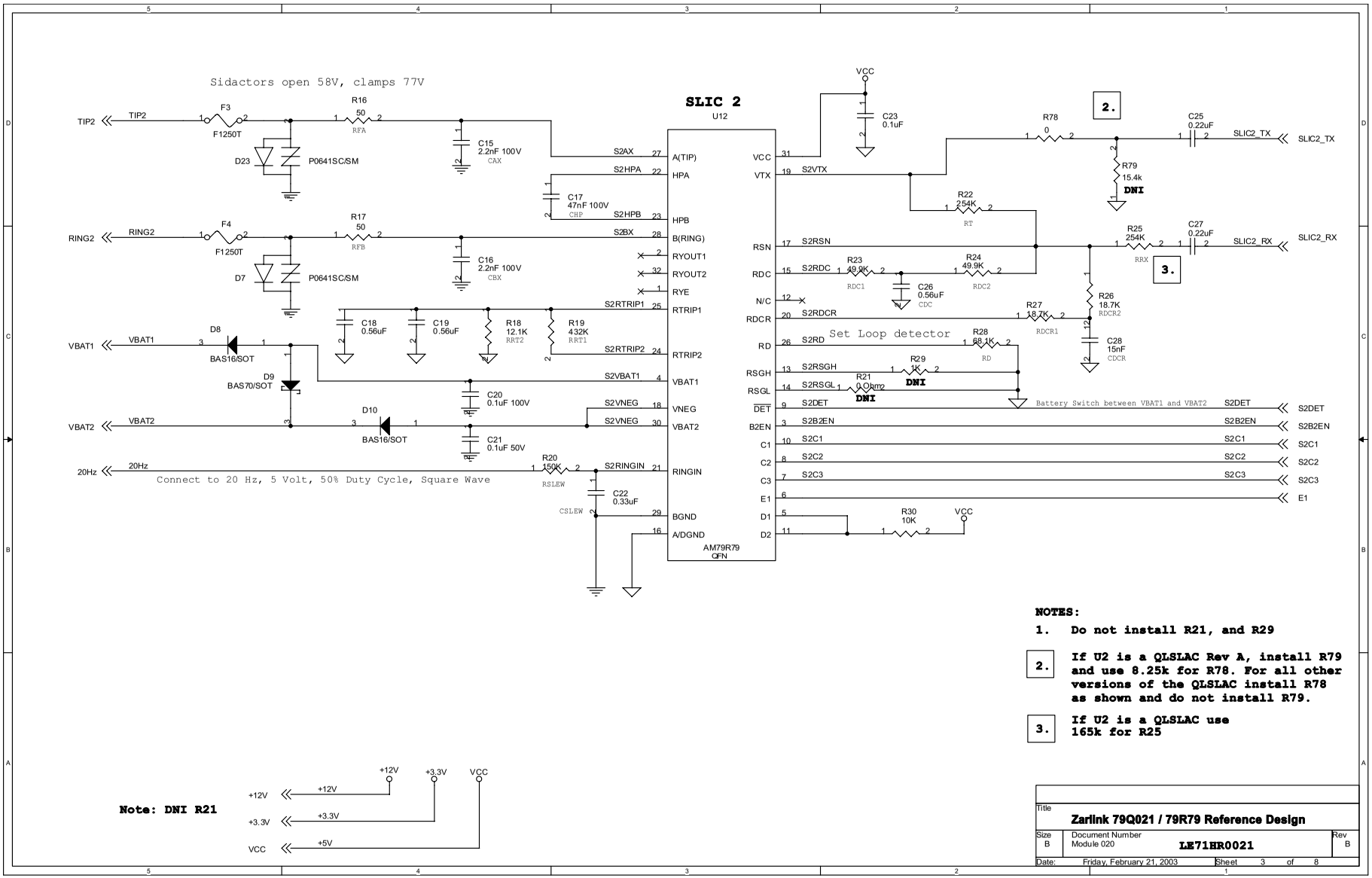
2.


SLIC 1
U11
Sidactors open 58V, clamps 77V
20 Hz, 5 Volt, 50% Duty Cycle, Square Wave
Set Loop detector
Battery Switch between VBAT1 and VBAT2
AM79R79
QFN
NOTES:
1. Do not install R6, and R14
2. If U2 is a QLSLAC Rev A, install R77 and use 8.25k for R76. For all other versions of the QLSLAC install R76 as shown and do not install R77.
3. If U2 is a QLSLAC use 165k for R10
Zarlink 79Q021 / 79R79 Reference Design
LE71HR0021
Friday, February 21, 2003


Sidactors open 58V, clamps 77V
SLIC 2
U12
AM79R79
QFN
Set Loop detector
Battery Switch between VBAT1 and VBAT2
Connect to 20 Hz, 5 Volt, 50% Duty Cycle, Square Wave
NOTES:
1. Do not install R21, and R29
2. If U2 is a QLSLAC Rev A, install R79 and use 8.25k for R78. For all other versions of the QLSLAC install R78 as shown and do not install R79.
3. If U2 is a QLSLAC use 165k for R25
Note: DNI R21
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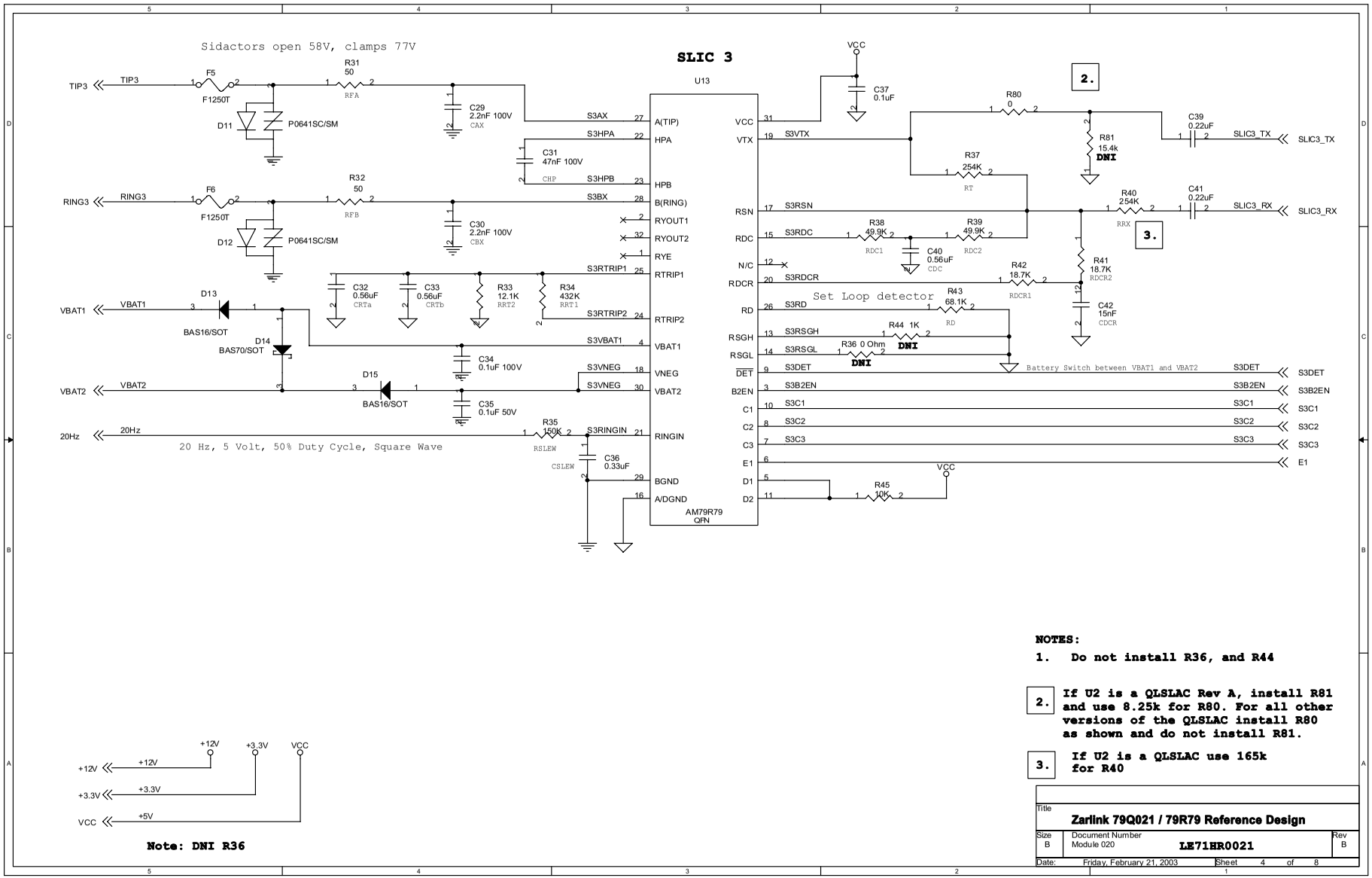
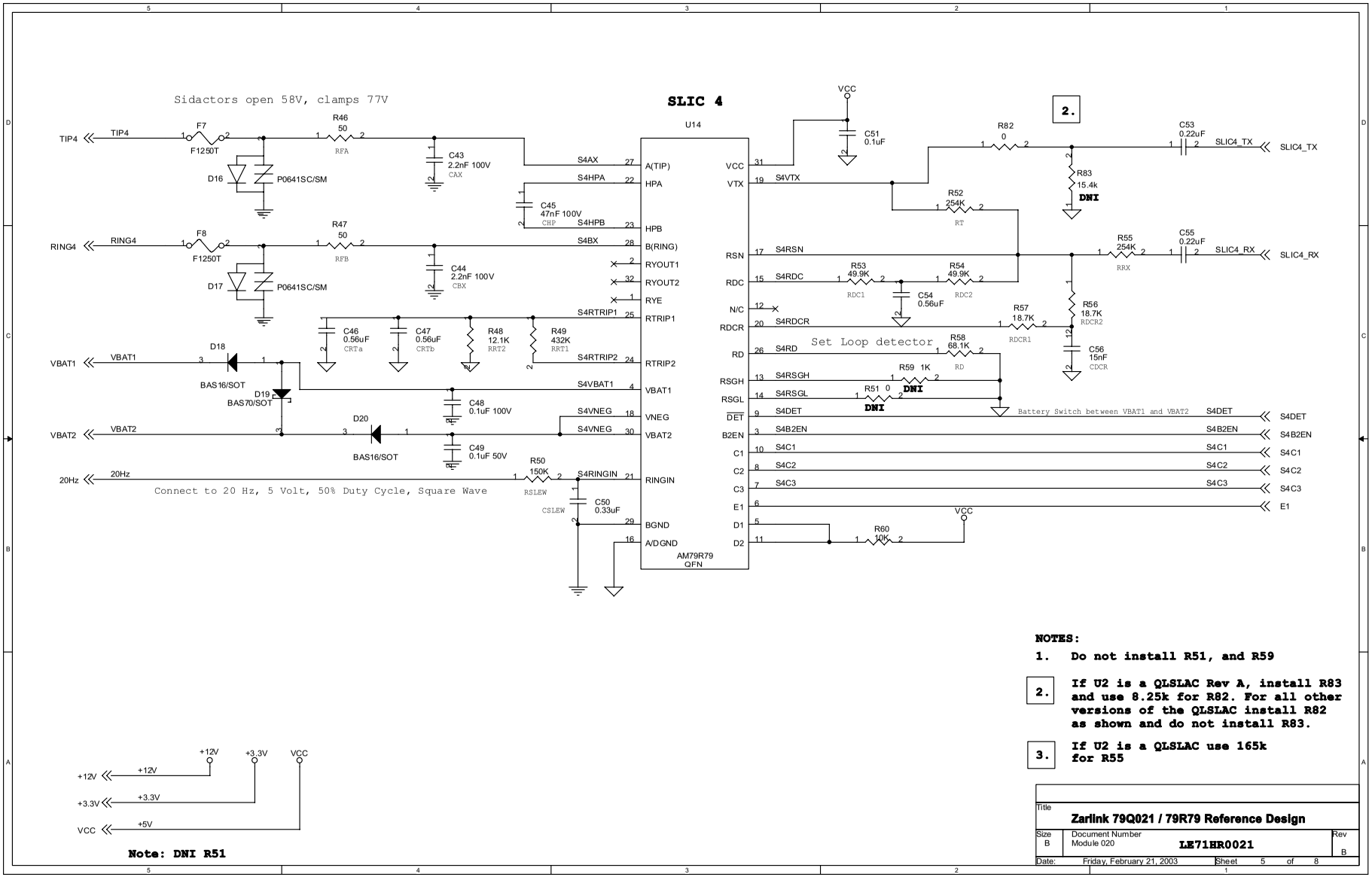

Sidactors open 58V, clamps 77V
SLIC 3
U13
AM79R79
QFN
Set Loop detector
Battery Switch between VBAT1 and VBAT2
20 Hz, 5 Volt, 50% Duty Cycle, Square Wave
Note: DNI R36
NOTES:
1. Do not install R36, and R44
2. If U2 is a QLSLAC Rev A, install R81 and use 8.25k for R80. For all other versions of the QLSLAC install R80 as shown and do not install R81.
3. If U2 is a QLSLAC use 165k for R40
Zarlink 79Q021 / 79R79 Reference Design
Document Number
Module 020
LE71HR0021
Friday, February 21, 2003


SLIC 4
U14
Sidactors open 58V, clamps 77V
TIP4
RING4
VBAT1
VBAT2
20Hz
F7
F8
F1250T
R46
R47
50
RFA
RFB
D16
D17
P0641SC/SM
C43
2.2nF 100V
CAX
C44
CBX
C45
47nF 100V
CHP
D18
BAS16/SOT
D19
BAS70/SOT
D20
C46
0.56uF
CRTa
C47
CRTb
R48
12.1K
RRT2
R49
432K
RRT1
C48
0.1uF 100V
C49
0.1uF 50V
R50
150K
RSLEW
C50
0.33uF
CSLEW
Connect to 20 Hz, 5 Volt, 50% Duty Cycle, Square Wave
S4AX
S4HPA
S4HPB
S4BX
S4RTRIP1
S4RTRIP2
S4VBAT1
S4VNEG
S4VNEG
S4RINGIN
A(TIP)
HPA
HPB
B(RING)
RYOUT1
RYOUT2
RYE
RTRIP1
RTRIP2
VBAT1
VNEG
VBAT2
RINGIN
BGND
A/DGND
AM79R79
QFN
VCC
C51
0.1uF
S4VTX
S4RSN
S4RDC
S4RDCR
S4RD
S4RSGH
S4RSGL
S4DET
S4B2EN
S4C1
S4C2
S4C3
VTX
RSN
RDC
N/C
RDCR
RD
RSGH
RSGL
DET
B2EN
C1
C2
C3
E1
D1
D2
R52
254K
RT
R53
49.9K
RDC1
R54
49.9K
RDC2
C54
0.56uF
R57
18.7K
RDCR1
R58
68.1K
RD
R59 1K
DNI
R51 0
DNI
R60
10K
R82
0
R83
15.4k
DNI
R55
254K
RRX
C53
0.22uF
C55
0.22uF
C56
15nF
CDCR
SLIC4_TX
SLIC4_RX
Set Loop detector
Battery Switch between VBAT1 and VBAT2
2.
+12V
+3.3V
VCC
+5V
Note: DNI R51
NOTES:
1. Do not install R51, and R59
2. If U2 is a QLSLAC Rev A, install R83 and use 8.25k for R82. For all other versions of the QLSLAC install R82 as shown and do not install R83.
3. If U2 is a QLSLAC use 165k for R55
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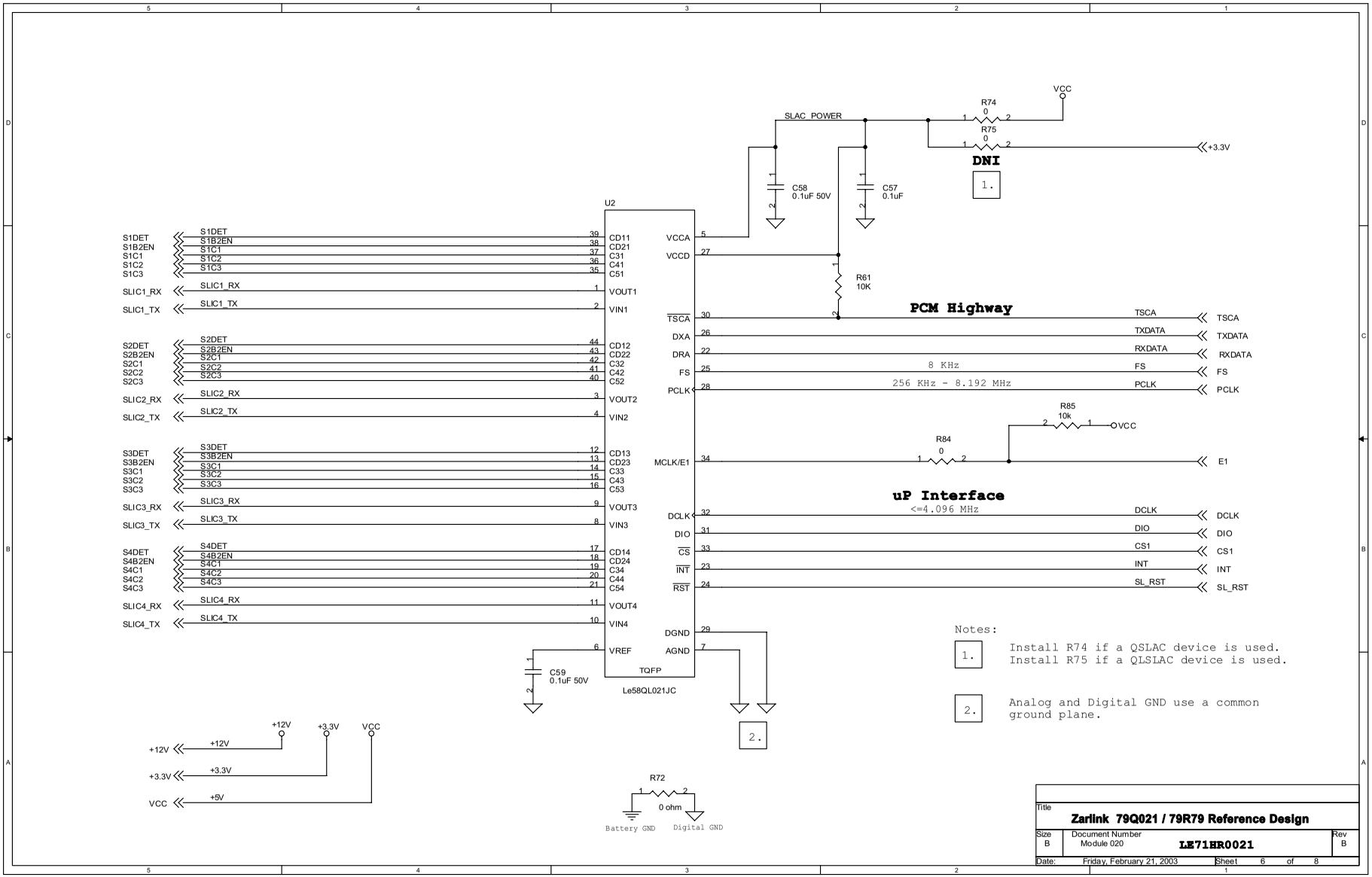
U2
Le58QL021JC
TQFP
VCC
SLAC_POWER
R74
R75
DNI
+3.3V
C58
0.1uF 50V
C57
0.1uF
R61
10K
PCM Highway
TSCA
TXDATA
RXDATA
8 KHz
FS
256 KHz - 8.192 MHz
PCLK
R85
10k
R84
E1
uP Interface
<=4.096 MHz
DCLK
DIO
CS1
INT
SL_RST
C59
0.1uF 50V
R72
0 ohm
Battery GND
Digital GND
+12V
+5V
Notes:
1. Install R74 if a QSLAC device is used.
Install R75 if a QLSLAC device is used.
2. Analog and Digital GND use a common ground plane.
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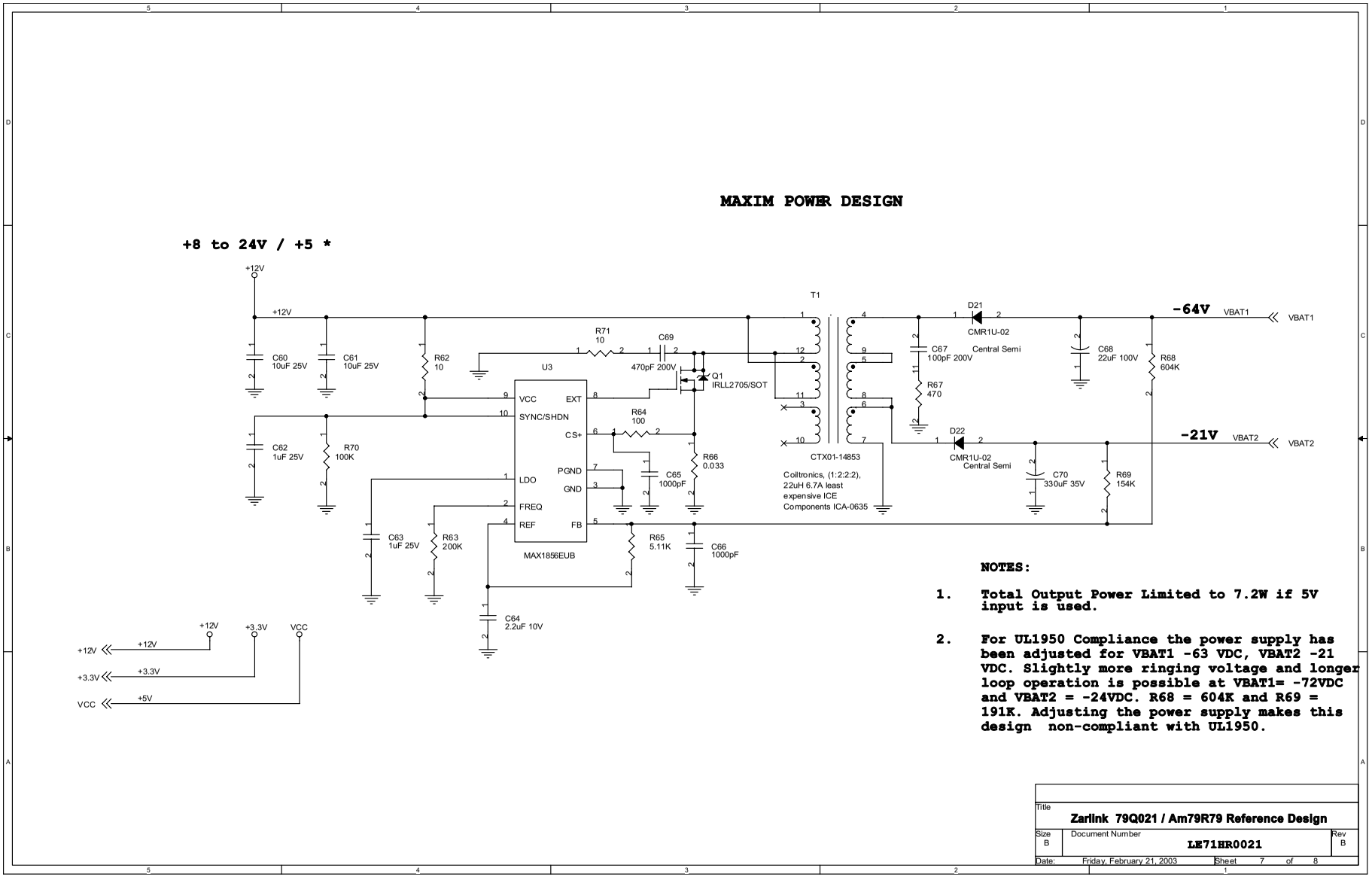
MAXIM POWER DESIGN
+8 to 24V / +5 *
+12V
T1
D21
CMR1U-02
-64V
VBAT1
C60
10uF 25V
C61
10uF 25V
R62
10
R71
10
C69
470pF 200V
U3
Q1
IRLL2705/SOT
C67
100pF 200V
Central Semi
C68
22uF 100V
R68
604K
R67
470
VCC
EXT
SYNC/SHDN
R64
100
CS+
C62
1uF 25V
R70
100K
R66
0.033
PGND
GND
C65
1000pF
CTX01-14853
Coiltronics, (1:2:2:2),
22uH 6.7A least
expensive ICE
Components ICA-0635
D22
CMR1U-02
Central Semi
-21V
VBAT2
C70
330uF 35V
R69
154K
LDO
FREQ
REF
FB
C63
1uF 25V
R63
200K
MAX1856EUB
R65
5.11K
C66
1000pF
C64
2.2uF 10V
+3.3V
VCC
+5V
NOTES:
1. Total Output Power Limited to 7.2W if 5V input is used.
2. For UL1950 Compliance the power supply has been adjusted for VBAT1 -63 VDC, VBAT2 -21 VDC. Slightly more ringing voltage and longer loop operation is possible at VBAT1= -72VDC and VBAT2 = -24VDC. R68 = 604K and R69 = 191K. Adjusting the power supply makes this design non-compliant with UL1950.
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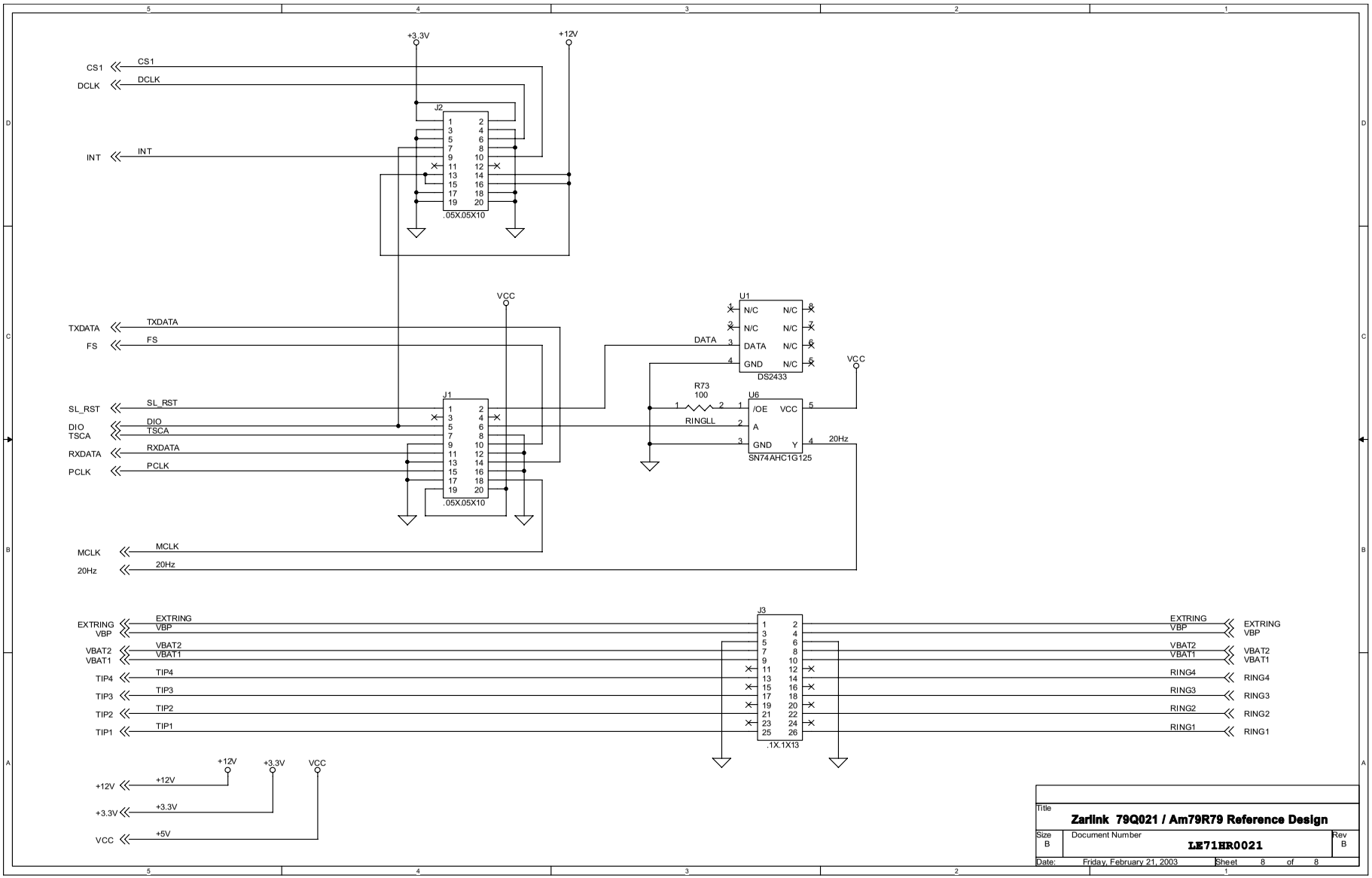
+3.3V
+12V
CS1
DCLK
INT
J2
.05X.05X10
VCC
TXDATA
FS
SL_RST
DIO
TSCA
RXDATA
PCLK
J1
.05X.05X10
U1
N/C
DATA
GND
DS2433
R73
100
RINGLL
U6
/OE
VCC
A
GND
Y
SN74AHC1G125
20Hz
MCLK
EXTRING
VBP
VBAT2
VBAT1
TIP4
TIP3
TIP2
TIP1
J3
.1X.1X13
RING4
RING3
RING2
RING1
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6.2 BILL OF MATERIALS

Item	Assy.	Part Number	Manufacturer	Tol.	Voltage	Package	Description & Package Type	Ref. Des.
1	8	C0603C222M1RAC	Kemet	20%	100V	SM/C_0603	2.2nF 100V	C1, C2, C15, C16, C29, C30, C43, C44
2	4	C1206C473M1RAC	Kemet	20%	100V	SM/C_1206	47nF 100V	C3, C17, C31, C45
3	6	ECJ-2YB1A564K	AVX	20%	10V	SM/C_0805	0.56uF	C4, C5, C12, C18, C19, C26
5	6	0805ZC564MAT2A	AVX	20%	10V	SM/C_0805	0.56uF	C32, C33, C40, C46, C47, C54
6	4	C1206C104M1RAC	Kemet	20%	100V	SM/C_1206	0.1uF 100V	C6, C20, C34, C48
7	6	C0805C104M5RAC	Kemet	20%	50V	SM/C_0805	0.1uF 50V	C7, C21, C35, C49, C58, C59
8	4	C0805C334M4RAC	Kemet	20%	10V	SM/C_0805	0.33uF	C8, C22, C36, C50
9	5	C0603C104M4RAC	Kemet	20%	16V	SM/C_0603	0.1uF 16V	C9, C23, C37, C51, C57
10	8	C0805C224M4RAC	Kemet	20%	16V	SM/C_0805	0.22uF 16V	C11, C13, C25, C27, C39, C41, C53, C55
11	4	C0603C153M4RAC	Kemet	20%	16V	SM/C_0603	15nF	C14, C28, C42, C56
12	2	TMK432BJ106KM	Taiyo Yuden	10%	25V	SM/C_1812	10uF 25V	C60, C61
13	1	TMK316BJ105KL	Taiyo Yuden	10%	25V	SM/C_1206	1uF 25V	C62
14	1	LMK212BJ105KG	Taiyo Yuden	10%	10V	SM/C_0805	1uF 25V	C63
15	1	GRM42-6X7R225K010AD	Murata	10%	10V	SM/C_1206	2.2uF 10V	C64
16	2	0805-5A-102-JAT-2A	AVX	5%	50V	SM/C_0805	1000pF	C65,C66
17	1	GRM40COG101K200	Murata	10%	200V	SM/C_0805	100pF 200V	C67
18	1	100MV22AX,EEU-FC2A220	SANYO	80%	100V	CYL/D.325/ LS.125/.034	22uF 100V	C68
19	1	GRM40X7R471K200	Murata	10%	200V	SM/C_0805	470pF 200V	C69
20	1	35MV100AX, EEU-FC1V331	SANYO	80%	35V	CYL/D.325/ LS.125/.034	330uF 35V	C70
21	8	P0641SC	Teccor		58/77V	SM/DO214AA_12	P0641SC/SM	D1, D2, D7, D11, D12, D16, D17, D23
22	8	BAS16DICT-ND	General Semi		100V	SOT-23	BAS16/SOT	D4, D6, D8, D10, D13, D15, D18, D20
23	4	BAS70DICT-ND	General Semi		70V	SOT-23	BAS70/SOT	D5, D9, D14, D19
24	2	CMR1U-02	Central Semi	U	200V	SM/_SMB	CMR1U-02	D21, D22
25	8	F1250T 1.25A replaces MZ2L-50R	Teccor replaces ChiCom				F1250T 1.25A	F1-F8
26	2	SMS-110-01-S-D	SamTec			.5X.1X10Dual Row	Conn 20	J1, J2
28	1	SSQ-113-01-S-D	SamTec			.1X.1X13Dual Row	Conn 26	J3
29	1	IRLL2705-ND	Intl Rect		55V	TO261AA/SOT223	IRLL2705/SOT	Q1
30	8	ERJ-3EKF51R1	Panasonic	1%		SM/R_0805	51.1	R1, R2, R16, R17, R31, R32, R46, R47
31	4	ERJ-3EKF1212	Panasonic	1%		SM/R_0603	12.1K	R3, R18, R33, R48
32	4	ERJ-3EKF	Panasonic	1%		SM/R_0603	432K	R4, R19, R34, R49
33	4	ERJ-3EKF	Panasonic	1%		SM/R_0603	150K	R5, R20, R35, R50
33a	1					SM/R_1210	0	R72
34	7	ERJ-3EKF				SM/R_0603	0	R76, R78, R80, R82, R84, R74
34a	13	no install						R77, R79,R81,R83, R75, R6, R14, R21, R29, R36, R44, R51, R59
35	8	ERJ-3EKF	Panasonic	1%		SM/R_0603	254K OR 255K	R7, R10, R22, R25, R37, R40, R52, R55
36	8	ERJ-3EKF	Panasonic	1%		SM/R_0603	49.9K	R8, R9, R23, R24, R38, R39, R53, R54
37	8	ERJ-3EKF	Panasonic	1%		SM/R_0603	18.7K	R11, R12, R26, R27, R41, R42, R56, R57
38	4	ERJ-3EKF	Panasonic	1%		SM/R_0603	68.1K	R13, R28, R43, R58
40	6	ERJ-3EKF	Panasonic	1%		SM/R_0603	10K	R15, R30, R45, R60, R61, R85
41	1	ERJ-3EKF	Panasonic	5%		SM/R_1210	10	R62
42	1	ERJ-3EKF	Panasonic	5%		SM/R_1210	10	R71
43	1	ERJ-3EKF	Panasonic	1%		SM/R_0805	200K	R63
44	1	ERJ-3EKF	Panasonic	1%		SM/R_0805	100	R64
44A	1			1%		SM/R_0603	100	R73
45	1	ERJ-3EKF	Panasonic	1%		SM/R_0805	5.11K	R65
46	1	WSL2010 0.033R	IRC	1%		SM/R_2512	0.033	R66
47	1	ERJ-3EKF	Panasonic	5%		SM/R_2010	470	R67
48	1	ERJ-3EKF	Panasonic	1%		SM/R_0805	604K	R68
49	1	ERJ-3EKF	Panasonic	1%		SM/R_0805	154K	R69
50	1	ERJ-3EKF	Panasonic	1%		SM/R_0805	100K	R70
51	1	CTX01-14853	Coiltronics			**	CTX01-14853	T1
52	1	Le79Q021JC	Zarlink			TQFP44	Le79Q021	U2
53	1	MAX1856EUB	Maxim			uMAX**	MAX1856	U3
54	1	SN74AHC1G125DCKR	TI			SO-6	74AHC1G125	U6
55	1	DS2433S	Dallas Semi			SO-8 (208 MIL)	DS2433	U1
56	4	Le79R79-3JC	Zarlink			PLCC32	Le79R79	U11, U12, U13, U14

CHAPTER

7 BOARD LAYOUT

7.1 BOARD LAYOUT GRAPHICS

This design uses a four-layer FR4 fiberglass design with 1 oz. copper. The internal layer consists of a ground plane and a power plane. The ground plane is composed of two grounds, a signal ground and a battery ground. These grounds are tied together near the point of entry onto the board. All safety devices are connected to the battery ground since this ground is routed around the SLIC and SLAC devices.

Also note that the power supply routing is placed mostly on the top side of the board. In addition, the traces in the high current paths have been made as wide as possible. This minimizes the trace inductances in the high current switching paths, increases efficiency, and reduces radiated and conducted noise.

Figure 7–1 Top Side Silk Screen

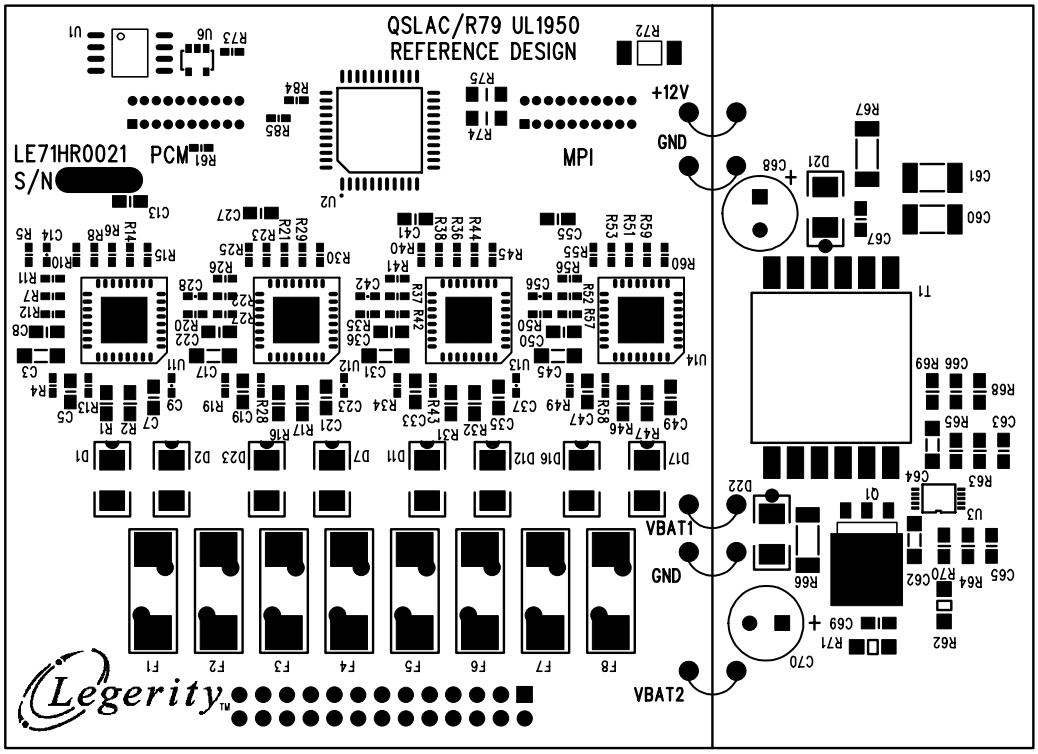

Figure 7–2 Top (Component) Side

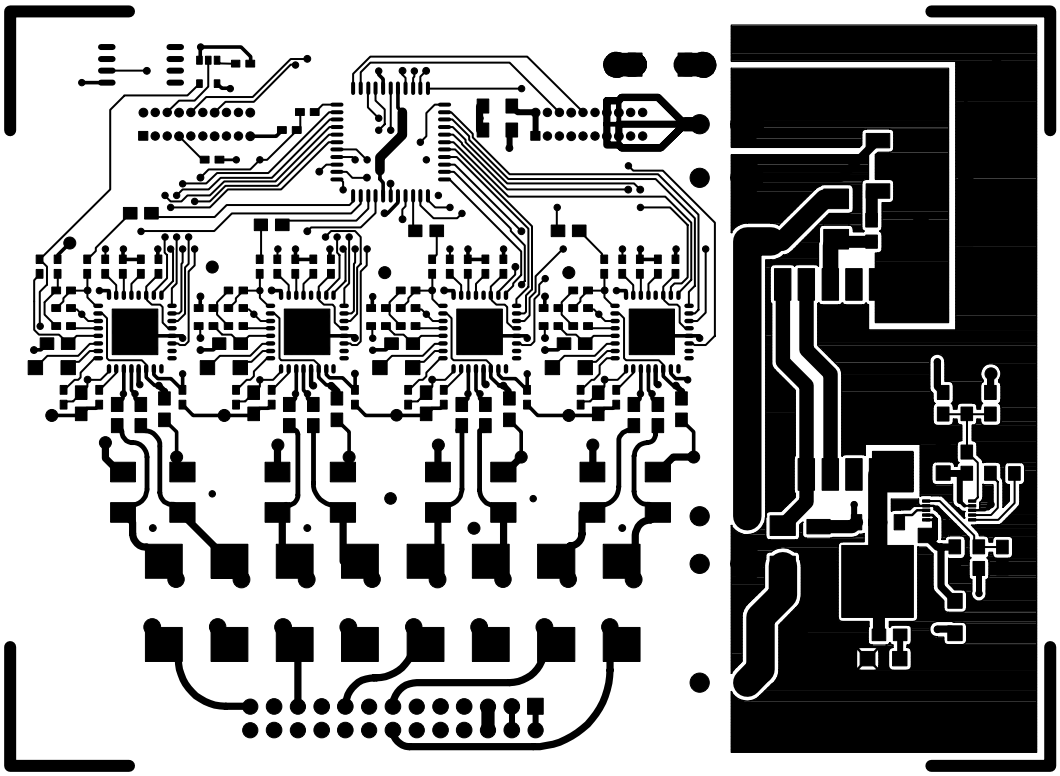

Figure 7–3 Internal Layer 1 (Ground Plane)

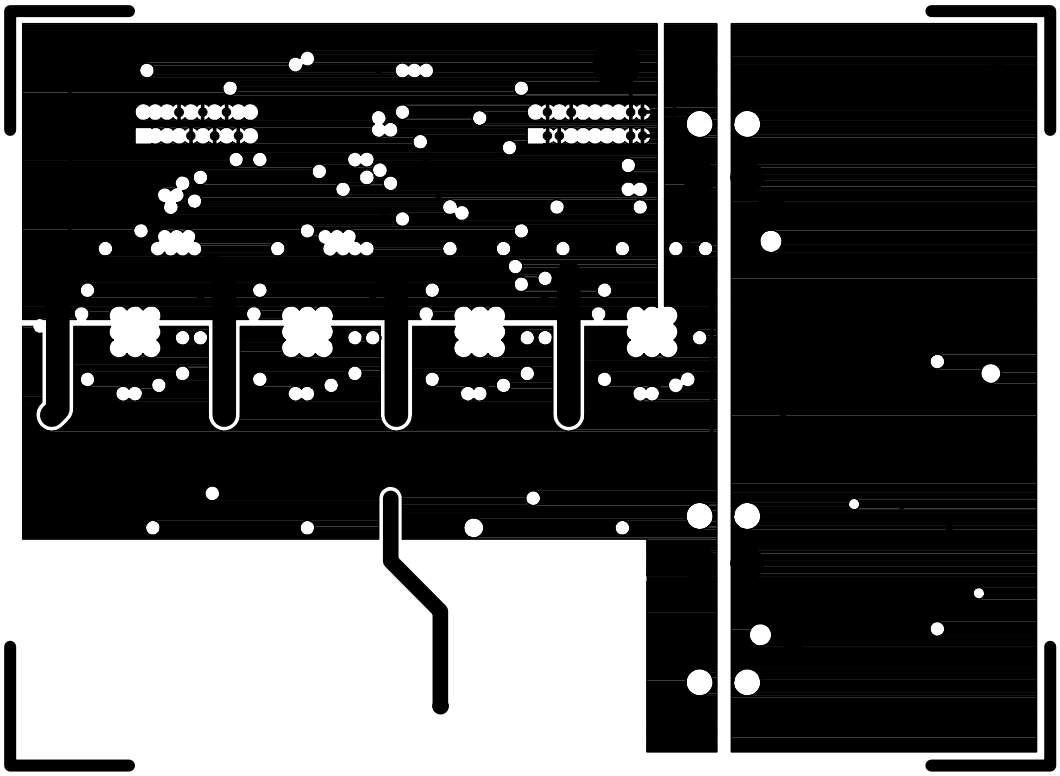

Figure 7–4 VCC Layer

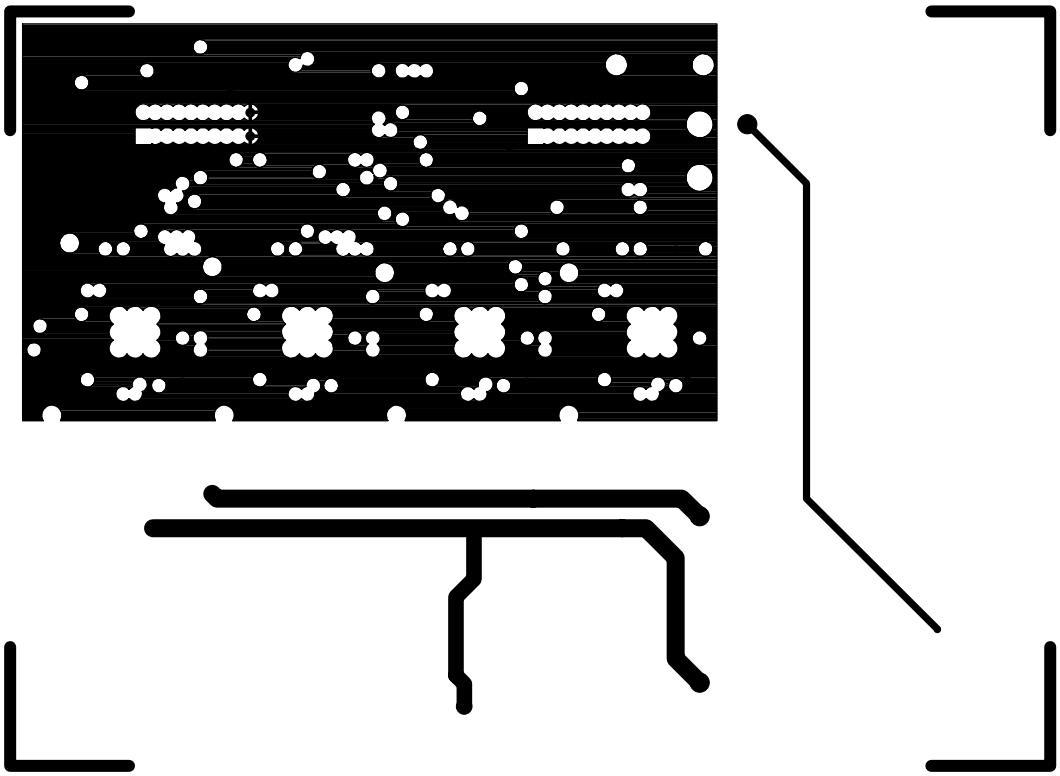

Figure 7–5 Solder Side Silk Screen