MIC2179

1.5A Synchronous Buck Regulator

Features

- Input Voltage Range: +4.5V to +16.5V
- Dual-Mode Operation for High Efficiency (up to 96%):
  - PWM Mode for > 150 mA Load Current
  - Skip Mode for < 150 mA Load Current
- 150 mΩ Internal Power MOSFETs at 12V Input
- 200 kHz Preset Switching Frequency
- Low Quiescent Current
  - 1.0 mA in PWM Mode
  - 600 µA in Skip Mode
  - < 5 µA in Shutdown Mode
- Current-Mode Control
  - Simplified Loop Compensation
  - Superior Line Regulation
- 100% Duty Cycle for Low Dropout Operation
- Current Limit
- Thermal Shutdown
- Undervoltage Lockout

Applications

- High-Efficiency, Battery-Powered Supplies
- Buck (Step-Down) DC/DC Converters
- Laptop Computers
- Cellular Telephones
- Handheld Instruments
- Battery Chargers

General Description

The MIC2179 is a 200 kHz synchronous buck (step-down) switching regulator designed for high-efficiency, battery-powered applications.

The MIC2179 operates from a 4.5V to 16.5V input and features internal power MOSFETs that can supply up to 1.5A output current. It can operate with a maximum duty cycle of 100% for use in low-dropout conditions. It also features a shutdown mode that reduces quiescent current to less than 5 µA.

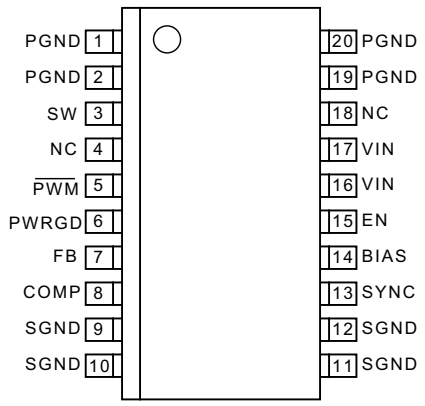
The MIC2179 achieves high efficiency over a wide output current range by operating in either PWM or skip mode. The operating mode is externally selected, typically by an intelligent system, which chooses the appropriate mode according to operating conditions, efficiency, and noise requirements. The switching frequency is preset to 200 kHz and can be synchronized to an external clock signal of up to 300 kHz.

The MIC2179 uses current-mode control with internal current sensing. Current-mode control provides superior line regulation and makes the regulator control loop easy to compensate. The output is protected with pulse-by-pulse current limiting and thermal shutdown. Undervoltage lockout turns the output off when the input voltage is less than 4.5V.

The MIC2179 is packaged in a 20-lead SSOP package with an operating temperature range of -40°C to +85°C.

Package Type

MIC2179
20-Lead SSOP (SM)
(Top View)



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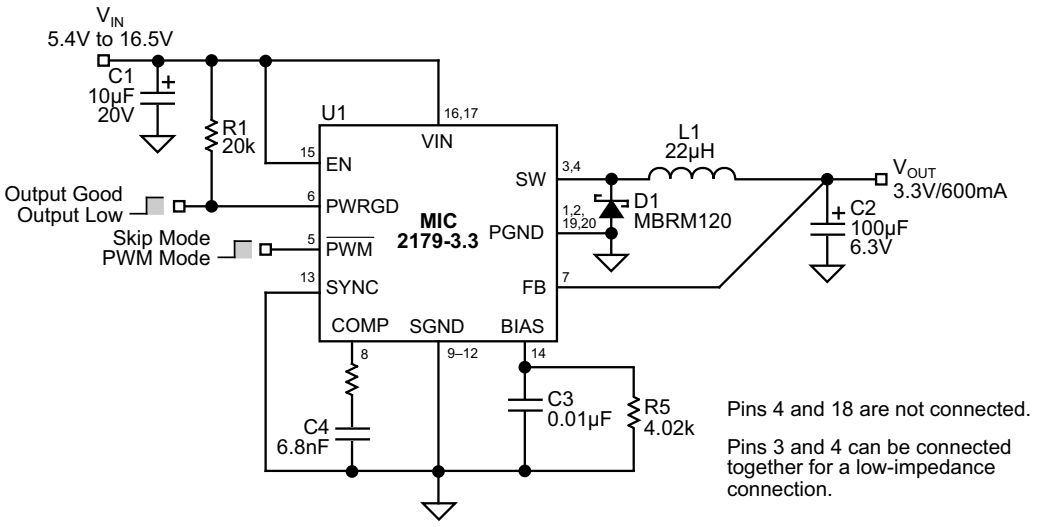
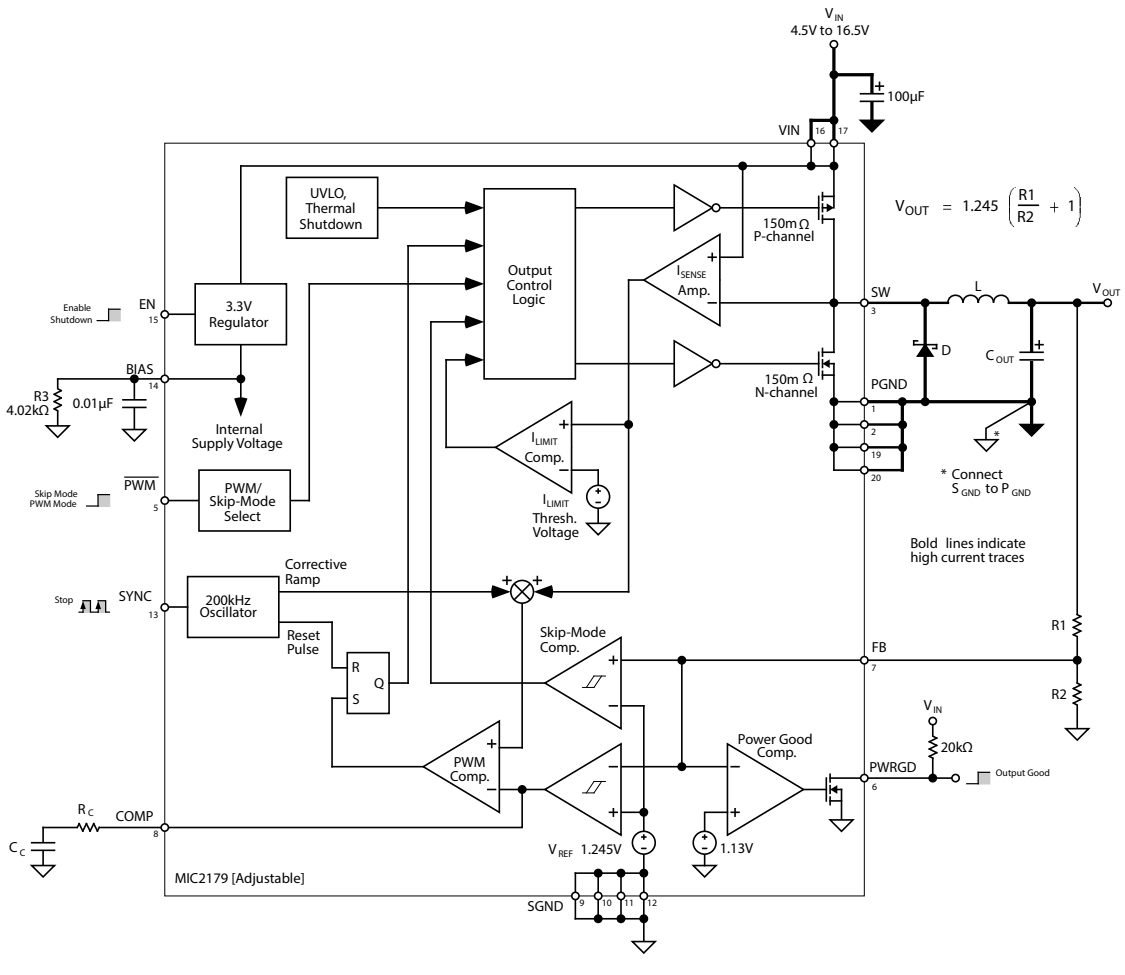
Typical Application Circuit



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage, 100 ms Transient (V_{IN}) ..... +18V
Output Switch Voltage (V_{SW}) ..... +18V
Output Switch Current (I_{SW}) 6.0A
Enable, $\overline{PWM}$ Control Voltage (V_{EN}, $V_{\overline{PWM}}$) ..... +18V
Sync Voltage (V_{SYNC}) ..... +6V

Operating Ratings ††

Supply Voltage (V_{IN}) ..... +4.5V to +16.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = 7.0V; T_A = +25°C, **bold** indicates –40°C ≤ T_A ≤ +85°C; unless noted. Devices are ESD sensitive. Handling precautions recommended.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Supply Current	I_{SS}	—	1.0	**1.5**	mA	PWM mode, output not switching, 4.5V ≤ V_{IN} ≤ 16.5V
		—	600	**750**	µA	Skip mode, output not switching, 4.5V ≤ V_{IN} ≤ 16.5V
		—	1	**25**	µA	V_{EN} = 0V, 4.5V ≤ V_{IN} ≤ 16.5V
Bias Regulator Output Voltage	V_{BIAS}	**3.10**	3.30	**3.4**	V	V_{IN} = 16.5V
Feedback Voltage	V_{FB}	**1.22**	1.245	**1.27**	V	MIC2179 [adj.]: V_{OUT} = 3.3V, I_{LOAD} = 0A
Output Voltage	V_{OUT}	3.20	3.3	3.40	V	MIC2179 [adj.]: V_{OUT} = 3.3V, 5V ≤ V_{IN} ≤ 16V, 10 mA ≤ I_{LOAD} ≤ 1A
		3.14	—	**3.46**	V	
		4.85	5.0	**5.15**	V	MIC2179-5.0: I_{LOAD} = 0A
		4.85	5.0	5.15	V	MIC2179-5.0: 6V ≤ V_{IN} ≤ 16V, 10 mA ≤ I_{LOAD} ≤ 1A
		4.75	—	**5.25**	V	
		3.20	3.3	**3.40**	V	MIC2179-3.3: I_{LOAD} = 0A
		3.20	3.3	3.40	V	MIC2179-3.3: 5V ≤ V_{IN} ≤ 16V, 10 mA ≤ I_{LOAD} ≤ 1A
		3.14	—	**3.46**	V	
Undervoltage Lockout	V_{TH}	—	4.25	**4.35**	V	Upper threshold
	V_{TL}	**3.90**	4.15	—	V	Lower threshold
Feedback Bias Current	I_{FB}	—	60	**150**	nA	MIC2179 [adj.]
		—	20	**40**	µA	MIC2179-5.0, MIC2179-3.3
Error Amplifier Gain	A_{VOL}	**15**	18	**20**	—	0.6V ≤ V_{COMP} ≤ 0.8V
Error Amplifier Output Swing	—	**0.9**	15	—	V	Upper Limit
		—	0.05	**0.1**		Lower Limit

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 7.0V; T_A = +25°C, **bold** indicates –40°C ≤ T_A ≤ +85°C; unless noted. Devices are ESD sensitive. Handling precautions recommended.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Error Amplifier Output Current	—	**15**	25	**35**	µA	Source and sink
Oscillator Frequency	f_O	**160**	200	**240**	kHz	—
Maximum Duty Cycle	D_{MAX}	**100**	—	—	%	V_{FB} = 1.0V
Minimum On-Time	$t_{ON(MIN)}$	—	300	**400**	ns	V_{FB} = 1.5V
SYNC Frequency Range	—	**220**	—	**300**	kHz	—
SYNC Threshold	—	**0.8**	1.6	**2.2**	V	—
SYNC Minimum Pulse Width	—	**500**	—	—	ns	—
SYNC Leakage	I_{SYNC}	**–1**	0.01	**1**	µA	V_{SYNC} = 0V to 5.5V
Current Limit	I_{LIM}	**3.4**	4.3	**5.5**	A	PWM mode, V_{IN} = 12V
		—	600	—	mA	Skip mode
Switch On-Resistance	R_{ON}	—	160	**350**	mΩ	High-side switch, V_{IN} = 12V
		—	140	**350**		Low-side switch, V_{IN} = 12V
Output Switch Leakage	I_{SW}	—	1	**10**	µA	V_{SW} = 16.5V
Enable Threshold	—	**0.8**	1.6	**2.2**	V	—
Enable Leakage	I_{EN}	**–1**	0.01	**1**	µA	V_{EN} = 0V to 5.5V
$\overline{PWM}$ Threshold	—	**0.6**	1.1	**1.4**	V	—
$\overline{PWM}$ Leakage	$I_{\overline{PWM}}$	**–1**	0.01	**1**	µA	$V_{\overline{PWM}}$ = 0V to 5.5V
PWRGD Threshold	—	**1.09**	1.13	**1.17**	V	MIC2179 [adj.]: measured at FB pin
		4.33	4.54	**4.75**		MIC2179-5.0: measured at FB pin
		2.87	3.00	**3.13**		MIC2179-3.3: measured at FB pin
PWRGD Output Low	—	—	0.25	**0.4**	V	I_{SINK} = 0.5 mA
PWRGD Off Leakage	—	—	0.01	**1**	µA	V_{PWRGD} = 5.5V

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	–40	—	+125	°C	Note 1

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

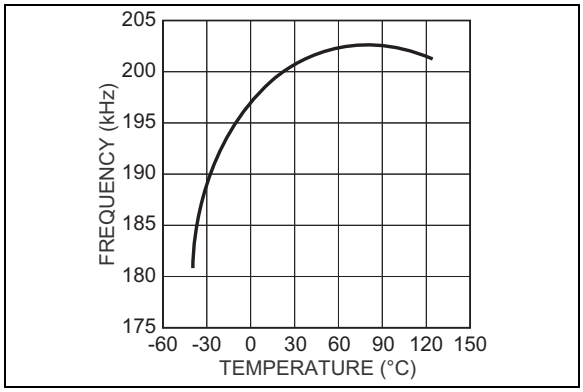

FIGURE 2-1: *Oscillator Frequency vs. Temperature.*

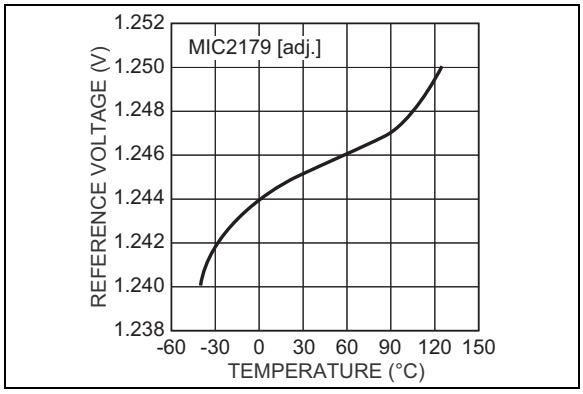

FIGURE 2-2: *Reference Voltage vs. Temperature.*

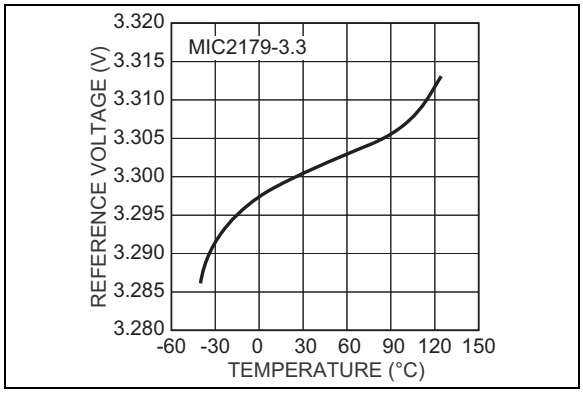

FIGURE 2-3: *Reference Voltage vs. Temperature.*

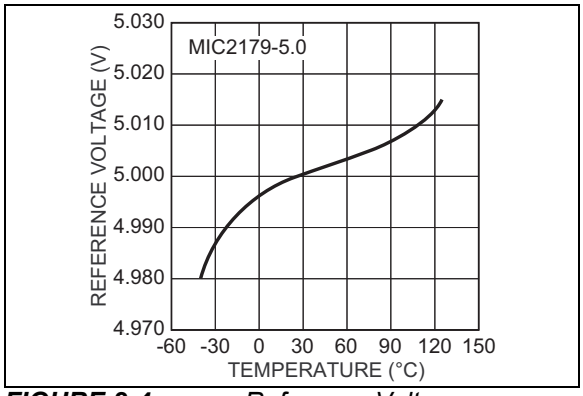

FIGURE 2-4: *Reference Voltage vs. Temperature.*

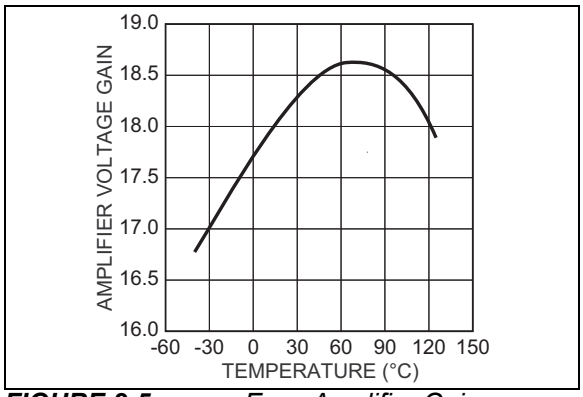

FIGURE 2-5: *Error-Amplifier Gain vs. Temperature.*

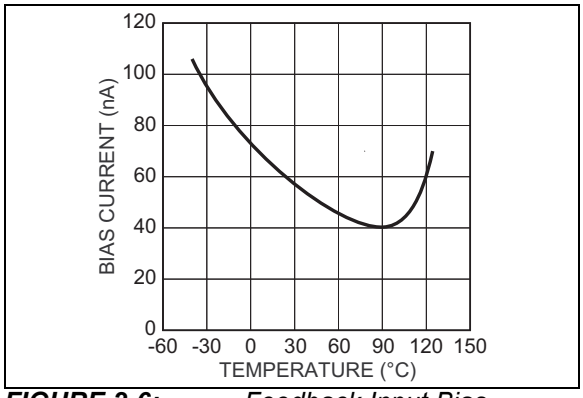

FIGURE 2-6: *Feedback Input Bias Current vs. Temperature.*

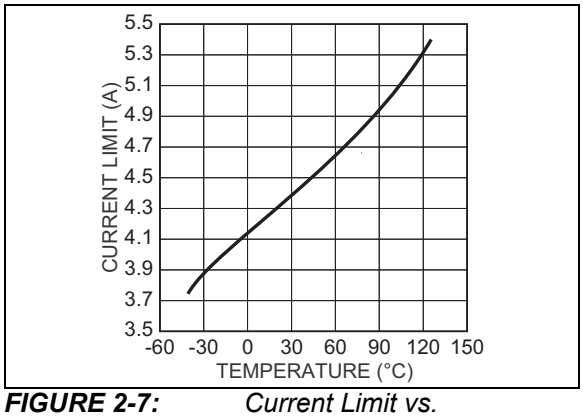

FIGURE 2-7: *Current Limit vs. Temperature.*

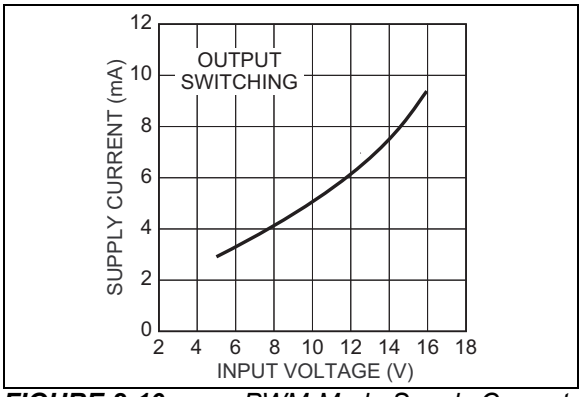

FIGURE 2-10: *PWM-Mode Supply Current.*

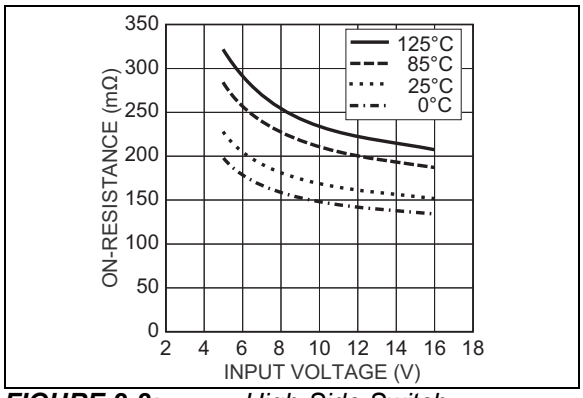

FIGURE 2-8: *High-Side Switch On-Resistance.*

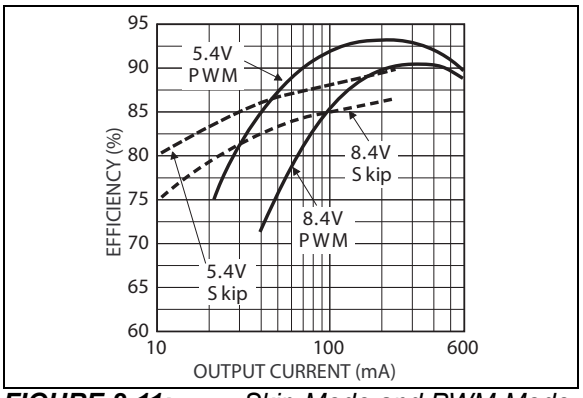

FIGURE 2-11: *Skip-Mode and PWM-Mode Efficiency.*

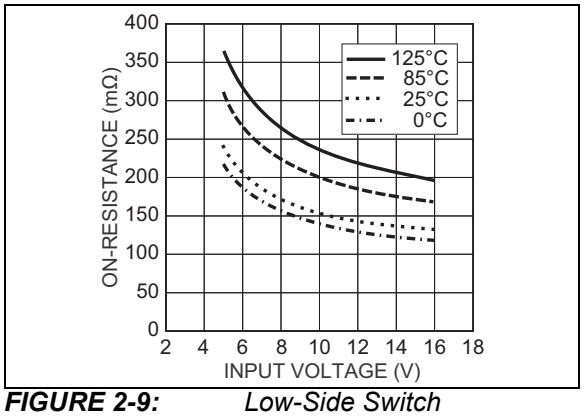

FIGURE 2-9: *Low-Side Switch On-Resistance.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2, 19, 20	PGND	Power ground: Connect all pins to central ground point.
3	SW	Switch (output): Internal power MOSFET output switches.
4, 18	NC	Not internally connected.
5	$\overline{\text{PWM}}$	PWM/Skip Mode Control (input): Logic-level input. Controls regulator operating mode. Logic low enables PWM mode. Logic high enables skip mode. Do not allow pin to float.
6	PWRGD	Error flag (output): Open-drain output. Active-low when FB input is 10% below the reference voltage (V_{REF}).
7	FB	Feedback (input): Connect to output voltage divider resistors.
8	COMP	Compensation: Output of internal error amplifier. Connect capacitor or series RC network to compensate the regulator control loop.
9, 10, 11, 12	SGND	Signal ground: Connect all pins to ground, PGND.
13	SYNC	Frequency synchronization (input): Optional. Connect an external clock signal to synchronize the oscillator. Leading edge of signal above 1.7V terminates switching cycle. Connect to SGND if not used.
14	BIAS	Internal 3.3V bias supply: Decouple with 0.01 µF bypass capacitor to SGND. Do not apply any external load.
15	EN	Enable (input): Logic high enables operation. Logic low shuts down regulator. Do not allow pin to float.
16, 17	VIN	Supply voltage (input): Requires bypass capacitor to PGND. Both pins must be connected to VIN.

4.0 FUNCTIONAL DESCRIPTION

The MIC2179 is a synchronous buck regulator that operates from an input voltage of 4.5V to 16.5V and provides a regulated output voltage of 1.25V to 16.5V. It has internal power MOSFETs that supply up to 1.5A load current and operates with up to 100% duty cycle to allow low-dropout operation. To optimize efficiency, the MIC2179 operates in PWM and skip mode. Skip mode provides the best efficiency when load current is less than 150 mA, while PWM mode is more efficient at higher current. PWM or skip mode operation is selected externally, allowing an intelligent system (i.e. microprocessor controlled) to select the correct operating mode for efficiency and noise requirements.

During PWM operation, the MIC2179 uses current-mode control that provides superior line regulation and makes the control loop easier to compensate. The PWM switching frequency is set internally to 200 kHz and can be synchronized to an external clock frequency up to 300 kHz. Other features include a low-current shutdown mode, current limit, undervoltage lockout, and thermal shutdown. See the following sections for more detail.

4.1 Switch Output

The switch output (SW) is a half H-bridge consisting of a high-side P-channel and low-side N-channel power MOSFET. These MOSFETs have a typical on-resistance of 150 mΩ when the MIC2179 operates from a 12V supply. Anti-shoot-through circuitry prevents the P-channel and N-channel from turning on at the same time.

4.2 Current Limit

The MIC2179 uses pulse-by-pulse current limiting to protect the output. During each switching period, a current limit comparator detects if the P-channel current exceeds 4.3A. When it does, the P-channel is turned off until the next switching period begins.

4.3 Undervoltage Lockout

Undervoltage lockout (UVLO) turns off the output when the input voltage (V_{IN}) is too low to provide sufficient gate drive for the output MOSFETs. It prevents the output from turning on until V_{IN} exceeds 4.3V. Once operating, the output will not shut off until V_{IN} drops below 4.2V.

4.4 Thermal Shutdown

Thermal shutdown turns off the output when the MIC2179 junction temperature exceeds the maximum value for safe operation. After thermal shutdown occurs, the output will not turn on until the junction temperature drops approximately 10°C.

4.5 Shutdown Mode

The MIC2179 has a low-current shutdown mode that is controlled by the enable input (EN). When a logic 0 is applied to EN, the MIC2179 is in shutdown mode, and its quiescent current drops to less than 5 µA.

4.6 Internal Bias Regulator

An internal 3.3V regulator provides power to the MIC2179 control circuits. This internal supply is brought out to the BIAS pin for bypassing by an external 0.01 µF capacitor. Do not connect an external load to the BIAS pin. It is not designed to provide an external supply voltage.

4.7 Frequency Synchronization

The MIC2179 operates at a preset switching frequency of 200 kHz. It can be synchronized to a higher frequency by connecting an external clock to the SYNC pin. The SYNC pin is a logic level input that synchronizes the oscillator to the rising edge of an external clock signal. It has a frequency range of 220 kHz to 300 kHz, and can operate with a minimum pulse width of 500 ns. If synchronization is not required, connect SYNC to ground.

4.8 Power Good Flag

The power good flag (PWRGD) is an error flag that alerts a system when the output is not in regulation. When the output voltage is 10% below its nominal value, PWRGD is logic low, signaling that V_{OUT} is too low. PWRGD is an open-drain output that can sink 1 mA from a pull-up resistor connected to V_{IN}.

4.9 Low-Dropout Operation

Output regulation is maintained in PWM or skip mode even when the difference between V_{IN} and V_{OUT} decreases below 1V. As $V_{IN} – V_{OUT}$ decreases, the duty cycle increases until it reaches 100%. At this point, the P-channel is kept on for several cycles at a time, and the output stays in regulation until $V_{IN} – V_{OUT}$ falls below the dropout voltage (dropout voltage = P-channel on-resistance × load current).

4.10 PWM-Mode Operation

Refer to the PWM Mode Functional Diagram which is a simplified block diagram of the MIC2179 operating in PWM mode and its associated waveforms.

When operating in PWM mode, the output P-channel and N-channel MOSFETs are alternately switched on at a constant frequency and variable duty cycle. A switching period begins when the oscillator generates a reset pulse. This pulse resets the RS latch which turns on the P-channel and turns off the N-channel. During this time, inductor current (I_{L1}) increases and

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energy is stored in the inductor. The current sense amplifier (I_{SENSE} Amp) measures the P-channel drain-to-source voltage and outputs a voltage proportional to I_{L1}. The output of I_{SENSE} Amp is added to a sawtooth waveform (corrective ramp) generated by the oscillator, creating a composite waveform labeled I_{SENSE} on the timing diagram. When I_{SENSE} is greater than the error amplifier output, the PWM comparator will set the RS latch which turns off the P-channel and turns on the N-channel. Energy is then discharged from the inductor and I_{L1} decreases until the next switching cycle begins. By varying the P-channel on-time (duty cycle), the average inductor current is adjusted to whatever value is required to regulate the output voltage.

The MIC2179 uses current-mode control to adjust the duty cycle and regulate the output voltage. Current-mode control has two signal loops that determine the duty cycle. One is an outer loop that senses the output voltage, and the other is a faster inner loop that senses the inductor current. Signals from these two loops control the duty cycle in the following way: V_{OUT} is fed back to the error amplifier which compares the feedback voltage (V_{FB}) to an internal reference voltage (V_{REF}). When V_{OUT} is lower than its nominal value, the error amplifier output voltage increases. This voltage then intersects the current sense waveform later in switching period which increases the duty cycle and the average inductor current. If V_{OUT} is higher than nominal, the error amplifier output voltage decreases, reducing the duty cycle.

The PWM control loop is stabilized in two ways. First, the inner signal loop is compensated by adding a corrective ramp to the output of the current sense amplifier. This allows the regulator to remain stable when operating at greater than 50% duty cycle. Second, a series resistor-capacitor load is connected to the error amplifier output (COMP pin). This places a pole-zero pair in the regulator control loop.

One more important item is synchronous rectification. As mentioned earlier, the N-channel output MOSFET is turned on after the P-channel turns off. When the N-channel turns on, its on-resistance is low enough to create a short across the output diode. As a result, inductor current flows through the N-channel and the voltage drop across it is significantly lower than a diode forward voltage. This reduces power dissipation and improves efficiency to greater than 95% under certain operating conditions.

To prevent shoot-through current, the output stage employs break-before-make circuitry that provides approximately 50 ns of delay from the time one MOSFET turns off and the other turns on. As a result, inductor current briefly flows through the output diode during this transition.

4.11 Skip Mode Operation

Refer to the Skip Mode Functional Diagram which is a simplified block diagram of the MIC2179 operating in skip mode and its associated waveforms.

Skip mode operation turns on the output P-channel at a frequency and duty cycle that is a function of V_{IN}, V_{OUT}, and the output inductor value. While in skip mode, the N-channel is kept off to optimize efficiency by reducing gate charge dissipation. V_{OUT} is regulated by skipping switching cycles that turn on the P-channel.

To begin analyzing MIC2179 skip mode operation, assume the skip mode comparator output is high and the latch output has been reset to a logic 1. This turns on the P-channel and causes I_{L1} to increase linearly until it reaches a current limit of 600 mA. When I_{L1} reaches this value, the current limit comparator sets the RS latch output to logic 0, turning off the P-channel. The output switch voltage (V_{SW}) then swings from V_{IN} to 0.4V below ground, and I_{L1} flows through the Schottky diode. L1 discharges its energy to the output and I_{L1} decreases to zero. When I_{L1} = 0, V_{SW} swings from -0.4V to V_{OUT}, and this triggers a one-shot that resets the RS latch. Resetting the RS latch turns on the P-channel, and this begins another switching cycle.

The skip-mode comparator regulates V_{OUT} by controlling when the MIC2179 skips cycles. It compares V_{FB} to V_{REF} and has 10 mV of hysteresis to prevent oscillations in the control loop. When V_{FB} is less than V_{REF} – 5 mV, the comparator output is logic 1, allowing the P-channel to turn on. Conversely, when V_{FB} is greater than V_{REF} + 5 mV, the P-channel is turned off.

Note that this is a self-oscillating topology that explains why the switching frequency and duty cycle are a function of V_{IN}, V_{OUT}, and the value of L1. It has the unique feature (for a pulse-skipping regulator) of supplying the same value of maximum load current for any value of V_{IN}, V_{OUT}, or L1. This allows the MIC2179 to always supply up to 300 mA of load current when operating in skip mode.

4.12 Selecting PWM- or Skip-Mode Operation

PWM or skip mode operation is selected by an external logic signal applied to the $\overline{PWM}$ pin. A logic low places the MIC2179 into PWM mode, and logic high places it into skip mode. Skip mode operation provides the best efficiency when load current is less than 150 mA, and PWM operation is more efficient at higher currents.

The MIC2179 was designed to be used in intelligent systems that determine when it should operate in PWM or skip mode. This makes the MIC2179 ideal for applications where a regulator must guarantee low noise operation when supplying light load currents, such as cellular telephone, audio, and multimedia circuits.

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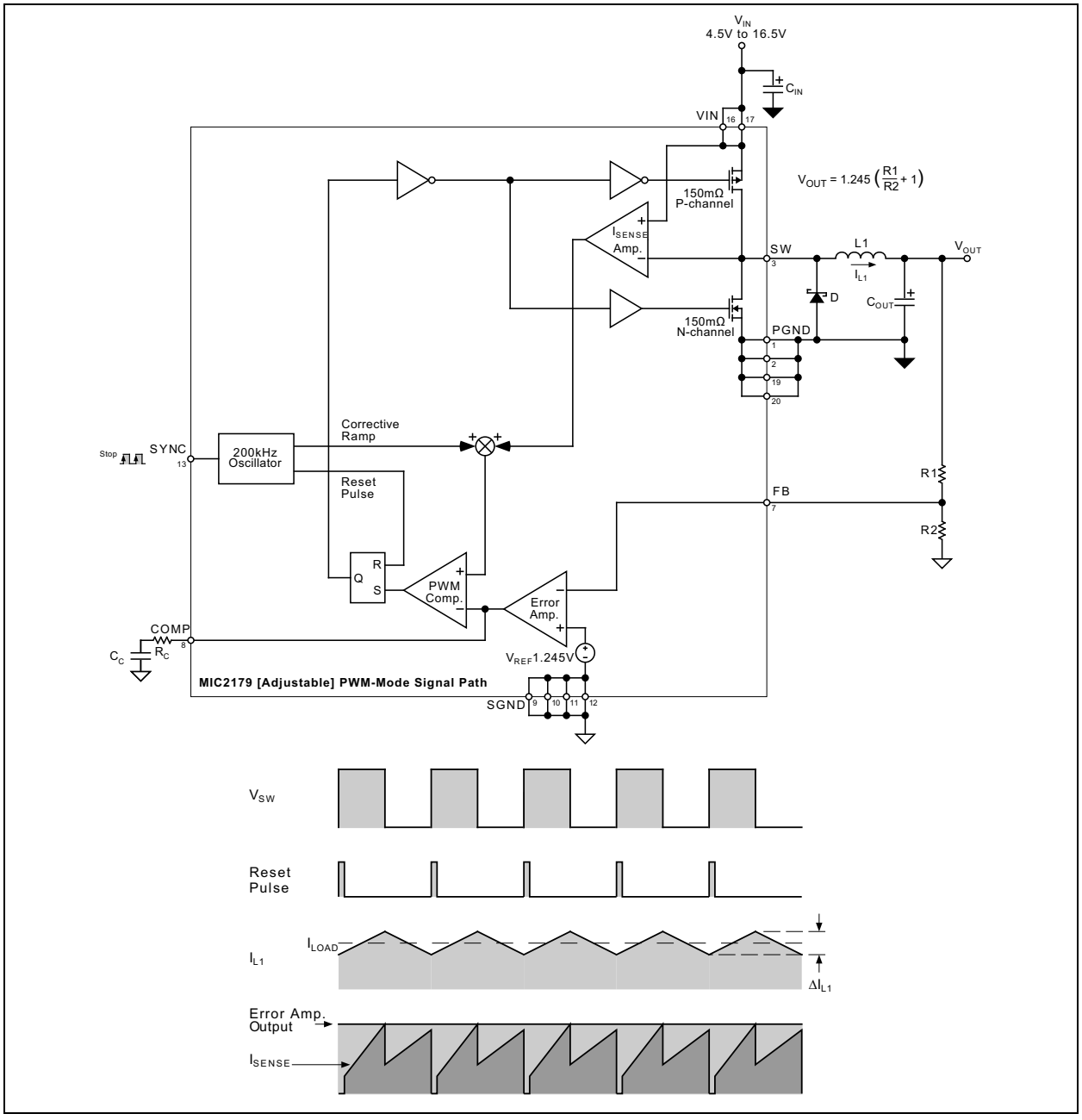
There are two important items to be aware of when selecting PWM or skip mode. First, the MIC2179 can start-up only in PWM mode, and therefore requires a logic low at $\overline{PWM}$ during start-up. Second, in skip mode, the MIC2179 will supply a maximum load current of approximately 300 mA, so the output will drop out of regulation when load current exceeds this limit. To prevent this from occurring, the MIC2179 should change from skip to PWM mode when load current exceeds 200 mA.

PWM Mode Functional Diagram



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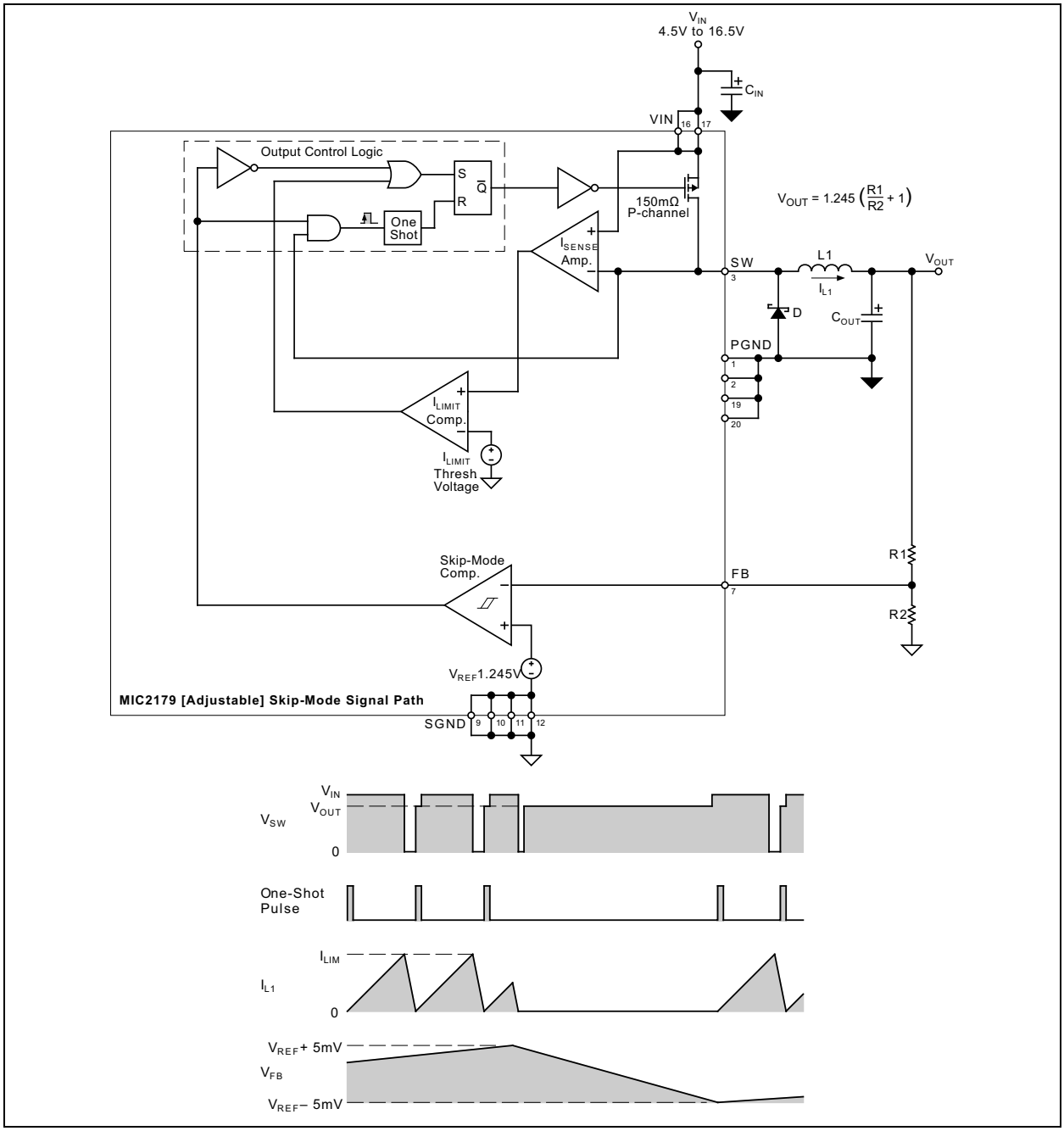
Skip Mode Functional Diagram



5.0 APPLICATION INFORMATION

5.1 Feedback Resistor Selection (Adjustable Version)

The output voltage is programmed by connecting an external resistive divider to the FB pin as shown in the Functional Block Diagram. The ratio of R1 to R2 determines the output voltage. To optimize efficiency during low output current operation, R2 should not be less than 20 kΩ. However, to prevent feedback error due to input bias current at the FB pin, R2 should not be greater than 100 kΩ. After selecting R2, calculate R1 with the following formula:

EQUATION 5-1:

$$R1 = R2 \times \left(\left(\frac{V_{OUT}}{1.245V}\right) - 1\right)$$

5.2 Input Capacitor Selection

The input capacitor is selected for its RMS current and voltage rating and should be a low ESR (equivalent series resistance) electrolytic or tantalum capacitor. As a rule of thumb, the voltage rating for a tantalum capacitor should be twice the value of V_{IN}, and the voltage rating for an electrolytic should be 40% higher than V_{IN}. The RMS current rating must be equal or greater than the maximum RMS input ripple current. A simple, worst case formula for calculating this RMS current is:

EQUATION 5-2:

$$I_{RMS(MAX)} = \frac{I_{LOAD(MAX)}}{2}$$

Tantalum capacitors are a better choice for applications that require the most compact layout or operation below 0°C. The input capacitor must be located very close to the VIN pin (within 0.2 in, 5 mm). Also, place a 0.1 µF ceramic bypass capacitor as close as possible to VIN.

5.3 Inductor Selection

The MIC2179 is a current-mode controller with internal slope compensation. As a result, the inductor must be at least a minimum value to prevent subharmonic oscillations. This minimum value is calculated by the following formula:

EQUATION 5-3:

$$L_{MIN} = V_{OUT} \times 3.0\mu H/V$$

In general, a value at least 20% greater than L_{MIN} should be selected because inductor values have a tolerance of ±20%.

Two other parameters to consider in selecting an inductor are winding resistance and peak current rating. The inductor must have a peak current rating equal or greater than the peak inductor current. Otherwise, the inductor may saturate, causing excessive current in the output switch. Also, the inductor's core loss may increase significantly. Both of these effects will degrade efficiency. The formula for peak inductor current is:

EQUATION 5-4:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{\Delta I_{L(MAX)}}{2}$$

Where:

$$\Delta I_{L(MAX)} = V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \times \frac{1}{L \times f}$$

To maximize efficiency, the inductor's resistance must be less than the output switch on-resistance (preferably, 50 mΩ or less).

5.4 Output Capacitor Selection

Select an output capacitor that has a low value of ESR. This parameter determines a regulator's output ripple voltage (V_{RIPPLE}) which is generated by ΔI_L x ESR. Therefore, ESR must be equal or less than a maximum value calculated for a specified V_{RIPPLE} (typically less than 1% of the output voltage) and $\Delta I_{L(MAX)}$:

EQUATION 5-5:

$$ESR_{MAX} = \frac{V_{RIPPLE}}{\Delta I_{L(MAX)}}$$

Typically, capacitors in the range of 100 µF to 220 µF have ESR less than this maximum value. The output capacitor can be a low ESR electrolytic or tantalum capacitor, but tantalum is a better choice for compact

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layout and operation at temperatures below 0°C. The voltage rating of a tantalum capacitor must be $2 \times V_{OUT}$, and the voltage rating of an electrolytic must be $1.4 \times V_{OUT}$.

5.5 Output Diode Selection

In PWM operation, inductor current flows through the output diode approximately 50 ns during the dead time when one output MOSFET turns off the other turns on. In skip mode, the inductor current flows through the diode during the entire P-channel off time. The correct diode for both of these conditions is a 1A diode with a reverse voltage rating greater than V_{IN}. It must be a Schottky or ultrafast-recovery diode (t_R <100 ns) to minimize power dissipation from the diode's reverse-recovery charge.

5.6 Compensation

Compensation is provided by connecting a series RC load to the COMP pin. This creates a pole-zero pair in the regulator control loop, allowing the regulator to remain stable with enough low frequency loop-gain for good load and line regulation. At higher frequencies, the pole-zero reduces loop-gain to a level referred to as the mid-band gain. The midband gain is low enough so that the loop gain crosses 0 dB with sufficient phase margin. Typical values for the RC load are 4.7 nF to 10 nF for the capacitor and 5 kΩ to 20 kΩ for the resistor.

5.7 Printed Circuit Board Layout

A well designed PC board will prevent switching noise and ground bounce from interfering with the operation of the MIC2179. A good design takes into consideration component placement and routing of power traces.

The first thing to consider is the locations of the input capacitor, inductor, output diode, and output capacitor. The input capacitor must be placed very close to the VIN pin, the inductor and output diode very close to the SW pin, and the output capacitor near the inductor. These components pass large high-frequency current pulses, so they must use short, wide power traces. In addition, their ground pins and PGND are connected to a ground plane that is nearest the power supply ground bus.

The feedback resistors, RC compensation network, and BIAS pin bypass capacitor should be located close to their respective pins. To prevent ground bounce, their ground traces and SGND should not be in the path of switching currents returning to the power supply ground bus. SGND and PGND should be tied together by a ground plane that extends under the MIC2179.

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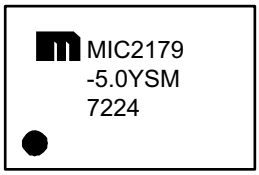
6.0 PACKAGING INFORMATION

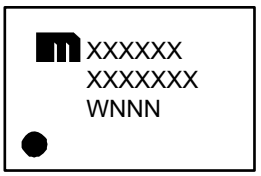
6.1 Package Marking Information

20-Lead Fixed SSOP*

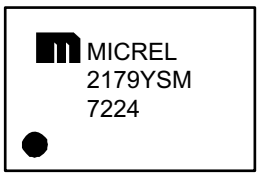
Example



20-Lead Adj. SSOP*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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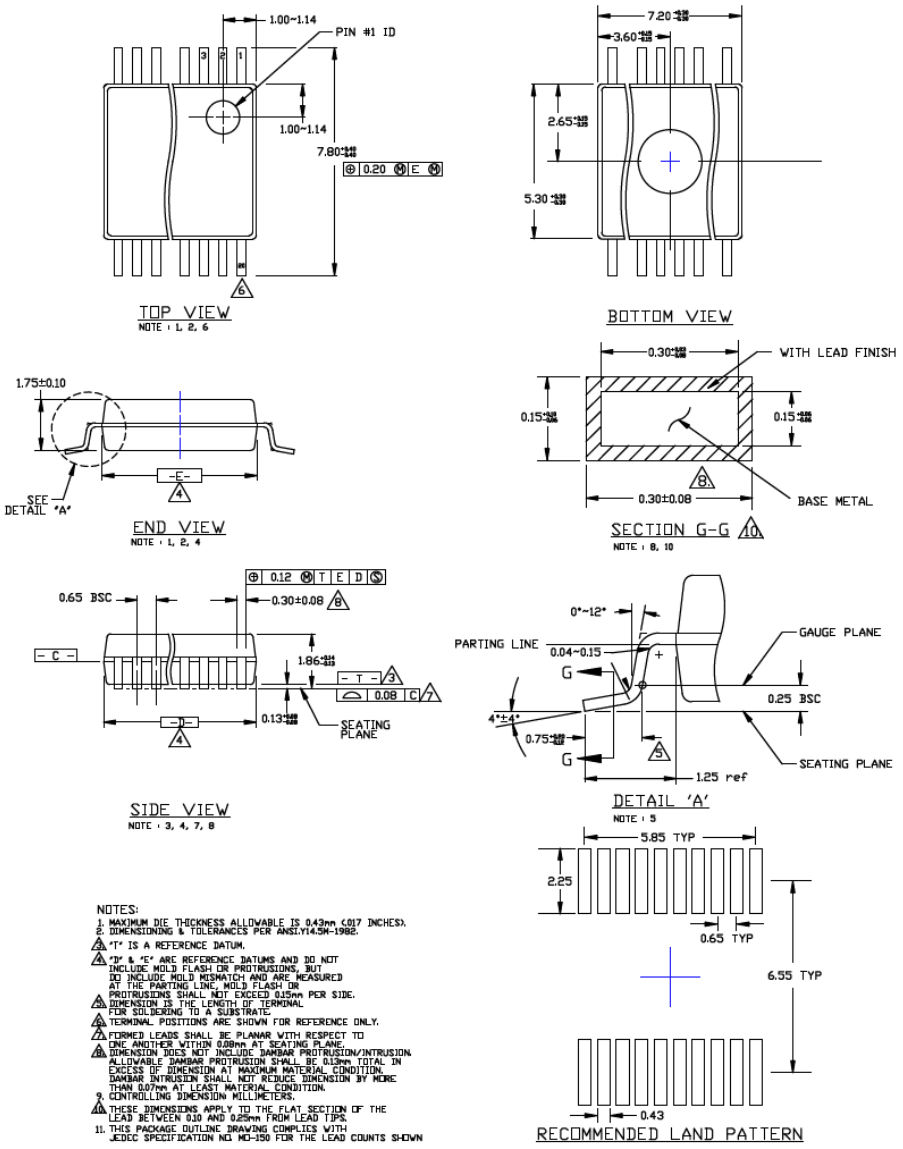
20-Lead SSOP Package Outline and Recommended Land Pattern

TITLE
20 LEAD SSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SSOP-20LD-PL-1	UNIT	MM



NOTES:
1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO: MO-150 FOR THE LEAD COUNTS SHOWN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision B (March 2021)

- Updated the Electrical Characteristics table.

Revision A (January 2020)

- Converted Micrel document MIC2179 to Microchip data sheet template DS20006284A.
- Minor grammatical text changes throughout.
- Multiple values unbolded in the Electrical Characteristics section.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X.X	X	XX	-XX
Part No.	Output Voltage	Junction Temp. Range	Package	Media Type

Device:	MIC2179:	1.5A Synchronous Buck Regulator
Output Voltage:	<blank> = Adjustable 3.3 = 3.3V 5.0 = 5.0V	
Junction Temperature Range:	Y =	–40°C to +85°C, RoHS-Compliant
Package:	SM =	20-Lead SSOP
Media Type:	<blank>= 67/Tube TR =	1,000/Reel

Examples:

a) MIC2179YSM: MIC2179, Adjustable Output Voltage, –40°C to +85°C Temperature Range, 20-Lead SSOP, 67/Tube

b) MIC2179YSM-TR: MIC2179, Adjustable Output Voltage, –40°C to +85°C Temperature Range, 20-Lead SSOP, 1,000/Reel

c) MIC2179-3.3YSM: MIC2179, 3.3V Output Voltage, –40°C to +85°C Temperature Range, 20-Lead SSOP, 67/Tube

d) MIC2179-3.3YSM-TR: MIC2179, 3.3V Output Voltage, –40°C to +85°C Temperature Range, 20-Lead SSOP, 1,000/Reel

e) MIC2179-5.0YSM: MIC2179, 5.0V Output Voltage, –40°C to +85°C Temperature Range, 20-Lead SSOP, 67/Tube

f) MIC2179-5.0YSM-TR: MIC2179, 5.0V Output Voltage, –40°C to +85°C Temperature Range, 20-Lead SSOP, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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