

# SN54AS882A, SN74AS882A 32-BIT LOOK-AHEAD CARRY GENERATORS

SDAS235 – D2661, DECEMBER 1982 – REVISED NOVEMBER 1985

- Directly Compatible With 'AS181B, 'AS1181, 'AS881B, and 'AS1881 ALUs
- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Capable of Anticipating the Carry Across a Group of Eight 4-Bit Binary Adders
- Cascadable to Perform Look-Ahead Across n-Bit Adders
- Typical Carry Time,  $C_n$  to Any  $C_{n+i}$ , is Less Than 6 ns
- Dependable Texas Instruments Quality and Reliability

## description

The 'AS882A is a high-speed look-ahead carry generator capable of anticipating the carry across a group of eight 4-bit adders permitting the designer to implement look-ahead for a 32-bit ALU with a single package or, by cascading 'AS882As, full look-ahead is possible across n-bit adders.

The SN54AS882A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS882A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### 'AS882A LOGIC EQUATIONS

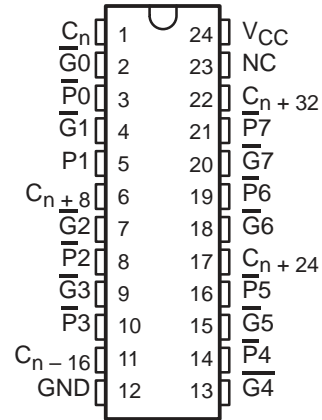
$$C_{n+8} = G1 + P1G0 + P1P0C_n$$

$$C_{n+16} = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C_n$$

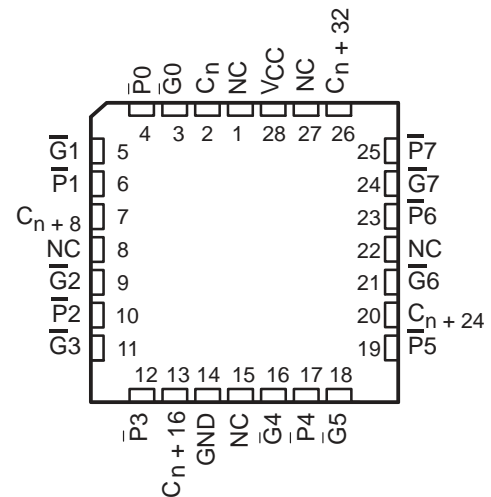
$$C_{n+24} = G5 + P5G4 + P5P4G3 + P5P4P3G2 + P5P4P3P2G1 + P5P4P3P2P1G0 + P5P4P3P2P1P0C_n$$

$$C_{n+32} = G7 + P7G6 + P7P6G5 + P7P6P5G4 + P7P6P5P4G3 + P7P6P5P4P3G2 + P7P6P5P4P3P2G1 + P7P6P5P4P3P2P1G0 + P7P6P5P4P3P2P1P0C_n$$

SN54AS882A . . . JT PACKAGE  
SN74AS882A . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54AS882A . . . FK PACKAGE  
SN74AS882A . . . DW OR NT PACKAGE  
(TOP VIEW)

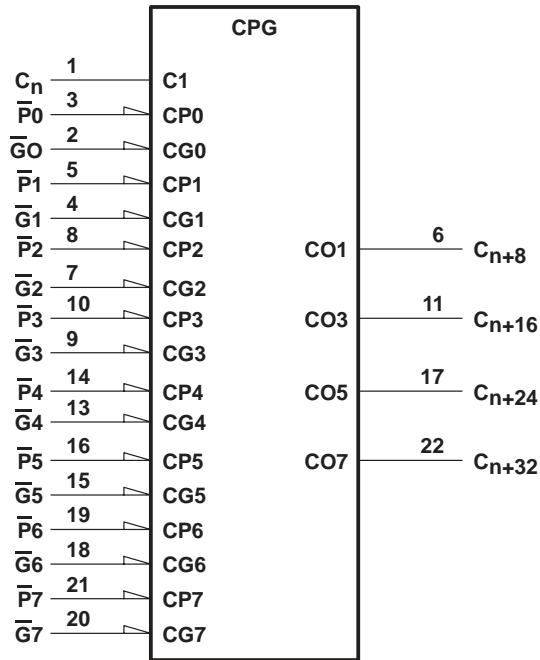


NC – No internal connection

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for DW, JT, and NT packages.

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**FUNCTION TABLE  
FOR  $C_n + 32$  OUTPUT**

INPUTS																	OUTPUT
G7	G6	G5	G4	G3	G2	G1	G0	P7	P6	P5	P4	P3	P2	P1	P0	$C_n$	$C_n + 32$
L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	L	L	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	L	L	L	L	X	X	X	X	X	H
X	X	X	X	X	L	X	X	L	L	L	L	L	X	X	X	X	H
X	X	X	X	X	X	L	X	L	L	L	L	L	L	X	X	X	H
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	H	H
All other combinations																	L

**FUNCTION TABLE  
FOR  $C_n + 24$  OUTPUT**

INPUTS													OUTPUT
G5	G4	G3	G2	G1	G0	P5	P4	P3	P2	P1	P0	$C_n$	$C_n + 24$
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	L	L	X	X	X	X	X	H
X	X	X	L	X	X	L	L	L	X	X	X	X	H
X	X	X	X	L	X	L	L	L	L	X	X	X	H
X	X	X	X	X	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	L	L	L	L	L	L	H	H
All other combinations													L

### Function Tables

**FOR  $C_n + 16$  OUTPUT**

INPUTS									OUTPUT
G3	G2	G1	G0	P3	P2	P1	P0	$C_n$	$C_n + 16$
L	X	X	X	X	X	X	X	X	H
X	L	X	X	L	X	X	X	X	H
X	X	L	X	L	L	X	X	X	H
X	X	X	L	L	L	L	X	X	H
X	X	X	X	L	L	L	L	H	H
All other combinations									L

**FOR  $C_n + 8$  OUTPUT**

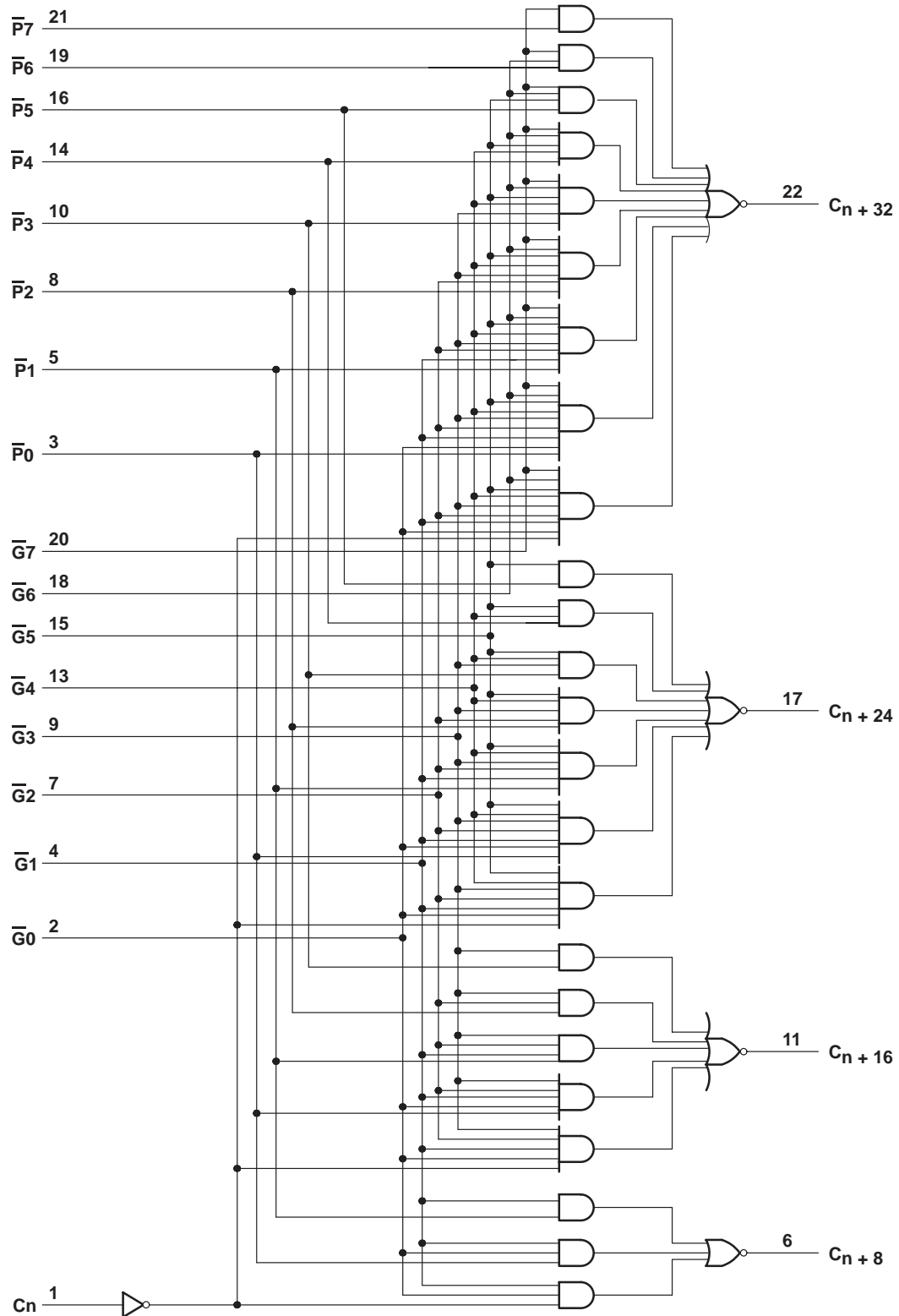
INPUTS					OUTPUT
G1	G0	P1	P0	$C_n$	$C_n + 8$
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

Any inputs not shown in a given table are irrelevant with respect to that output.

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## logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS882A			SN74AS882A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA	V <sub>CC</sub> -2			V <sub>CC</sub> -2			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA		0.3	0.5		0.3	0.5	V
I <sub>I</sub>	C <sub>n</sub> , P 0, P1	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V				0.4	0.4
	G0, G6						0.8	0.8
	G1, G2, G4						1.2	1.2
	G3, G5						1.5	1.5
	G7						0.9	0.9
	P2, P3						0.3	0.3
	P4, P5						0.2	0.2
	P6, P7						0.1	0.1
I <sub>IH</sub>	C <sub>n</sub> , P 0, P1	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V				80	80
	G0, G6						160	160
	G1, G2, G4						240	240
	G3, G5						300	300
	G7						180	180
	P2, P3						60	60
	P4, P5						40	40
	P6, P7						20	20
I <sub>IL</sub>	C <sub>n</sub> , P 0, P1	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V				-2	-2
	G0, G6						-4	-4
	G1, G2, G4						-6	-6
	G3, G5						-7.5	-7.5
	G7						-4.5	-4.5
	P2, P3						-1.5	-1.5
	P4, P5						-1	-1
	P6, P7						-0.5	-0.5
I <sub>O</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V		-30	-130		-30	-30	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V		44	70		44	70	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.



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## switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX				UNIT
			SN54AS882A		SN74AS882A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	C <sub>n</sub>	Any output	2	10	2	9	ns
t <sub>PHL</sub>			3	15	3	14	
t <sub>PLH</sub>	P or G	C <sub>n</sub> + 8	2	8	2	7	
t <sub>PHL</sub>			2	8	2	7	
t <sub>PLH</sub>	P or G	C <sub>n</sub> + 16	2	8	2	7	
t <sub>PHL</sub>			2	8	2	7	
t <sub>PLH</sub>	P or G	C <sub>n</sub> + 24	2	8	2	7	
t <sub>PHL</sub>			2	11	2	10	
t <sub>PLH</sub>	P or G	C <sub>n</sub> + 32	1.5	9	2	8	
t <sub>PHL</sub>			2	13	2	12	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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## TYPICAL APPLICATION DATA

The application given in Figure 1 illustrates how the 'AS882A can implement look-ahead carry for a 32-bit ALU (in this case, the popular 'AS881A) with a single package. Typical carry times shown are derived using the standard Advanced Schottky load circuit.

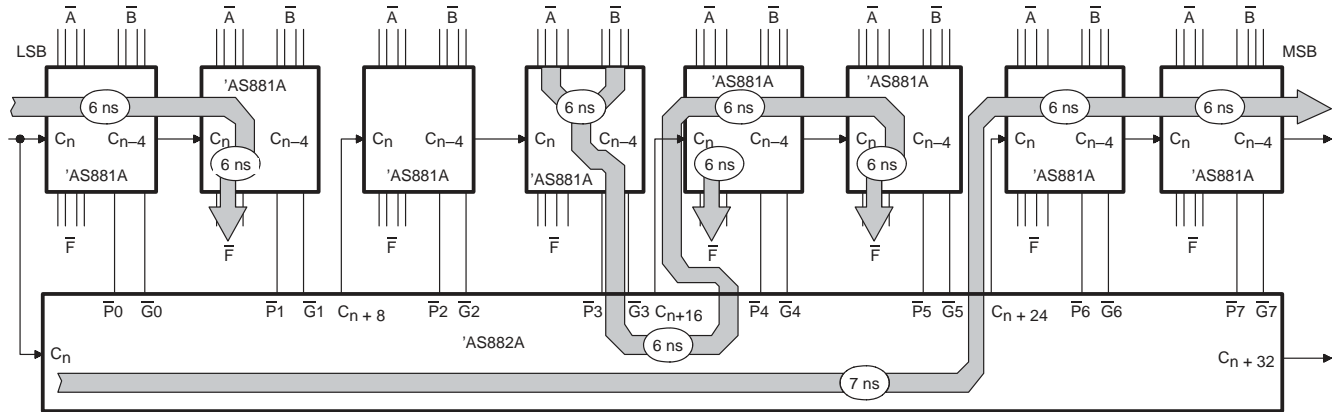


Figure 1

Likewise, Figure 2 illustrates the same 32-bit ALU using two 'AS882s. This shows the worst-case delay from LSB to MSB to be 19 ns as opposed to 25 ns in Figure 1.

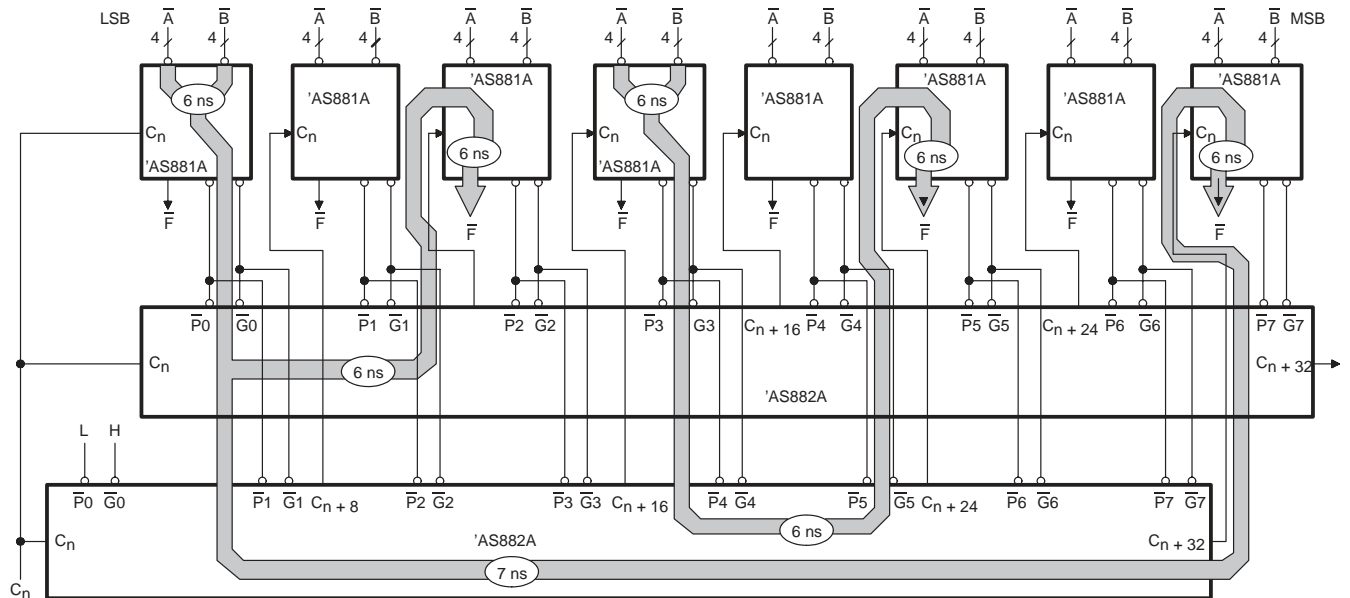


Figure 2



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