# 30V, N-Channel NexFET™ Power MOSFETs

**Check for Samples: CSD17510Q5A**

## FEATURES

- **Ultralow $Q_g$ and $Q_{gd}$**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm × 6-mm Plastic Package**

## APPLICATIONS

- **Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems**
- **Optimized for Control and Synchronous FET Applications**

## DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

## PRODUCT SUMMARY

| | | | | |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 30 | | V |
| $Q_g$ | Gate Charge Total (4.5V) | 6.4 | | nC |
| $Q_{gd}$ | Gate Charge Gate to Drain | 1.9 | | nC |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 4.5V | 5.4 | mΩ |
| | | $V_{GS}$ = 10V | 4.1 | mΩ |
| $V_{GS(th)}$ | Threshold Voltage | 1.5 | | V |

## ORDERING INFORMATION

| Device | Package | Media | Qty | Ship |
|---|---|---|---|---|
| CSD17510Q5A | SON 5-mm × 6-mm Plastic Package | 13-Inch Reel | 2500 | Tape and Reel |

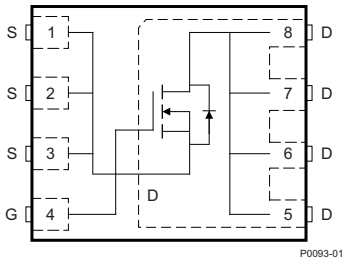
## ABSOLUTE MAXIMUM RATINGS

| $T_A$ = 25°C unless otherwise stated | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Continuous Drain Current, $T_C$ = 25°C | 55 | A |
| | Continuous Drain Current(1) | 20 | A |
| $I_{DM}$ | Pulsed Drain Current, $T_A$ = 25°C(2) | 129 | A |
| $P_D$ | Power Dissipation(1) | 3 | W |
| $T_J$, $T_{STG}$ | Operating Junction and Storage Temperature Range | –55 to 150 | °C |
| $E_{AS}$ | Avalanche Energy, single pulse $I_D$ = 54A, L = 0.1mH, $R_G$ = 25Ω | 146 | mJ |

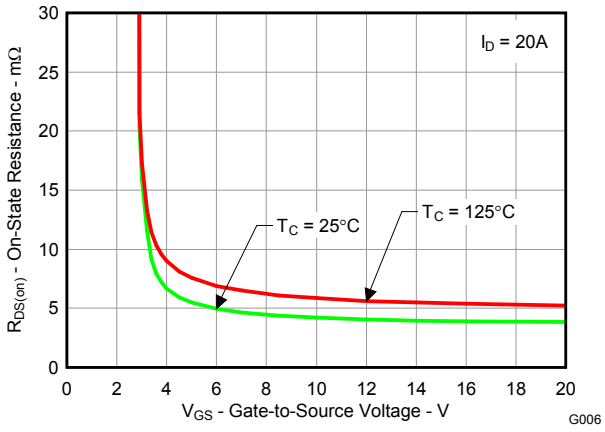
(1) Typical $R_{\theta JA}$ = 41°C/W on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300µs, duty cycle ≤2%

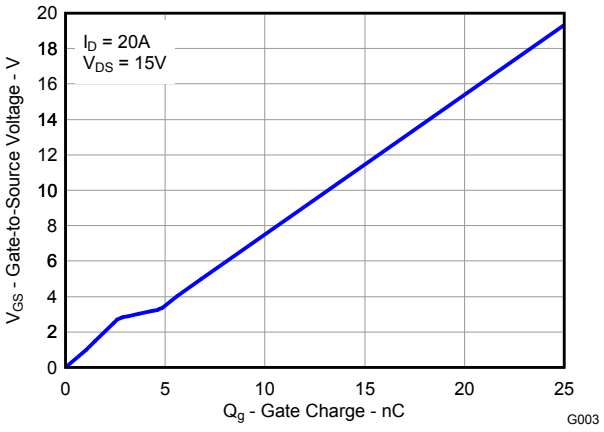
**Top View**




**$R_{DS(on)}$ vs $V_{GS}$**




**GATE CHARGE**




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C unless otherwise stated)

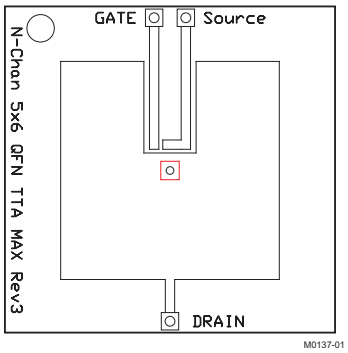
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Voltage | $V_{GS}$ = 0V, $I_{DS}$ = 250μA | 30 | | | V |
| $I_{DSS}$ | Drain to Source Leakage Current | $V_{GS}$ = 0V, $V_{DS}$ = 24V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{DS}$ = 0V, $V_{GS}$ = 20V | | | 100 | nA |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250μA | 1 | 1.5 | 2.1 | V |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 4.5V, $I_{DS}$ = 20A | | 5.4 | 7.3 | mΩ |
| | | $V_{GS}$ = 10V, $I_{DS}$ = 20A | | 4.1 | 5.2 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 15V, $I_{DS}$ = 20A | | 59 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 15V, f = 1MHz | | 960 | 1250 | pF |
| $C_{oss}$ | Output Capacitance | | | 630 | 820 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 51 | 66 | pF |
| $R_G$ | Series Gate Resistance | | | 0.85 | 1.7 | Ω |
| $Q_g$ | Gate Charge Total (4.5V) | $V_{DS}$ = 15V, $I_{DS}$ = 20A | | 6.4 | 8.3 | nC |
| $Q_{gd}$ | Gate Charge Gate to Drain | | | 1.9 | | nC |
| $Q_{gs}$ | Gate Charge Gate to Source | | | 2.7 | | nC |
| $Q_{g(th)}$ | Gate Charge at Vth | | | 1.5 | | nC |
| $Q_{oss}$ | Output Charge | $V_{DS}$ = 13.5V, $V_{GS}$ = 0V | | 16 | | nC |
| $t_{d(on)}$ | Turn On Delay Time | $V_{DS}$ = 15V, $V_{GS}$ = 4.5V, $I_{DS}$ = 20A,$R_G$ = 2Ω | | 7 | | ns |
| $t_r$ | Rise Time | | | 11 | | ns |
| $t_{d(off)}$ | Turn Off Delay Time | | | 9 | | ns |
| $t_f$ | Fall Time | | | 4.1 | | ns |
| **Diode Characteristics** | | | | | | |
| $V_{SD}$ | Diode Forward Voltage | $I_{SD}$ = 20A, $V_{GS}$ = 0V | | 0.85 | 1 | V |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DD}$= 13.5V, $I_F$ = 20A, di/dt = 300A/μs | | 25 | | nC |
| $t_{rr}$ | Reverse Recovery Time | | | 24 | | ns |

## THERMAL CHARACTERISTICS

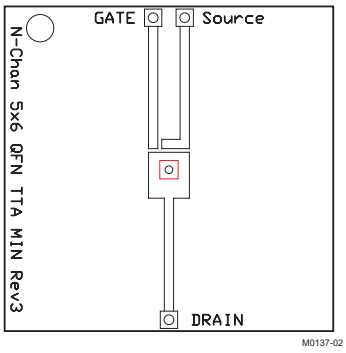
($T_A$ = 25°C unless otherwise stated)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case(1) | | | 1.6 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient(1)(2) | | | 51 | °C/W |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu.




Max $R_{\theta JA}$ = 51°C/W when mounted on 1 inch$^2$ (6.45 cm$^2$) of 2-oz. (0.071-mm thick) Cu.




Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

## TYPICAL MOSFET CHARACTERISTICS

($T_A$ = 25°C unless otherwise stated)

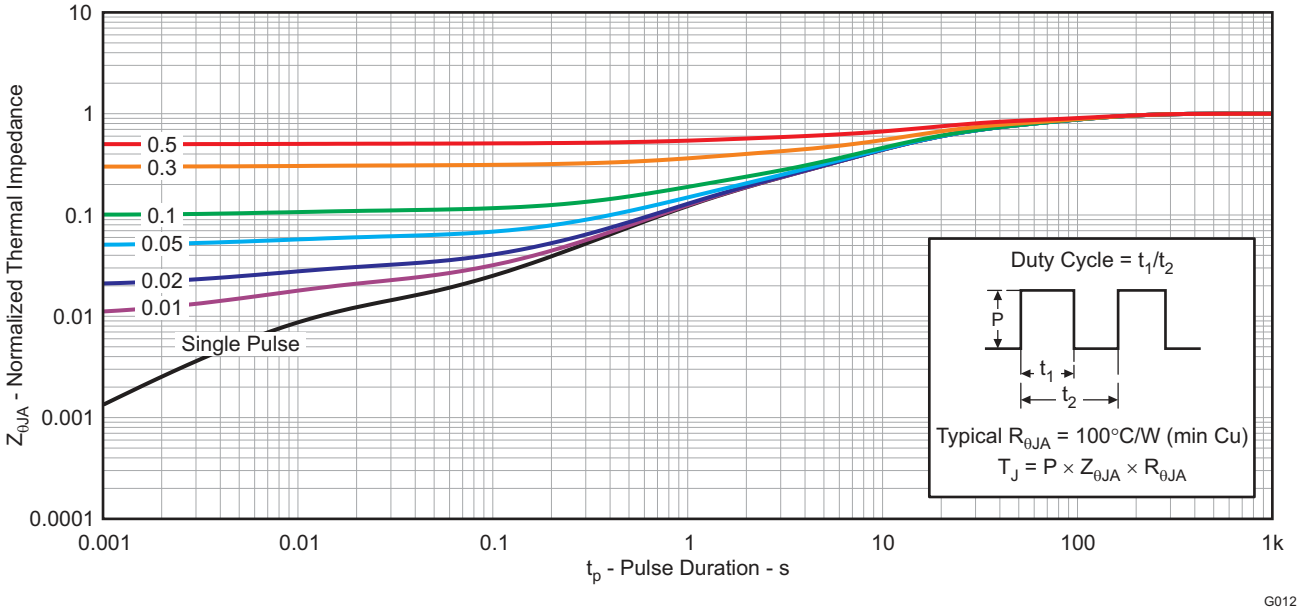



**Figure 1. Transient Thermal Impedance**

## TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A$ = 25°C unless otherwise stated)

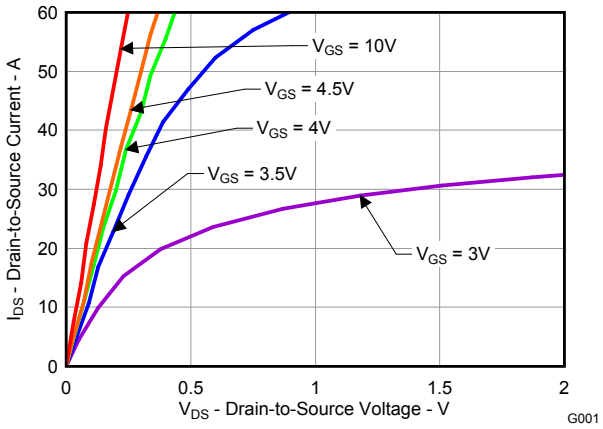



**Figure 2. Saturation Characteristics**

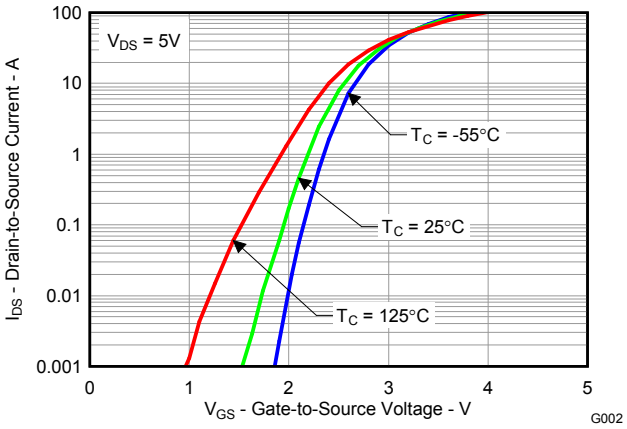



**Figure 3. Transfer Characteristics**

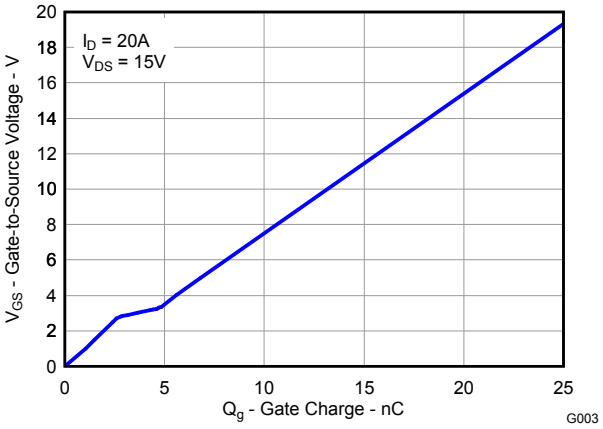



**Figure 4. Gate Charge**

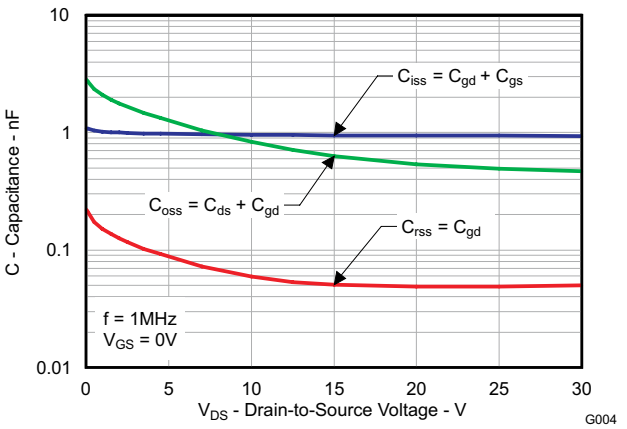



**Figure 5. Capacitance**

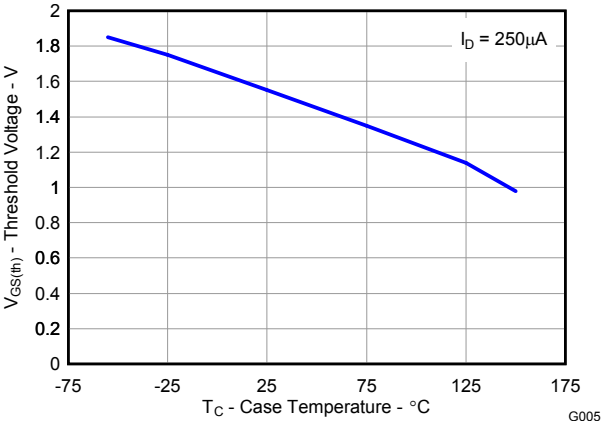



**Figure 6. Threshold Voltage vs. Temperature**

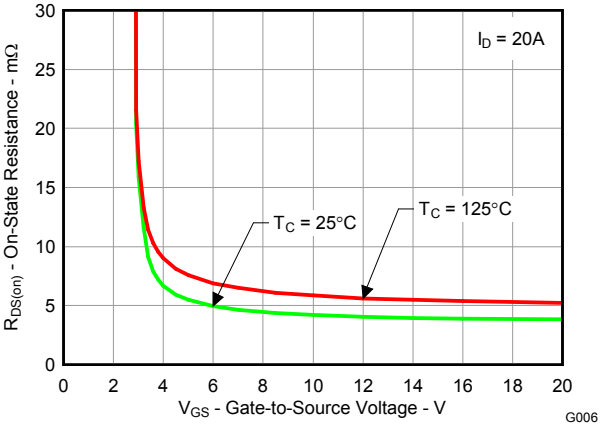



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

## TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A$ = 25°C unless otherwise stated)

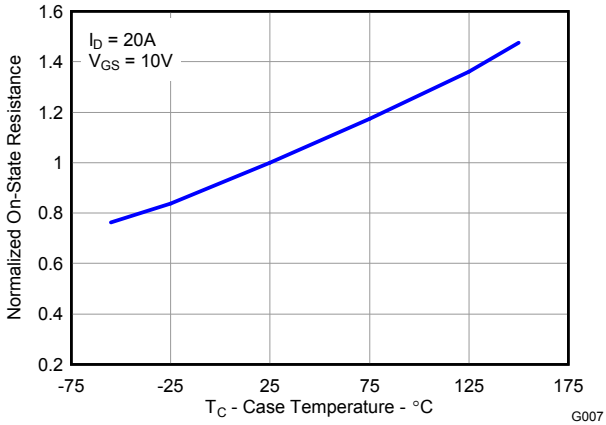



**Figure 8. Normalized On-State Resistance vs. Temperature**

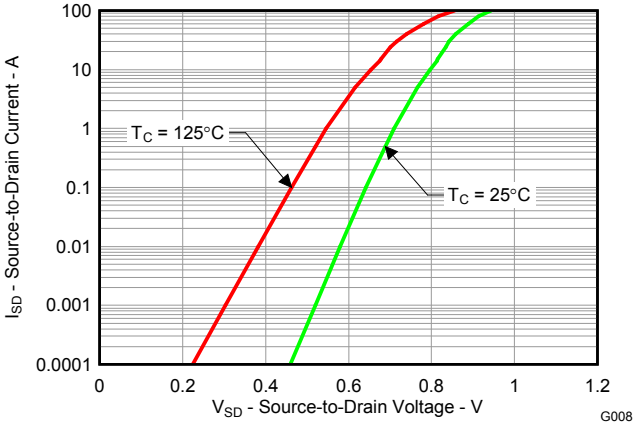



**Figure 9. Typical Diode Forward Voltage**

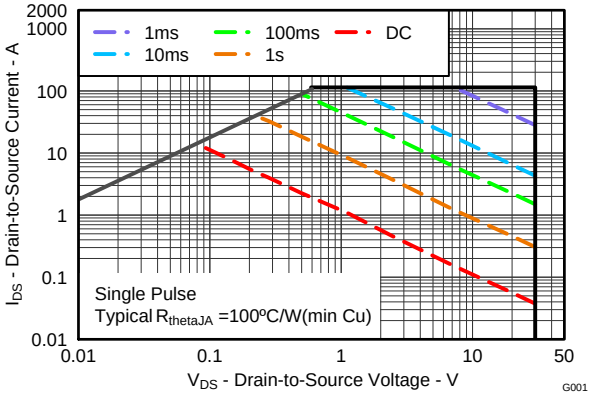



**Figure 10. Maximum Safe Operating Area**

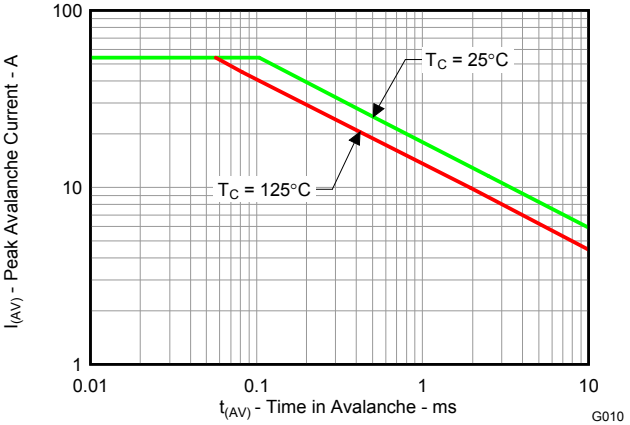



**Figure 11. Single Pulse Unclamped Inductive Switching**

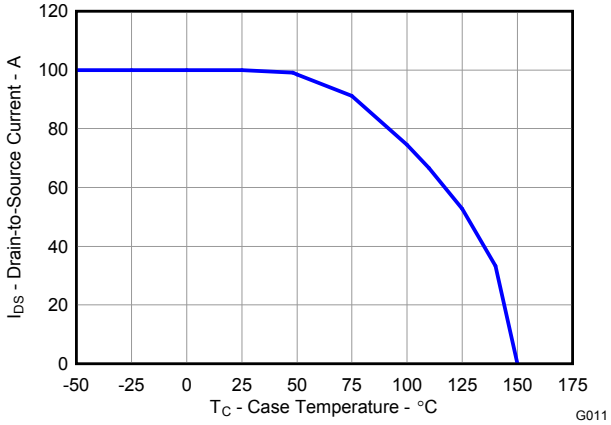
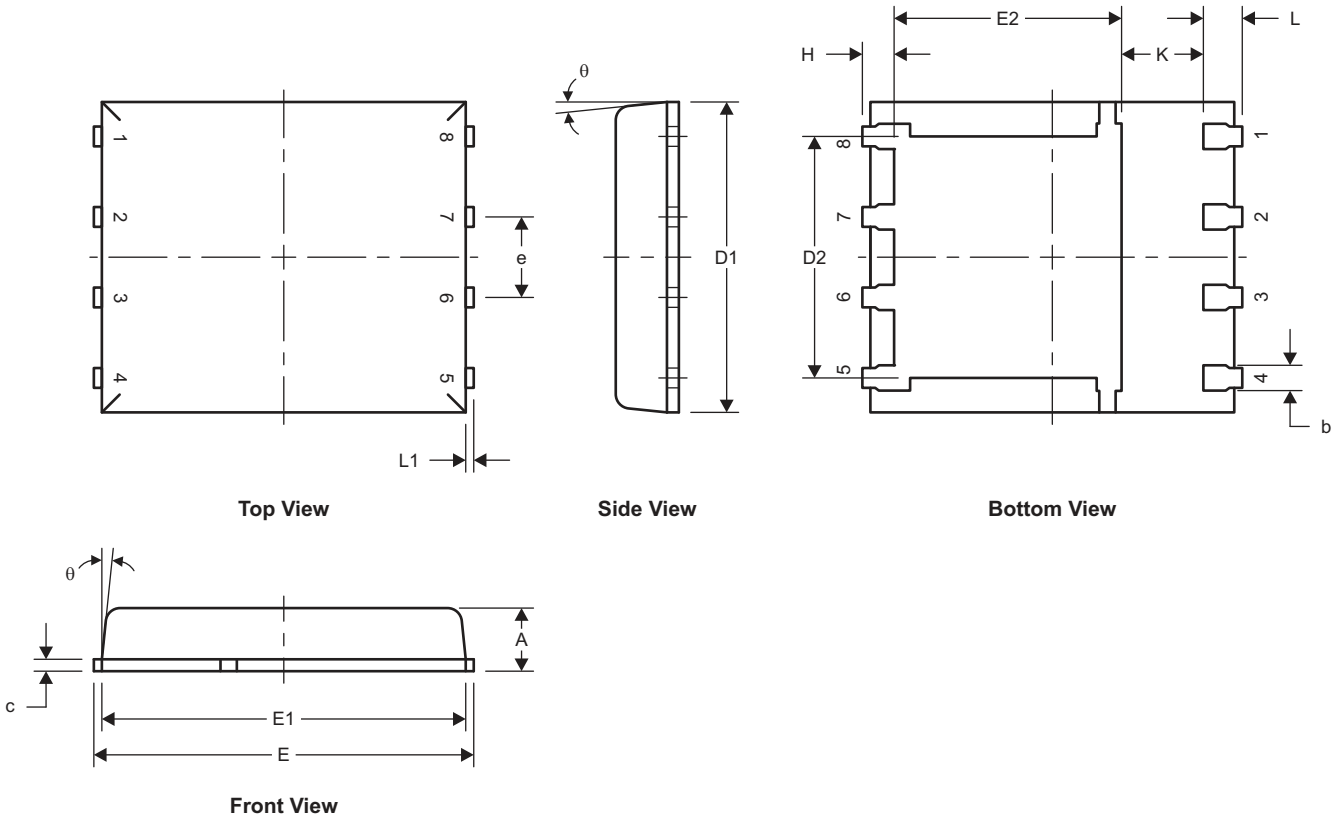



**Figure 12. Maximum Drain Current vs. Temperature**

## MECHANICAL DATA

### Q5A Package Dimensions



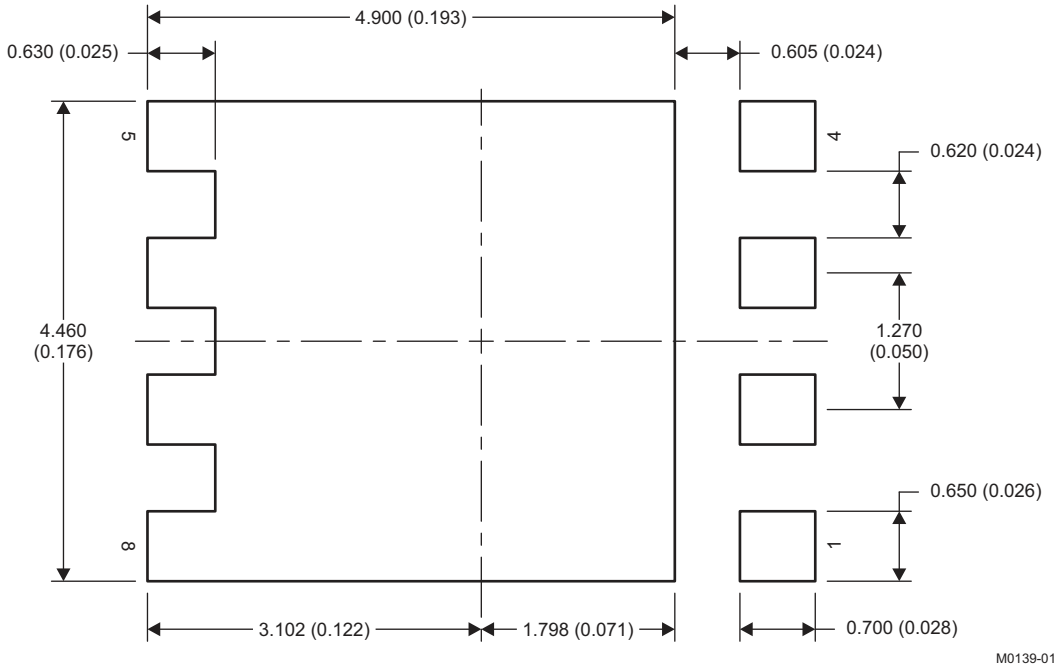

**Top View** **Side View** **Bottom View**

**Front View**

M0135-01

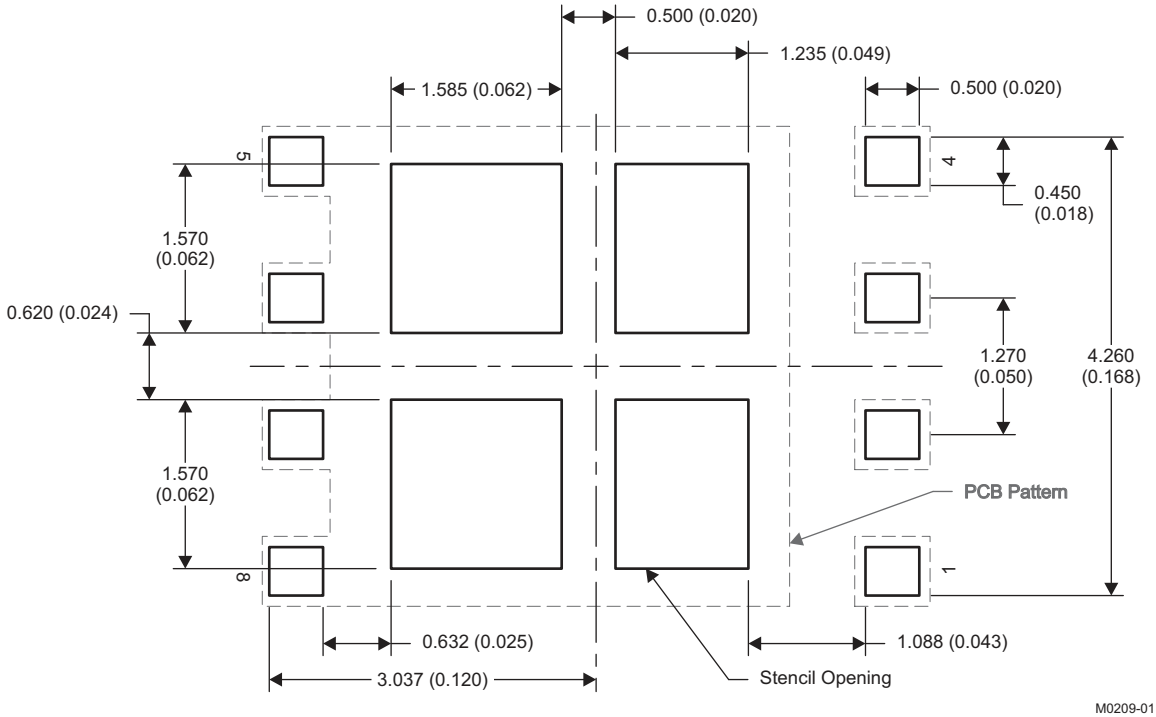
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.20 | 0.25 | 0.34 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 4.02 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.38 | 3.58 | 3.78 |
| e | 1.17 | 1.27 | 1.37 |
| H | 0.41 | 0.56 | 0.71 |
| K | 1.10 | | |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| θ | 0° | | 12° |

## Recommended PCB Pattern




NOTE: Dimensions are in mm (inches).

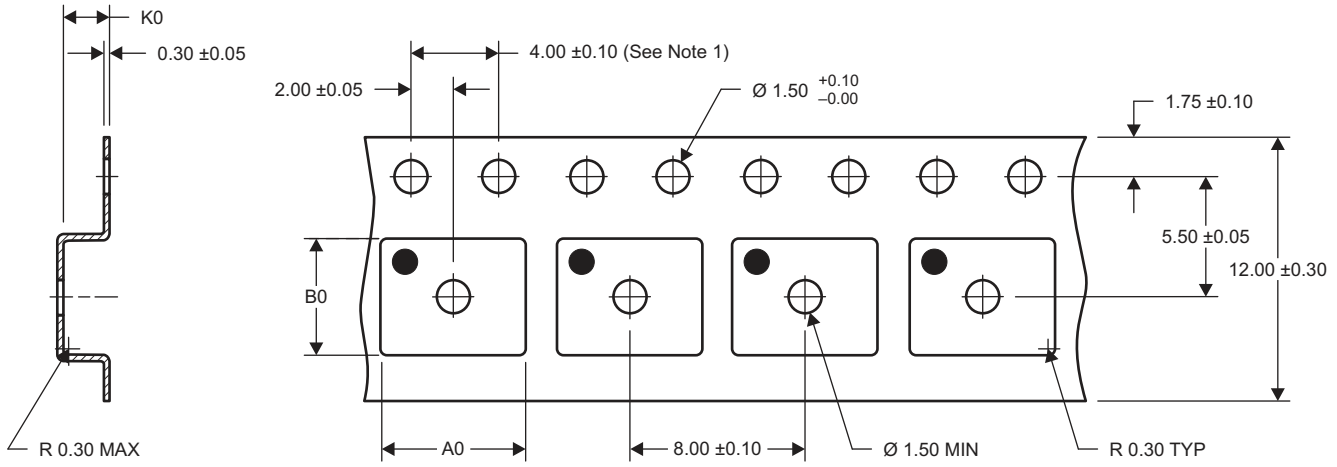
## Stencil Recommendation




NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

## Q5A Tape and Reel Information




A0 = 6.50 ±0.10
B0 = 5.30 ±0.10
K0 = 1.40 ±0.10

M0138-01

NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

## REVISION HISTORY

**Changes from Original (July 2010) to Revision A** **Page**

- Changed the Y axis scale for Figure 5 ..... 4

**Changes from Revision A (August 2010) to Revision B** **Page**

- Changed $R_{DS(on)}$ Test Conditions From $V_{GS}$ = 8V To: $V_{GS}$ = 10V ..... 2

**Changes from Revision B (September 2010) to Revision C** **Page**

- Absolute Maximum Ratings, changed the $E_{AS}$ value from 45 to 146 mJ ..... 1

**Changes from Revision C (September 2010) to Revision D** **Page**

- Added the Stencil Recommendation section ..... 7

**Changes from Revision D (November 2010) to Revision E** **Page**

- Changed $V_{GS}$ in the Abs Max Ratings table From: +20/-12V To: ±20V ..... 1
- Changed from +20/-12V to 20V ..... 2

**Changes from Revision E (July 2011) to Revision F** **Page**

- Changed the $I_D$ Continuous Drain Current, $T_C$ = 25°C value From: 100 A To: 55 A. ..... 1
- Changed Figure 10 ..... 5

**Changes from Revision F (October 2011) to Revision G** **Page**

- Changed Figure 10 ..... 5

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD17510Q5A | ACTIVE | VSONP | DQJ | 8 | 2500 | RoHS-Exempt & Green | SN | Level-1-260C-UNLIM | -55 to 150 | CSD17510 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265