

RAIL-TO-RAIL CMOS OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD1704A/ALD1704B/ALD1704/ALD1704G is a CMOS monolithic operational amplifier with MOSFET input that has rail-to-rail input and output voltage ranges. The input voltage range and output voltage range are very close to the positive and negative power supply voltages. Typically the input voltage can be beyond positive power supply voltage V+, or the negative power supply voltage V- by up to 300mV. The output voltage swings to within 60mV of either positive or negative power supply voltages at rated load.

This device is designed as an alternative to the popular JFET input operational amplifiers in applications where lower operating voltages, such as 9V battery or ±3.25V to ±5V power supplies are being used. It offers high slew rate of 5V/μs at low operating power of 30mW. Since the ALD1704A/ALD1704B/ALD1704/ALD1704G is designed and manufactured with Advanced Linear Devices' standard enhanced ACMOS silicon gate CMOS process, it also offers low unit cost and exceptional reliability.

The rail-to-rail input and output feature of the ALD1704A/ALD1704B/ALD1704/ALD1704G allows a lower operating supply voltage for a given signal voltage range and allows numerous analog serial stages to be implemented without losing operating voltage margin. The output stage is designed to drive up to 10mA into 400pF capacitive and 1.5KΩ resistive loads at unity gain and up to 4000 pF at a gain of 5. Short circuit protection to either ground or the power supply rails is at approximately 15mA clamp current. Due to complementary output stage design, the output can both source and sink 10mA into a load with symmetrical drive and is ideally suited for applications where push-pull voltage drive is desired.

The offset voltage is trimmed on-chip to eliminate the need for external nulling in many applications. For precision applications, the output is designed to settle to 0.1% in 2μs. For large signal buffer applications, the operational amplifier can function as an ultra high input impedance voltage follower/buffer that allows input and output voltage swings from positive to negative supply voltages. This feature is intended to greatly simplify systems design and eliminate higher voltage power supplies in many applications. Additionally, robust design and rigorous screening make this device especially suitable for operation in temperature-extreme environments and rugged conditions.

FEATURES

- Rail-to-rail input and output voltage ranges
- 5.0V/μs slew rate
- Output settles to 2mV of supply rails
- High capacitive load capability -- up to 4000pF
- Symmetrical push-pull output drives
- No frequency compensation required -- unity gain stable
- Extremely low input bias currents -- 1.0pA typical (20pAMax)
- Ideal for high source impedance applications
- High voltage gain -- typically 150V/mV
- Output short circuit protected
- Unity gain bandwidth of 2.1MHz
- Suitable for rugged, temperature-extreme environments

APPLICATIONS

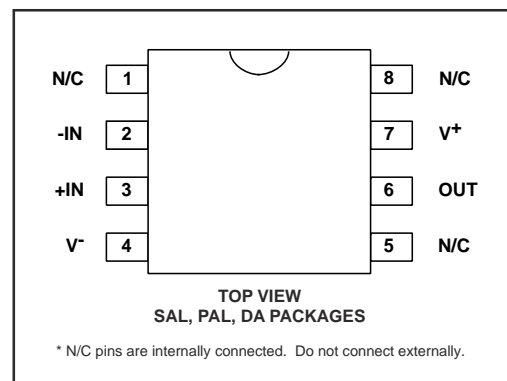
- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter
- Coaxial cable driver
- Capacitive sensor amplifier
- Piezoelectric transducer amplifier

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to 125°C
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD1704ASAL	ALD1704APAL	ALD1704ADA
ALD1704BSAL	ALD1704BPAL	ALD17041BDA
ALD1704SAL	ALD1704PAL	ALD1704DA
ALD1704GSAL	ALD1704GPAL	ALD1704GDA

* Contact factory for leaded (non-RoHS) or extended high/low temperature versions.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply voltage, V+	_____	10.6V
Differential input voltage range	_____	-0.3V to V+ +0.3V
Power dissipation	_____	600 mW
Operating temperature range	SAL, PAL packages _____	0°C to +70°C
	DA package _____	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C
Lead temperature, 10 seconds	_____	+260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

T_A = 25°C V_S = ±5.0V unless otherwise specified

Parameter	Symbol	1704A			1704B			1704			1704G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Supply Voltage	V _S V+	±3.25 6.5		±5.0 10.0	±3.25 6.5		±5.0 10.0	±3.25 6.5		±5.0 10.0	±3.25 6.5		±5.0 10.0	V V	Dual Supply Single Supply
Input Offset Voltage	V _{OS}			0.9 1.7			2.0 2.8			4.5 5.3			10.0 11.0	mV mV	R _S ≤ 100KΩ 0°C ≤ T _A ≤ +70°C
Input Offset Current	I _{OS}		1.0	15 240		1.0	15 240		1.0	15 240		1.0	25 240	pA pA	T _A = 25°C 0°C ≤ T _A ≤ +70°C
Input Bias Current	I _B		1.0	20 300		1.0	20 300		1.0	20 300		1.0	30 300	pA pA	T _A = 25°C 0°C ≤ T _A ≤ +70°C
Input Voltage Range	V _{IR}	-5.3		+5.3	-5.3		+5.3	-5.3		+5.3		±5.0		V	
Input Resistance	R _{IN}		10 ¹²			10 ¹²			10 ¹²			10 ¹²		Ω	
Input Offset Voltage Drift	TCV _{OS}		5			5			5			7		μV/°C	R _S ≤ 100KΩ
Power Supply Rejection Ratio	PSRR	70	80		65	80		65	80		60	80		dB	R _S ≤ 100KΩ 0°C ≤ T _A ≤ +70°C
Common Mode Rejection Ratio	CMRR	70	83		65	83		65	83		60	83		dB	R _S ≤ 100KΩ 0°C ≤ T _A ≤ +70°C
Large Signal Voltage Gain	A _V	50 40	150 150		50 40	150 150		50 40	150 150		32 20	150 150		V/mV V/mV V/mV	R _L = 10KΩ No Load 0°C ≤ T _A ≤ +70°C
Output Voltage Range	V _O low V _O high	4.90	-4.96 4.95	-4.90	4.90	-4.96 4.95	-4.90	4.90	-4.96 4.95	-4.90	4.90	-4.96 4.95	-4.90	V	R _L = 10KΩ 0°C ≤ T _A ≤ +70°C
	V _O low V _O high	4.99	-4.998 4.998	-4.99	4.99	-4.998 4.998	-4.99	4.99	-4.998 4.998	-4.99	4.99	-4.998 4.998	-4.99	V	R _L = 1MΩ 0°C ≤ T _A ≤ +70°C
Output Short Circuit Current	I _{SC}		15			15			15			15		mA	
Supply Current	I _S		3.0	4.5		3.0	4.5		3.0	4.5		3.0	5.0	mA	V _{IN} = 0V No Load
Power Dissipation	P _D		30	45		30	45		30	45		30	50	mW	V _S = ±5.0 No Load
Input Capacitance	C _{IN}		1			1			1			1		pF	
Bandwidth	B _W		2.1			2.1			2.1			2.1		MHz	
Slew Rate	S _R		5.0			5.0			5.0			5.0		V/μs	A _V = +1 R _L = 2.0KΩ
Rise time	t _r		0.1			0.1			0.1			0.1		μs	R _L = 2.0KΩ
Overshoot Factor			15			15			15			15		%	R _L = 2.0KΩ C _L = 100pF

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

$T_A = 25^\circ\text{C}$ $V_S = \pm 5.0\text{V}$ unless otherwise specified

Parameter	Symbol	1704A			1704B			1704			1704G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Maximum Load Capacitance	C_L		400 4000			400 4000				400 4000			400 4000	pF pF	Gain = 1 Gain = 5
Input Noise Voltage	e_n		26			26				26			26	nV/ $\sqrt{\text{Hz}}$	f = 1KHZ
Input Current Noise	i_n		0.6			0.6				0.6			0.6	fA/ $\sqrt{\text{Hz}}$	f = 10HZ
Settling Time	t_s		5.0 2.0			5.0 2.0				5.0 2.0			5.0 2.0	μs μs	0.01% 0.1% $A_V = -1$ $R_L = 5\text{K}\Omega$ $C_L = 50\text{pF}$

$V_S = \pm 5.0\text{V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ unless otherwise specified

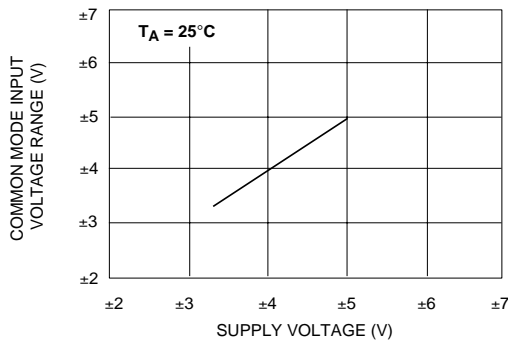
Parameter	Symbol	1704ADA			1704BDA			1704DA			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V_{OS}			2.0			4.0			7.0	mV	$R_S \leq 100\text{K}\Omega$
Input Offset Current	I_{OS}			8.0			8.0			8.0	nA	
Input Bias Current	I_B			10.0			10.0			10.0	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		60	75		dB	$R_S \leq 100\text{K}\Omega$
Common Mode Rejection Ratio	CMRR	60	83		60	83		60	83		dB	$R_S \leq 100\text{K}\Omega$
Large Signal Voltage Gain	A_V	30	125		30	125		30	125		V/mV	$R_L = 10\text{K}\Omega$
Output Voltage Range	$V_{O\text{ low}}$ $V_{O\text{ high}}$		-4.9 4.8	-4.8		-4.9 4.8	-4.8		-4.9 4.8	-4.8	V V	$R_L = 10\text{K}\Omega$ $R_L = 10\text{K}\Omega$

Design & Operating Notes:

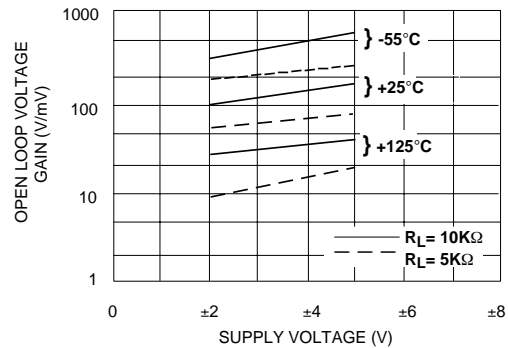
- The ALD1704A/ALD1704B/ALD1704/ALD1704G CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. The ALD1704A/ALD1704B/ALD1704/ALD1704G is internally compensated for unity gain stability using a novel scheme that produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency. A unity gain buffer using the ALD1704A/ALD1704B/ALD1704/ALD1704G will typically drive 400pF of external load capacitance without stability problems. In the inverting unity gain configuration, it can drive up to 800pF of load capacitance. Compared to other CMOS operational amplifiers, the ALD1704A/ALD1704B/ALD1704/ALD1704G has shown itself to be more resistant to parasitic oscillations.
- The ALD1704A/ALD1704B/ALD1704/ALD1704G has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V above the negative supply voltage. Since offset voltage trimming on the ALD1704A/ALD1704B/ALD1704/ALD1704G is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2 (10V operation), where the common mode voltage does not make excursions below this switching point.
- The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. For applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.
- The output stage consists of symmetrical class AB complementary output drivers, capable of driving a low resistance load with up to 10mA source current and 10mA sink current. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail-to-rail input and output feature, makes the ALD1704A/ALD1704B/ALD1704/ALD1704G an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.
- The ALD1704A/ALD1704B/ALD1704/ALD1704G operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.

TYPICAL PERFORMANCE CHARACTERISTICS

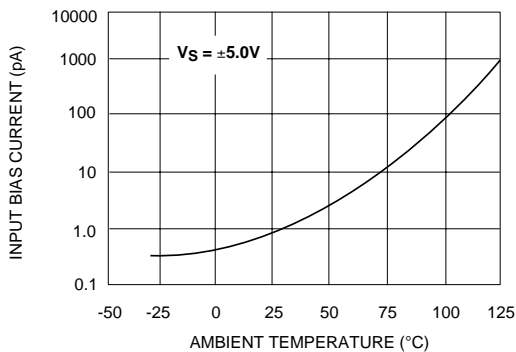
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



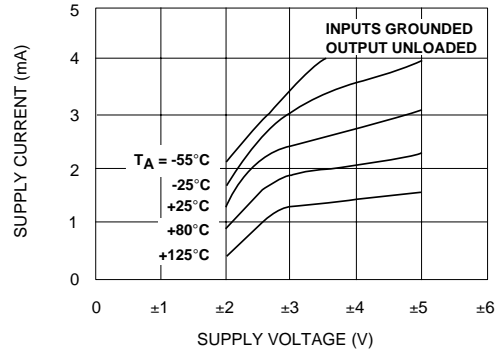
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



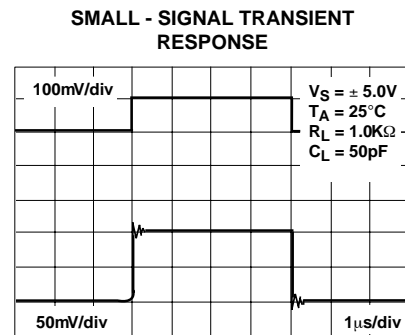
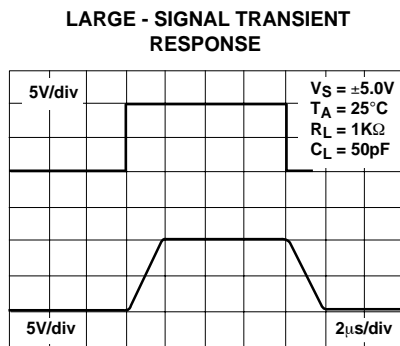
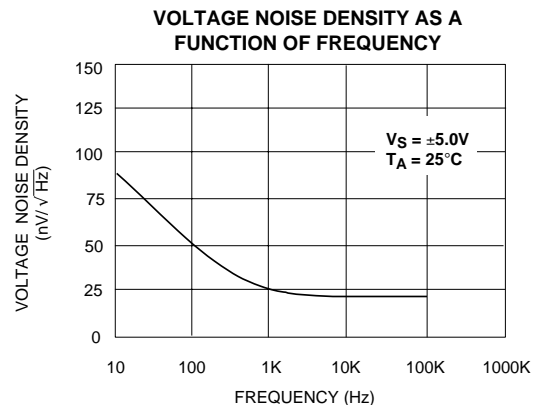
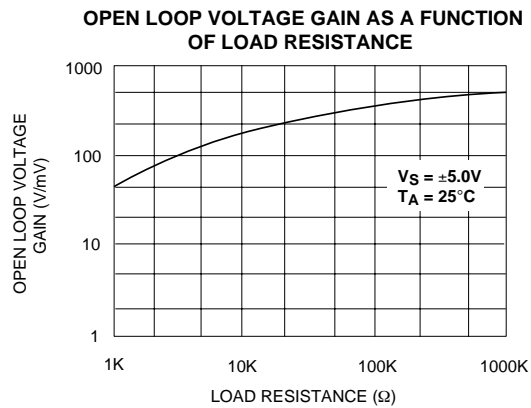
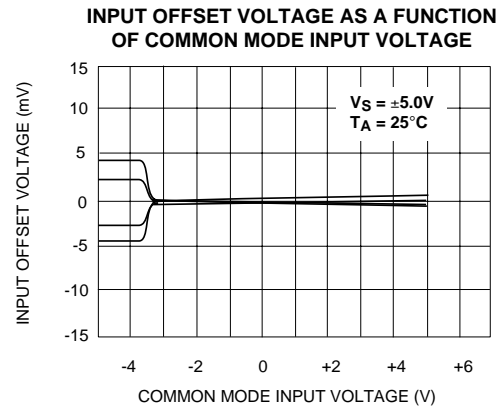
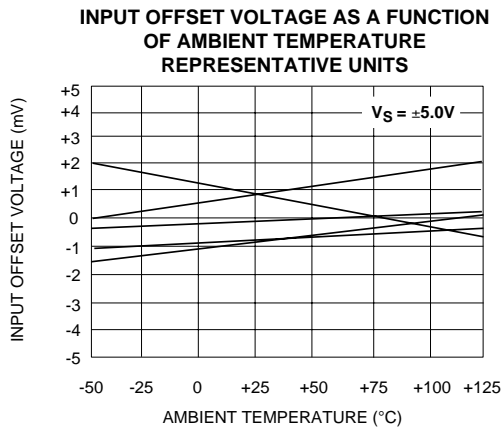
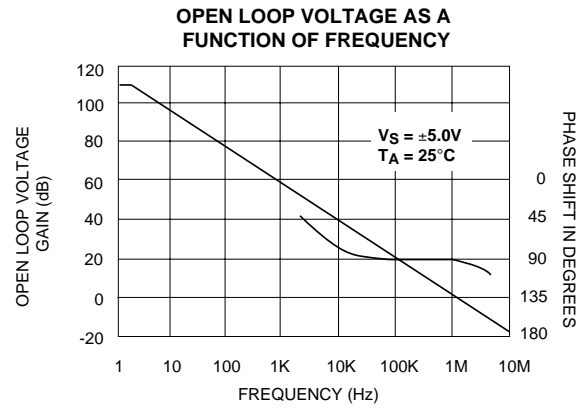
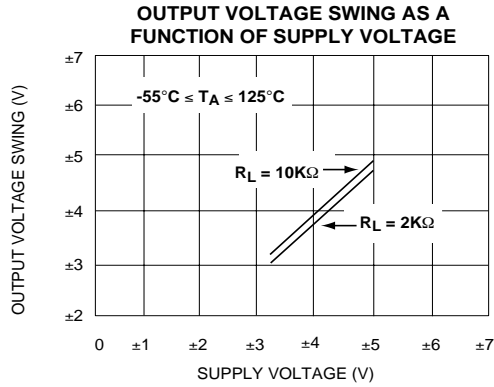
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

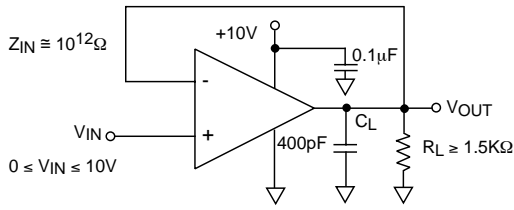


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

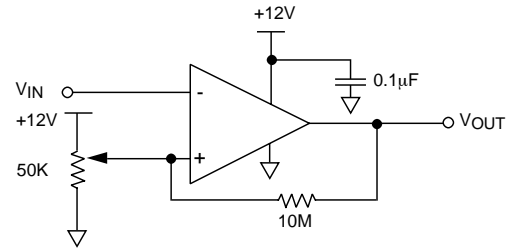


TYPICAL APPLICATIONS

RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER



RAIL-TO-RAIL VOLTAGE COMPARATOR



LOW OFFSET SUMMING AMPLIFIER

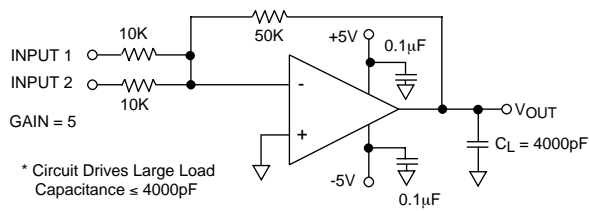
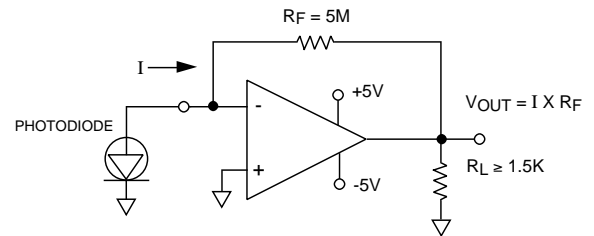
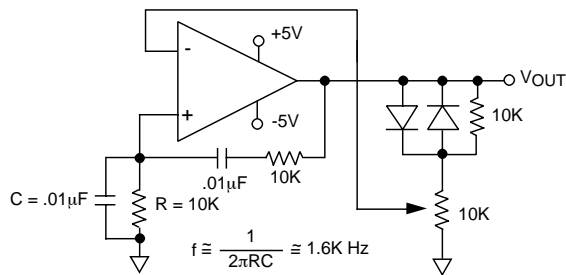


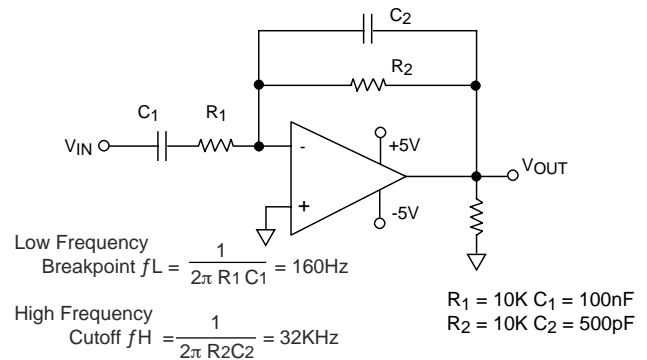
PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER



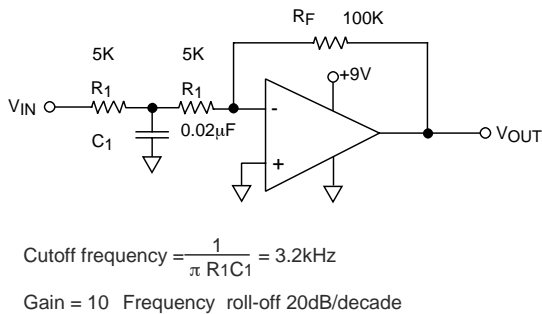
WIEN BRIDGE OSCILLATOR (RAIL-TO-RAIL) SINE WAVE GENERATOR



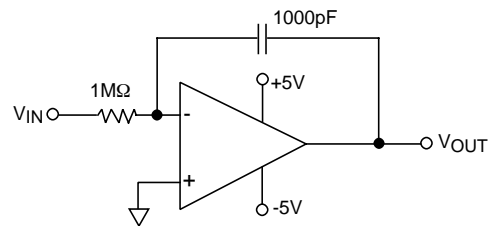
BANDPASS NETWORK



LOW PASS FILTER (RFI FILTER)

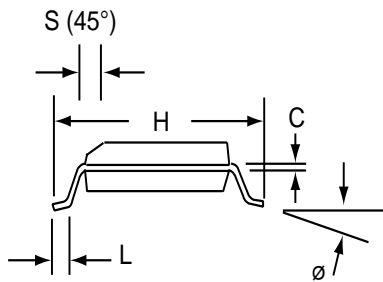
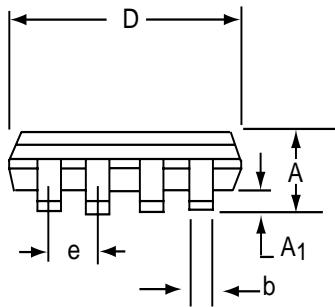
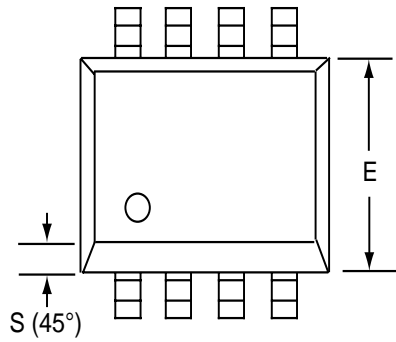


PRECISION CHARGE INTEGRATOR



SOIC-8 PACKAGE DRAWING

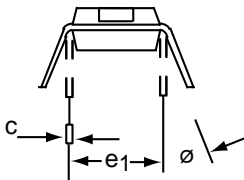
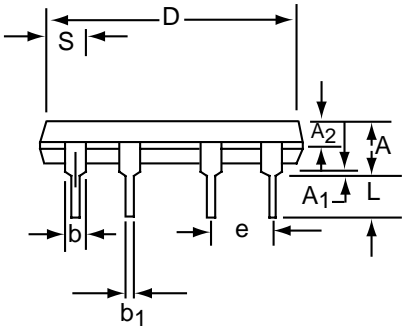
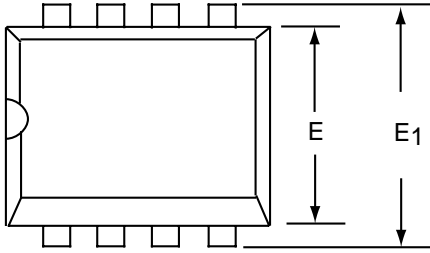
8 Pin Plastic SOIC Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-8 PACKAGE DRAWING

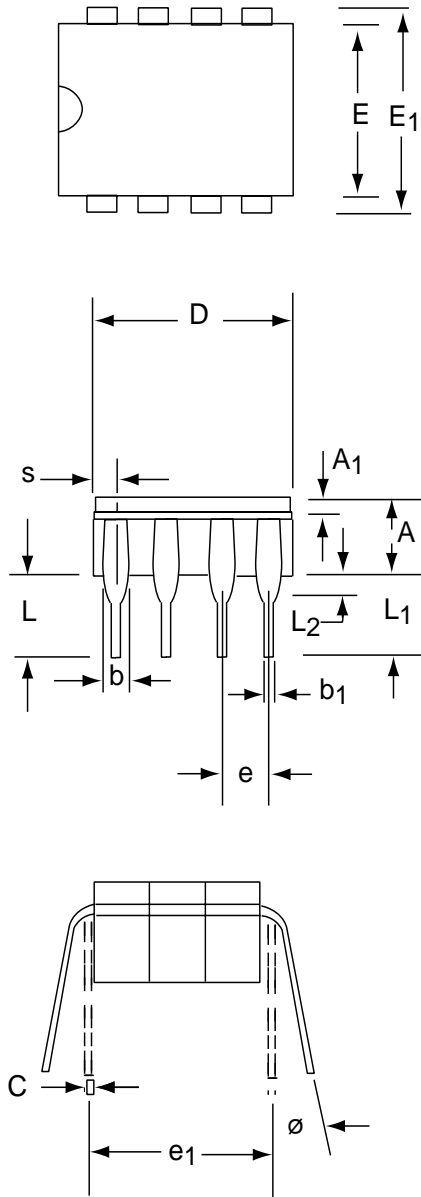
8 Pin Plastic DIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A ₁	0.38	1.27	0.015	0.050
A ₂	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b ₁	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E ₁	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e ₁	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
∅	0°	15°	0°	15°

CERDIP-8 PACKAGE DRAWING

8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A₁	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b₁	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-8	--	10.29	--	0.405
E	5.59	7.87	0.220	0.310
E₁	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e₁	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L₁	3.18	--	0.125	--
L₂	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
∅	0°	15°	0°	15°