

N-channel TrenchMOS logic level FET 28 July 2016

Product data sheet

1. General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with VGS(th) rating of greater than 0.5V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quie	ck reference data						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	56	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	96	W
Static characte	eristics					1	
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 15 A; T _j = 25 °C; <u>Fig. 11</u>		-	11.5	14	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 15 A; V _{DS} = 48 V; Fig. 13; Fig. 14		-	6.7	-	nC

nexperia

N-channel TrenchMOS logic level FET

5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain		
3	S	source		G-UF4
mb	D	mounting base; connected to drain	D2PAK (SOT404)	mbb076 S

6. Ordering information

Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
BUK9614-60E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404			

7. Marking

Table 4. Marking codes	
Type number	Marking code
BUK9614-60E	BUK9614-60E

8. Limiting values

Table 5.Limiting values

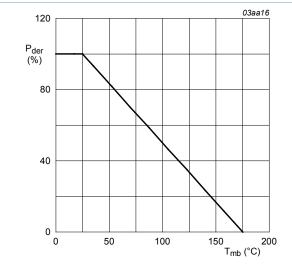
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	60	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ		-	60	V
V _{GS}	gate-source voltage	T _j ≤ 175 °C; DC		-10	10	V
		$T_j \le 175 \ ^{\circ}C; Pulsed$	[1][2]	-15	15	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	96	W
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; <u>Fig. 2</u>		-	56	А
		T _{mb} = 100 °C; V _{GS} = 5 V; <u>Fig. 2</u>		-	40	А
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \ \mu$ s; Fig. 3		-	224	А
T _{stg}	storage temperature			-55	175	°C
3UK9614-60E	All in	formation provided in this document is subject to legal disclaimers.		© Nexpe	ria B.V. 2017. A	Il rights reserve

N-channel TrenchMOS logic level FET

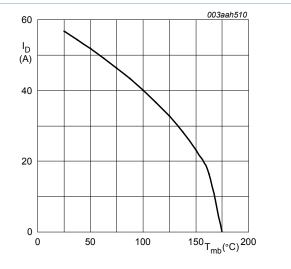
Symbol	Parameter	Conditions		Min	Мах	Unit
Tj	junction temperature			-55	175	°C
Source-dra	ain diode					
I _S	source current	T _{mb} = 25 °C	[3]	-	56	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^\circ C$		-	224	А
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$\begin{split} & {\sf I}_{\sf D} = 56 \; {\sf A}; {\sf V}_{\sf sup} \le 60 \; {\sf V}; {\sf R}_{\sf GS} = 50 \; \Omega; \\ & {\sf V}_{\sf GS} = 5 \; {\sf V}; \; {\sf T}_{\sf j(init)} = 25 \; {\rm ^{\circ}C}; \; {\sf unclamped}; \\ & {\sf Fig. 4} \end{split}$	[4][5]	-	39	mJ

- Accumulated pulse duration up to 50 hours delivers zero defect ppm [1]
- [2] Significantly longer life times are achieved by lowering T_{j} and or V_{GS}
- [3]
- Continuous current is limited by package. Single-pulse avalanche rating limited by maximum junction temperature of 175 °C. Refer to application note AN10273 for further information. [4]
- [5]



Normalized total power dissipation as a Fig. 1. function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

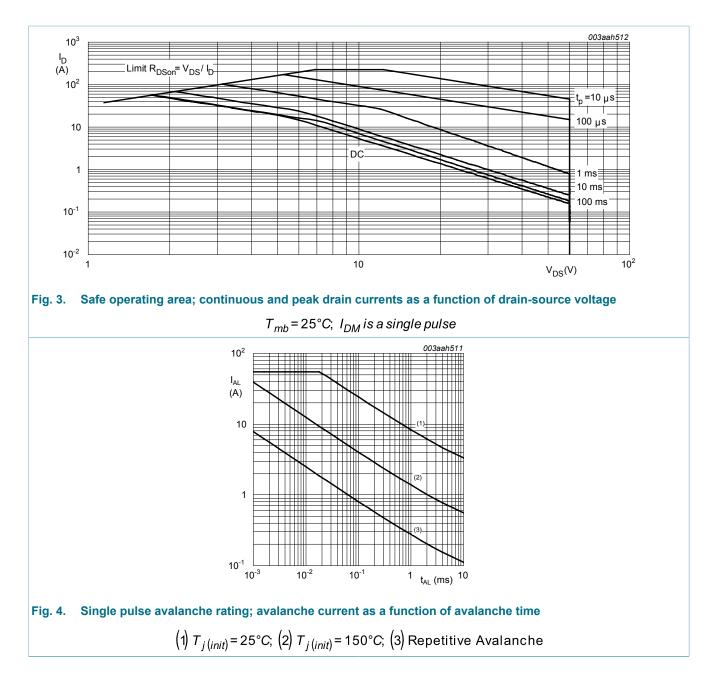


Continuous drain current as a function of Fig. 2. mounting base temperature

 $V_{GS} \ge 5V$

BUK9614-60E

N-channel TrenchMOS logic level FET



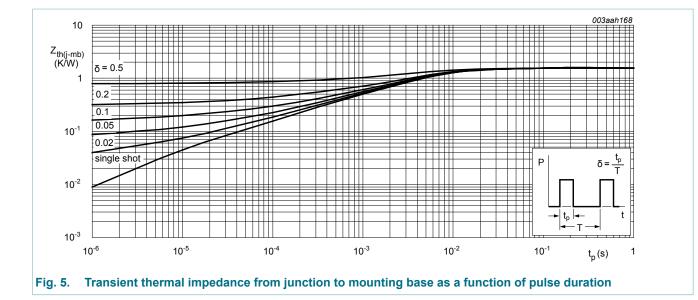
9. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	<u>Fig. 5</u>	-	-	1.56	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

Table 6. Thermal characteristics

BUK9614-60E

N-channel TrenchMOS logic level FET

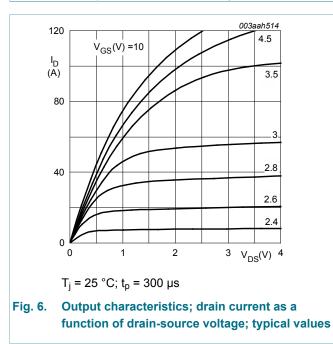


10. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	60	-	-	V
	breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	54	-	-	V
V _{GS(th)} gate-source thresho voltage	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V
I _{DSS} drain leakage current	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	μA
	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA	
I _{GSS} gate leakage curre	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon} drain-source on-siresistance	drain-source on-state	V _{GS} = 5 V; I _D = 15 A; T _j = 25 °C; <u>Fig. 11</u>	-	11.5	14	mΩ
	resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 11	-	10.3	12.8	mΩ
		V _{GS} = 5 V; I _D = 15 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	31	mΩ
Dynamic ch	naracteristics	· · ·				
Q _{G(tot)}	total gate charge	I _D = 15 A; V _{DS} = 48 V; V _{GS} = 5 V;	-	20.5	-	nC
Q _{GS}	gate-source charge	Fig. 13; Fig. 14	-	4	-	nC

N-channel TrenchMOS logic level FET

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Q _{GD}	gate-drain charge		-	6.7	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	1988	2651	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	196	235	pF
C _{rss}	reverse transfer capacitance	_	-	114	156	pF
t _{d(on)}	turn-on delay time	V_{DS} = 45 V; R _L = 3 Ω; V _{GS} = 5 V;	-	16.9	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	22.4	-	ns
t _{d(off)}	turn-off delay time		-	35.7	-	ns
t _f	fall time		-	22.9	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L _S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-dra	in diode	· · · · ·	I		1	
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; <u>Fig. 16</u>	-	0.83	1.2	V
t _{rr}	reverse recovery time	I_{S} = 15 A; dI _S /dt = -100 A/µs; V _{GS} = 0 V;	-	22.3	-	ns
Q _r	recovered charge	V _{DS} = 25 V	-	20.9	-	nC



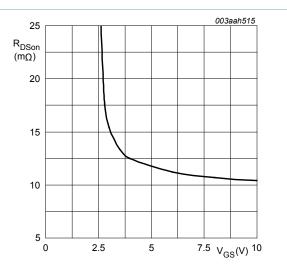
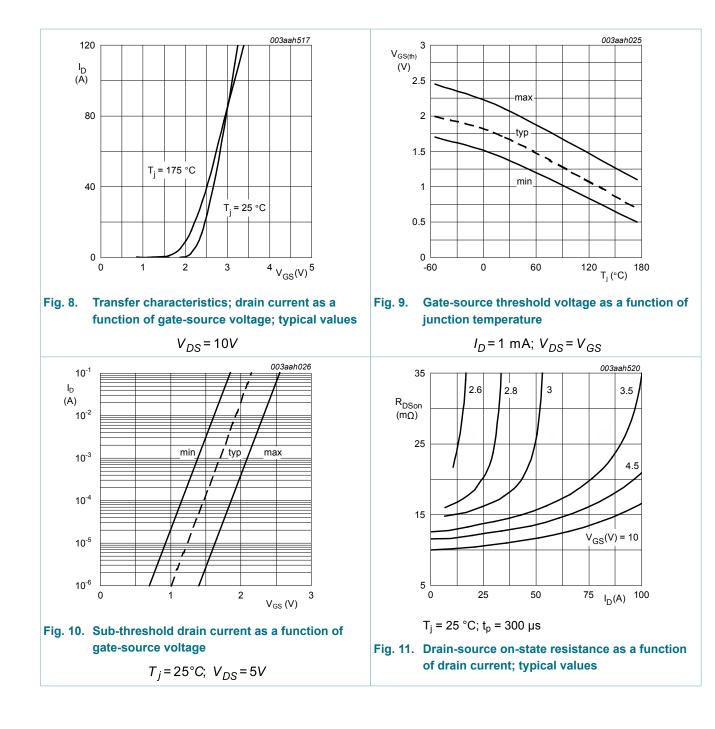


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

 $T_j = 25^{\circ}C; I_D = 15A$

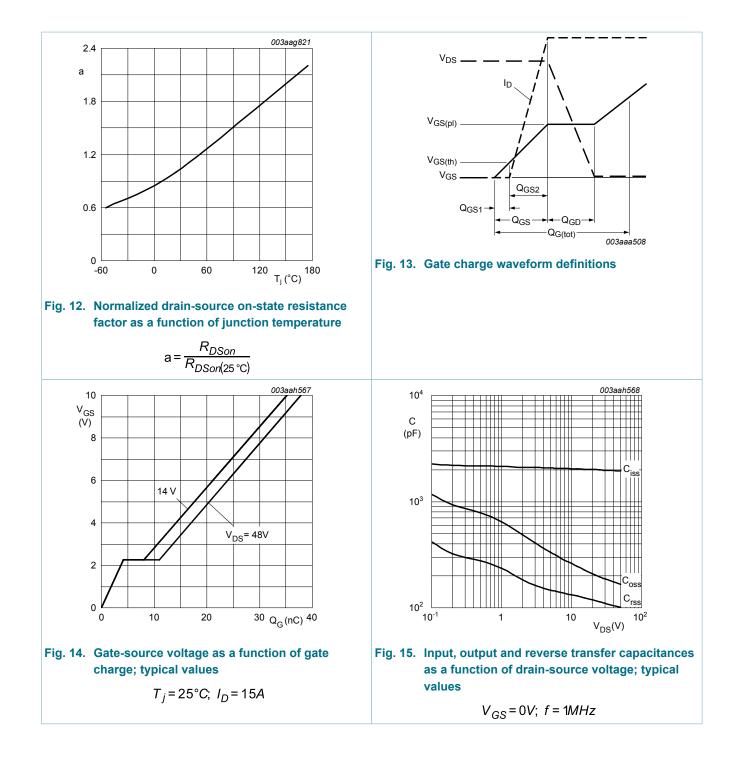
BUK9614-60E

N-channel TrenchMOS logic level FET



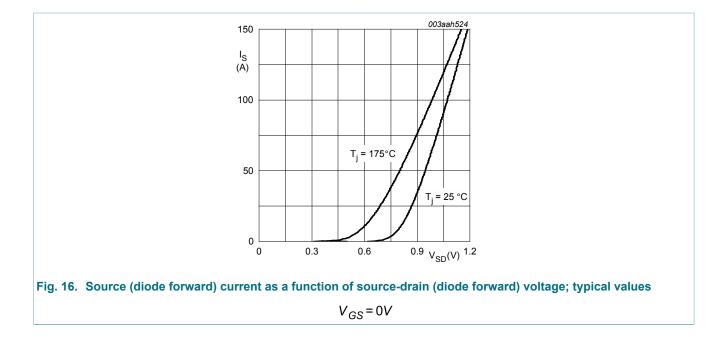
BUK9614-60E

N-channel TrenchMOS logic level FET



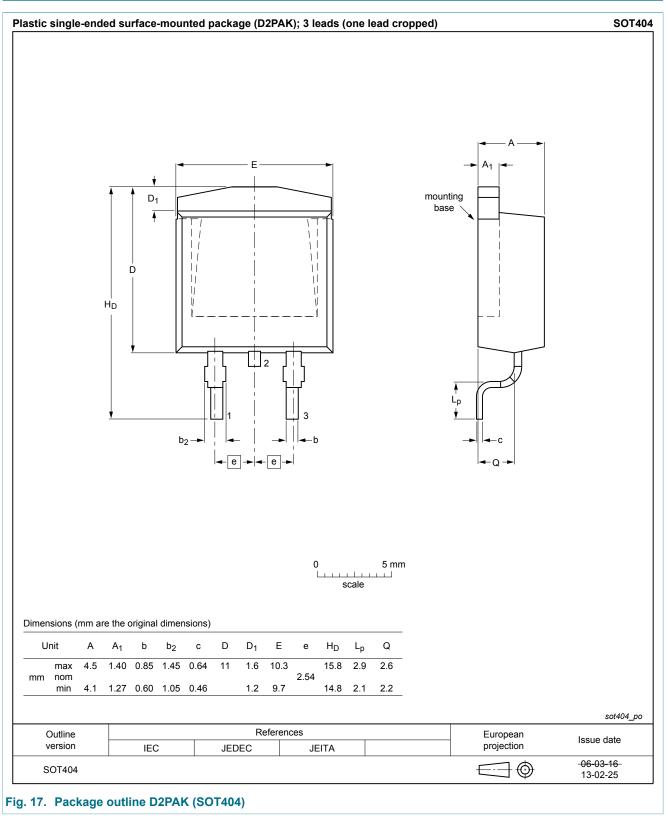
BUK9614-60E

N-channel TrenchMOS logic level FET



N-channel TrenchMOS logic level FET

11. Package outline



N-channel TrenchMOS logic level FET

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <u>http://www.nexperia.com</u>.

12.2 Definitions

Preview — The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and

customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This Nexperia product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale - Nexperia

products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

N-channel TrenchMOS logic level FET

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

N-channel TrenchMOS logic level FET

13. Contents

General description1	I
Features and benefits	1
Applications1	
Quick reference data	1
Pinning information2	2
Ordering information2	2
Marking2	2
Limiting values	2
Thermal characteristics4	ł
Characteristics5	5
Package outline10)
Legal information11	I
Data sheet status 17	1
Definitions11	I
Disclaimers11	J
Trademarks 12	2
	Features and benefits 1 Applications 1 Quick reference data 1 Pinning information 2 Ordering information 2 Limiting values 2 Limiting values 2 Characteristics 5 Package outline 10 Legal information 11 Data sheet status 11 Disclaimers 11

© Nexperia B.V. 2017. All rights reserved

For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com Date of release: 28 July 2016