# 74AVCH16245

16-bit transceiver with direction pin; 3.6 V tolerant; 3-state

Rev. 3 — 8 January 2013

Product data sheet

### 1. General description

The 74AVCH16245 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features two output enable inputs (nOE) for easy cascading and two send/receive inputs (nDIR) for direction control. Inputs nOE control the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74AVCH16245 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down, tie pins  $n\overline{OE}$  to  $V_{CC}$  through a pull-up resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient (see Figure 4 and Figure 5)

The 74AVCH16245 has active bus-hold circuitry to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

#### 2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-1A (2.7 V to 3.6 V)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple VCC and GND pins to minimize noise and ground bounce
- Supports Live Insertion
- All inputs have bus-hold

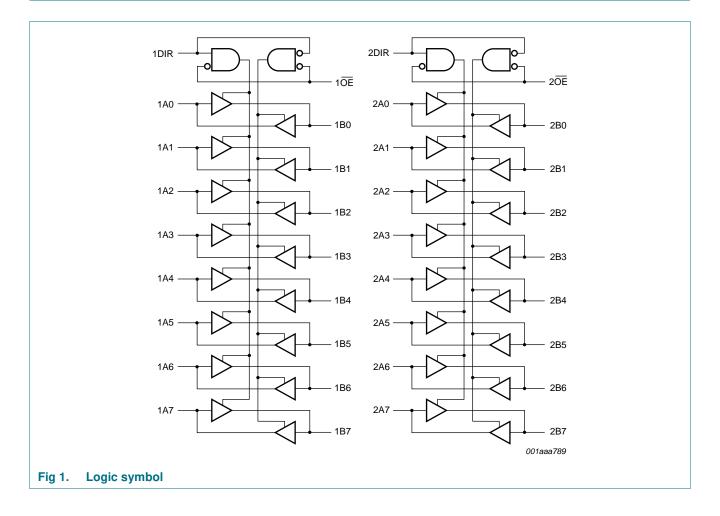


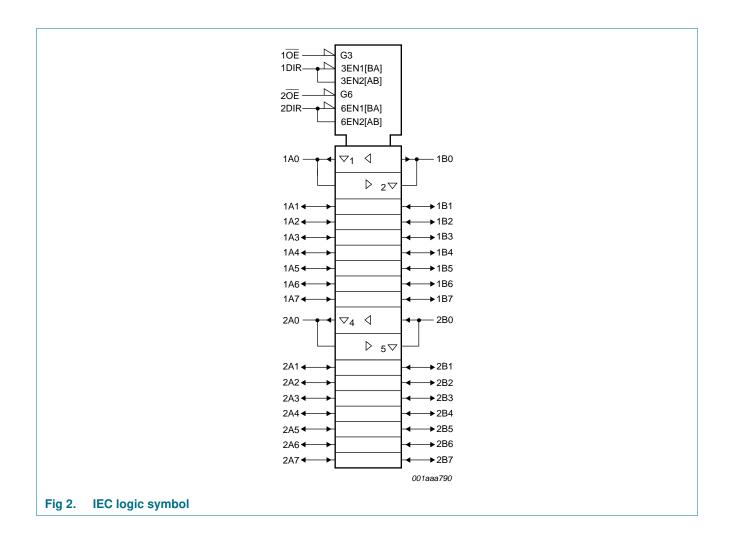
# 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVCH16245DGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

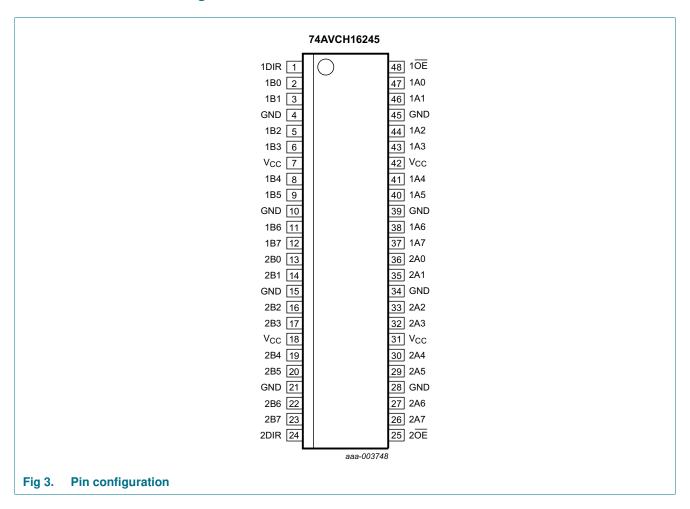
# 4. Functional diagram





# 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
$V_{CC}$	7, 18, 31, 42	supply voltage
1 <del>0E</del> , 2 <del>0E</del>	48, 25	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output

# 6. Functional description

Table 3. Function table[1]

Inputs nOE		Outputs		
nOE nDIR		nAn	nBn	
L	L	A = B	inputs	
L	Н	inputs	B = A	
Н	X	Z	Z	

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

# 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	$V_I < 0 V$	-50	-	mA
$V_{I}$	input voltage		<u>[1]</u> –0.5	+4.6	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
$V_{O}$	output voltage	output HIGH or LOW	<u>[1]</u> –0.5	$V_{CC} + 0.5$	V
		output 3-state	<u>[1]</u> –0.5	+4.6	V
I <sub>O</sub>	output current	$V_O = 0 V to V_{CC}$	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[2] -	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup> Above 60  $^{\circ}\text{C}$  the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

# 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CC}$	supply voltage	according to JEDEC Low Voltage Standards	1.4	-	1.6	V
			1.65	-	1.95	V
			2.3	-	2.7	V
			3.0	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
VI	input voltage		0	-	3.6	V
Vo	output voltage	output HIGH or LOW	0	-	$V_{CC}$	V
		output 3-state	0	-	3.6	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall	V <sub>CC</sub> = 1.4 V to 1.6 V	0	-	40	ns/V
	rate	V <sub>CC</sub> = 1.65 V to 1.95 V	0	-	30	ns/V
		V <sub>CC</sub> = 2.3 V to 3.0 V	0	-	20	ns/V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0	-	10	ns/V

### 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T <sub>amb</sub> = -	40 °C to +85 °C					
$V_{IH}$	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	$V_{CC}$	-	-	٧
		V <sub>CC</sub> = 1.4 V to 1.6 V	$0.65 \times V_{CC}$	0.9	-	٧
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	0.9	-	٧
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	٧
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	1.5	-	٧
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	GND	٧
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	0.9	$0.35 \times V_{CC}$	٧
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.9	$0.35 \times V_{CC}$	٧
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	٧
		$V_{CC}$ = 3.0 V to 3.6 V	-	1.5	0.8	٧
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_{O} = -100 \mu A$ ; $V_{CC} = 1.65 V$ to 3.6 V	$V_{CC}-0.20$	$V_{CC}$	-	٧
		$I_{O} = -3 \text{ mA}; V_{CC} = 1.4 \text{ V}$	$V_{CC}-0.35$	$V_{CC}-0.21$	-	٧
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	$V_{CC}-0.45$	$V_{CC}-0.25$	-	٧
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	$V_{CC}-0.55$	V <sub>CC</sub> - 0.37	-	٧
		$I_{O} = -12 \text{ mA}; V_{CC} = 3.0 \text{ V}$	$V_{CC}-0.70$	$V_{CC}-0.47$	-	V

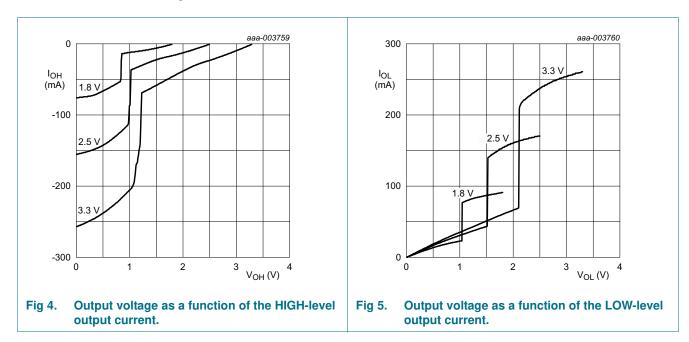
 Table 6.
 Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O$ = 100 $\mu$ A; $V_{CC}$ = 1.65 V to 3.6 V	-	GND	0.20	V
		$I_O = 3 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	0.22	0.35	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	0.24	0.45	V
		$I_{O} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	0.38	0.55	V
		$I_O = 12 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	0.53	0.70	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 1.4$ V to 3.6 V	-	0.1	2.5	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{I}$ or $V_{O} = 3.6 \text{ V}$ ; $V_{CC} = 0.0 \text{ V}$	-	±0.1	±10	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND				
		$V_{CC} = 1.4 \text{ V to } 2.7 \text{ V}$	-	0.1	5	μΑ
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	0.1	10	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A				
		V <sub>CC</sub> = 1.4 V to 2.7 V	-	0.1	20	μΑ
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	0.2	40	μΑ
I <sub>BHL</sub>	bus hold LOW current	$V_{CC} = 1.65 \text{ V}; V_{I} = 0.35 \times V_{CC}$	25	-	-	μΑ
		$V_{CC} = 2.3 \text{ V}; V_{I} = 0.7 \text{ V}$	45	-	-	μΑ
		$V_{CC} = 3.0 \text{ V}; V_I = 0.8 \text{ V}$	75	-	-	μΑ
I <sub>BHH</sub>	bus hold HIGH current	$V_{CC} = 1.65 \text{ V}; V_{I} = 0.35 \times V_{CC}$	-25	-	-	μΑ
		$V_{CC} = 2.3 \text{ V}; V_{I} = 0.35 \times V_{CC}$	-45	-	-	μΑ
		$V_{CC} = 3.0 \text{ V}; V_{I} = 0.35 \times V_{CC}$	<b>−75</b>	-	-	μΑ
I <sub>BHLO</sub>	bus hold LOW overdrive	V <sub>CC</sub> = 1.95 V	200	-	-	μΑ
	current	$V_{CC} = 2.7 \text{ V}$	300	-	-	μΑ
		V <sub>CC</sub> = 3.6 V	450	-	-	μΑ
I <sub>BHHO</sub>	bus hold HIGH overdrive	V <sub>CC</sub> = 1.95 V	-200	-	-	μΑ
	current	V <sub>CC</sub> = 2.7 V	-300	-	-	μΑ
		V <sub>CC</sub> = 3.6 V	-450	-	-	μΑ
Cı	input capacitance		-	5.0	-	pF

<sup>[1]</sup> All typical values are measured at  $T_{amb}$  = 25 °C.

### 9.1 Graphs



# 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions		-40	°C to +85	°C	Unit
				Min	Typ[2]	Max	
t <sub>pd</sub> propagation delay		nAn to nBn; nBn to nAn; see Figure 6	[1]		'		'
		V <sub>CC</sub> = 1.2 V		-	5.4	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V		-	3.1	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		1.4	2.3	3.3	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.5	1.6	2.2	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		0.7	1.4	2.0	ns
t <sub>en</sub>	enable time	nOE to nAn, nBn; see Figure 7	[1]				
		V <sub>CC</sub> = 1.2 V		-	7.4	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V		-	6.4	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		1.4	4.4	7.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.0	2.8	4.3	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		0.7	2.3	3.7	ns
t <sub>dis</sub>	disable time	nOE to nAn, nBn; see Figure 7	[1]				
		V <sub>CC</sub> = 1.2 V		-	7.3	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V		-	5.7	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		2.2	4.2	7.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.1	2.3	5.4	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.2	2.5	3.9	ns

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions	Conditions –40 °C to +85 °C		-40 °C to +85 °C	
			Min	Typ[2]	Max	
$C_{PD}$	power dissipation	per input; $V_I = GND$ to $V_{CC}$				
capacitance		outputs enabled	-	42	-	pF
		outputs disabled	-	2	-	pF

- t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.
  - $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [2] Typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).
  - $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

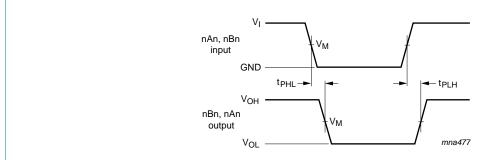
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

#### 11. Waveforms



Measurement points are given in Table 8.

Logic levels:  $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical output voltage levels that occur with the output load.

Fig 6. The input (nAn, nBn) to output (nBn, nAn) propagation delays

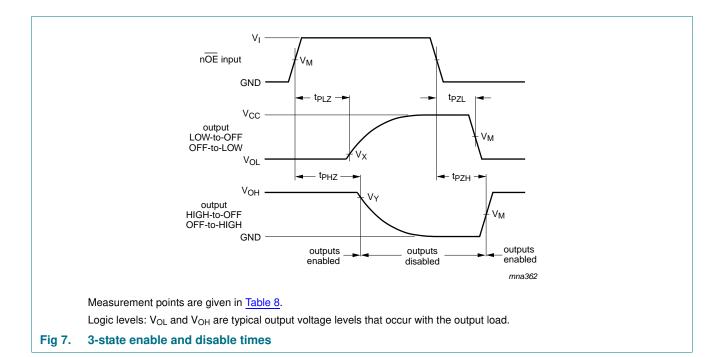
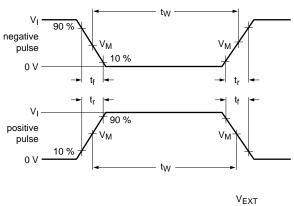
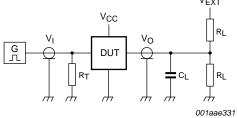


Table 8. Measurement points

Supply voltage	V <sub>M</sub>	Input			
V <sub>CC</sub>		VI	$t_r = t_f$	V <sub>X</sub>	V <sub>Y</sub>
1.2 V	$0.5 \times V_{CC}$	V <sub>CC</sub>	≤ 2 ns	V <sub>OL</sub> + 0.15 V	$V_{OH}-0.15\ V$
1.4 V to 1.6 V	$0.5 \times V_{CC}$	V <sub>CC</sub>	≤ 2 ns	V <sub>OL</sub> + 0.15 V	$V_{OH}-0.15\ V$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V <sub>CC</sub>	≤ 2 ns	V <sub>OL</sub> + 0.15 V	$V_{OH}-0.15\ V$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{CC}$	≤ 2 ns	$V_{OL} + 0.15 V$	$V_{OH}-0.15\ V$
3.0 V to 3.6 V	$0.5 \times V_{CC}$	$V_{CC}$	≤ 2 ns	$V_{OL} + 0.3 V$	$V_{OH}-0.3\ V$





Test data is given in Table 9.

Definitions for test circuit:

 $R_L$  = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

 $V_{EXT}$  = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

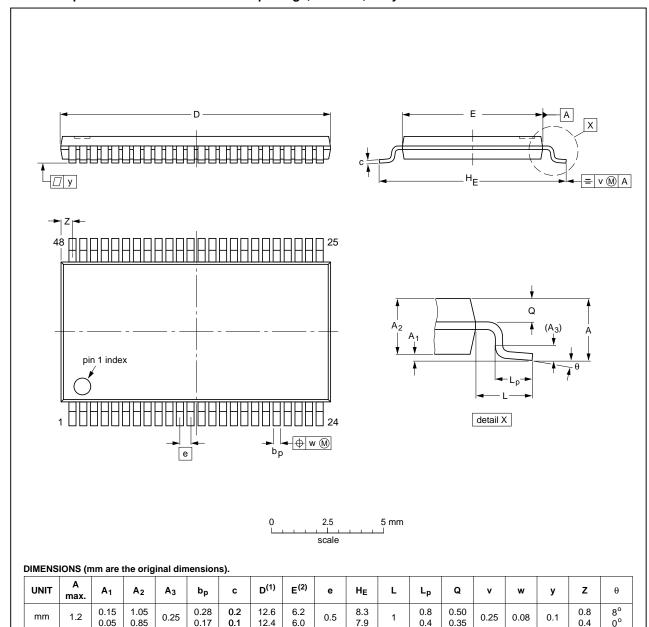
Table 9. Test data

Supply voltage			V <sub>EXT</sub>	V <sub>EXT</sub>			
			t <sub>PLH</sub> , t <sub>PHL</sub>	$t_{PLZ}$ , $t_{PZL}$	t <sub>PHZ</sub> , t <sub>PZH</sub>		
1.2 V	$V_{CC}$	≤ 2 ns	15 pF	$2 \text{ k}\Omega$	open	$2\times V_{CC}$	GND
1.4 V to 1.6 V	$V_{CC}$	≤ 2 ns	15 pF	$2  \mathrm{k}\Omega$	open	$2\times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	≤ 2 ns	30 pF	1 kΩ	open	$2\times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	≤ 2 ns	30 pF	$500 \Omega$	open	$2\times V_{CC}$	GND
3.0 V to 3.6 V	$V_{CC}$	≤ 2 ns	30 pF	$500 \Omega$	open	$2\times V_{CC}$	GND

# 12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



#### . .

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFERENCES			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT362-1		MO-153				<del>99-12-27</del> 03-02-19

Fig 9. Package outline SOT362-1 (TSSOP48)

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# 13. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

# 14. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes	
74AVCH16245 v.3	20130108	Product data sheet	-	-	74AVCH16245 v.2	
Modifications:	<ul> <li>Δl<sub>CC</sub> remo</li> </ul>	ved (errata).				
74AVCH16245 v.2	20120828	Product data sheet	-	-	74AVCH16245 v.1	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>					
	<ul> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>					
	<ul> <li>Ordering i</li> </ul>	nformation table correct	ted (errata).∆I <sub>CC</sub>			
74AVCH16245 v.1	20000307	Product specification	-	-	-	

### 15. Legal information

#### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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### 16-bit transceiver with direction pin; 3.6 V tolerant; 3-state

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