SN5426, SN54LS26, SN7426, SN74LS26 QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

DECEMBER 1983-REVISED MARCH 1988

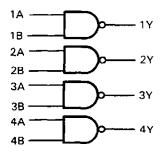
For Driving Low-Threshold-Voltage MOS Inputs

description

These 2-input open-collector NAND gates feature high-output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source.

The SN5426 and SN54LS26 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $\,^{\circ}\text{C}$. The SN7426 and SN74LS26 are characterized for operation from 0 $\,^{\circ}\text{C}$ to 70 $\,^{\circ}\text{C}$.

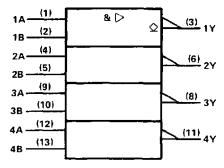
logic diagram



positive logic

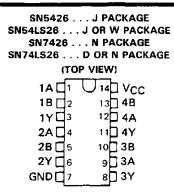
$$Y = \overline{AB}$$

logic symbol†

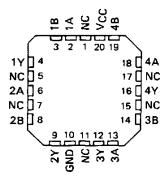


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

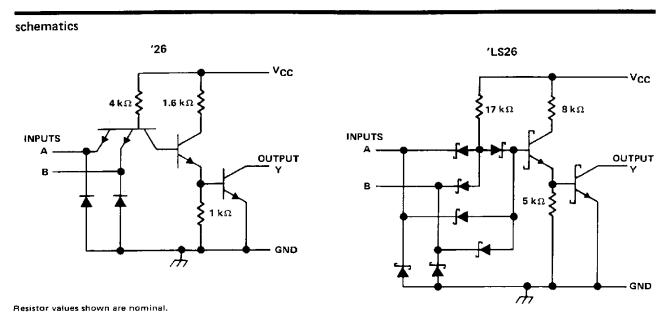


SN54LS26 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

SN5426, SN54LS26, SNSN7426, SN74LS26 QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES



Aesistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage , VCC (see Note 1)
Input voltage: '26
'LS26 7 V
Operating free-air temperature: SN54'
SN74′
Storage temperature range

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS26		SN74LS26			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX	UNII
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
VIL Low-level input voltage			0.7			0.8	V
VOH High-level output voltage			15			15	V
OL Law-level output current			4			8	mA
TA Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			S	N54LS	26	S	N74LS2	26	<u> </u>
PANAMETER				MIN TYP\$ MAX			MIN TYP\$ MAX			UNIT
VIK	V _{CC} = MIN,	I ₁ = 18 mA				- 1.5			– 1.5	٧
	V _{CC} = MIN,	VIL = MAX,	V _{OH} = 12 V			50			50	μΑ
юн	V _{CC} = MIN,	VIL = MAX,	V _{OH} = 15 V			1			1	mA
1.7	V _{CC} = MIN,	V _{1H} = 2 V,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	
V _O L	V _{CC} = MIN,	V _{1H} = 2 V,	IOL = 8 mA					0.35	0.5	· ·
lį.	V _{CC} = MAX,	V _I = 7 V				0.1			0.1	mΑ
ΊΗ	V _{CC} = MAX,	V _{IH} = 2.7 V				20			20	μΑ
11L	V _{CC} = MAX,	V _{IL} = 0.4 V	<u> </u>			- 0.4			- 0.4	mA
¹ ССН	V _{CC} = MAX,	V ₁ = 0			0.8	1.6		8.0	1.6	mA
ICCL	V _{CC} = MAX,	V _I = 4.5 V			2.4	4.4		2.4	4.4	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions, ‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYP	MAX	UNIT
tPLH .	A or B	'	$R_1 = 2 k\Omega$, $C_1 = 15 pF$	17	32	ns
tpHL	7 31 15	<u>'</u>	11[-2 Kas, C[-15 pr	15	28	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN5426, SN7426 QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

recommended operating conditions

	SN5426		SN7426			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX	CIVIT
VCC Supply voltage	4.5	5	5.5	4.75	5	5.25	
VIH High-level input voltage	2			2			V
VIL Low-level input voltage			0.8			0.8	>
VOH High-level output voltage			15			15	>
IOL Low-level output current			16			16	mΑ
TA Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS†	SN5426	\$N7426	i
PARAMETER	TEST CONDITIONS.	MIN TYP‡ MAX	MIN TYP‡ MAX	UNIT
VIK	$V_{CC} = MIN, i_{\parallel} \approx -12 \text{ mA}$	- 1.5	-1.5	V
	$V_{CC} = MIN$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 12 \text{ V}$		50	
ЮН	$V_{CC} = MIN$, $V_{IL} = 0.7 \text{ V}$, $V_{OH} = 12 \text{ V}$	50		μΑ
	VCC = MIN. VIL = 0.8 V, VOH = 15 V		1	
	$V_{CC} = MIN$, $V_{IL} = 0.7 \text{ V}$, $V_{OH} = 15 \text{ V}$	1		mA
VoL	$V_{CC} = MIN$, $V_{IH} = 2 V$, $I_{OL} = 16 mA$	0.4	0.4	V
lj .	V _{CC} = MAX, V _I = 5.5 V	1	1	mA
IH	V _{CC} = MAX, V ₁ = 2.4 V	40	40	μΑ
IL.	$V_{CC} = MAX$, $V_{\parallel} = 0.4 \text{ V}$	-1.6	-1.6	mΑ
Іссн	$V_{CC} = MAX, V_I = 0$	4 8	4 8	mA
CCL	$V_{CC} = MAX$, $V_I = 4.5 V$	12 22	12 22	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C (see note 2)

PAR	RAMETER	FROM (INPUT)	TQ (TUPTUO)	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
	^t PLH	A or B	Y	R ₁ = 1 kΩ,	C ₁ = 15 pF	Ī	16	24	ns
	^t PHL :						11	17	ns

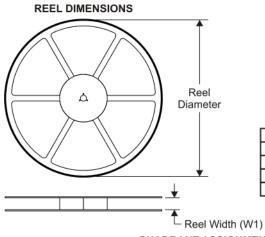
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

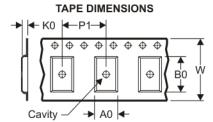
 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

PACKAGE MATERIALS INFORMATION

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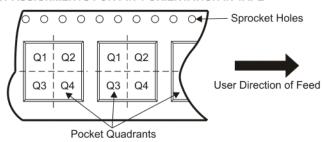
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS26DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	SN74LS26DR	SOIC	D	14	2500	346.0	346.0	33.0

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