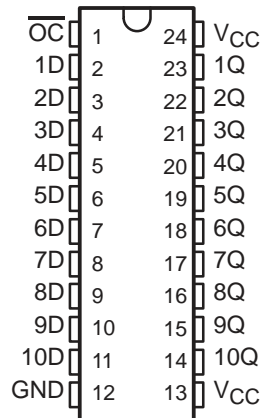


# SN54AS821, SN54AS822, SN74AS821, SN74AS822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS230 – D2825, DECEMBER 1983 – REVISED JANUARY 1986

- Functionally Equivalent to AMD's AM29821 and AM29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity
- Outputs Have Undershoot Protection Circuitry
- Powerup High-impedance State
- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

SN54AS821 . . . JT PACKAGE  
SN74AS821 . . . DW OR NT PACKAGE  
(TOP VIEW)



## description

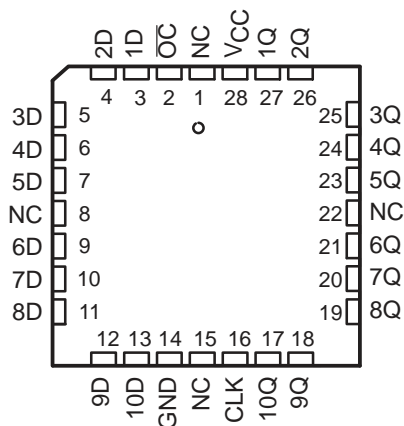
These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS821 will be true, and on the 'AS822 will be complementary to the data input.

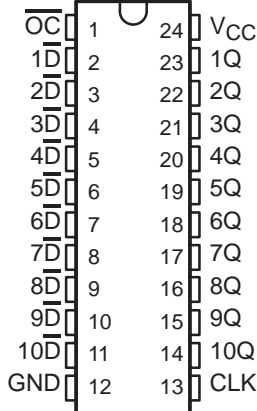
A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS' family is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS' family is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

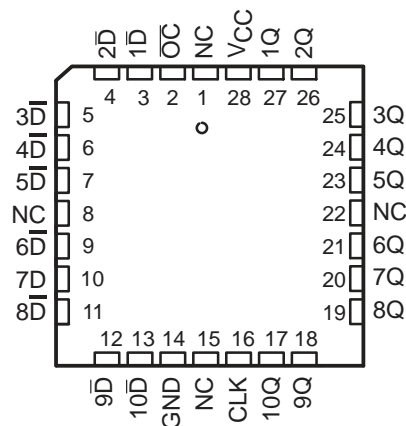
SN54AS821 . . . FK PACKAGE  
SN74AS821 . . . FN PACKAGE  
(TOP VIEW)



SN54AS822 . . . JT PACKAGE  
SN74AS822 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54AS822 . . . FK PACKAGE  
SN74AS822 . . . FN PACKAGE  
(TOP VIEW)



NC—No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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# SN54AS821, SN74AS821

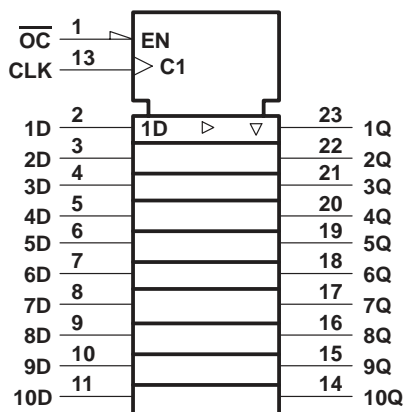
## 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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'AS821 FUNCTION TABLE  
(each flip-flop)

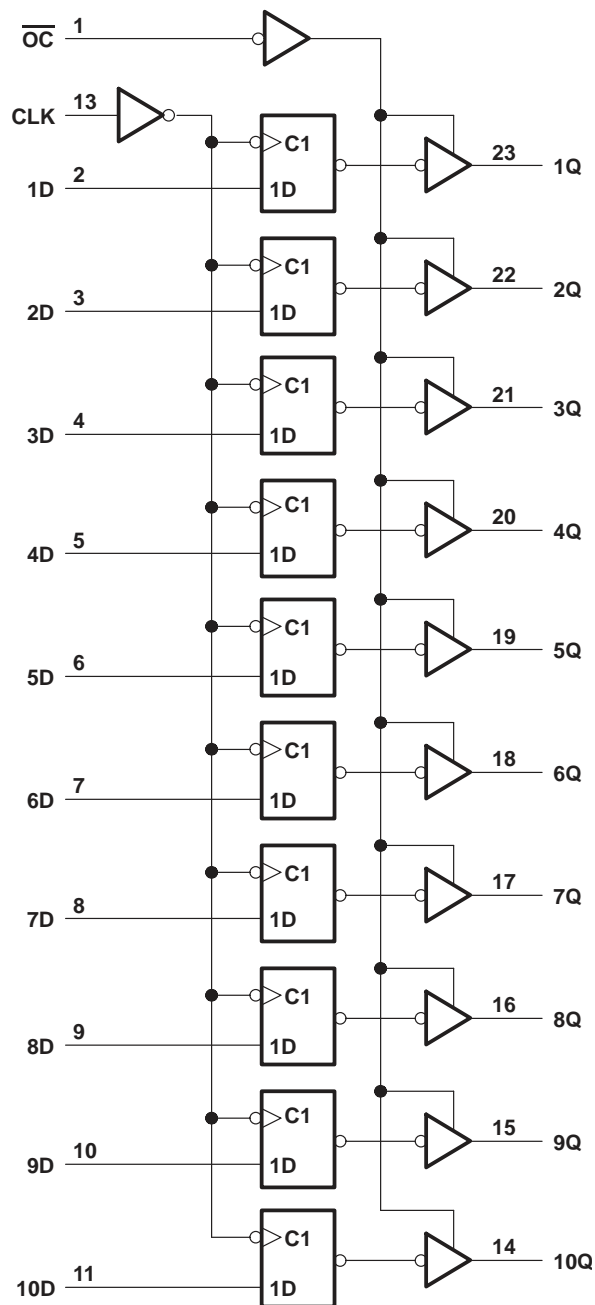
INPUTS			OUTPUT
OC	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

'AS821 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS821 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

# SN54AS822, SN74AS822

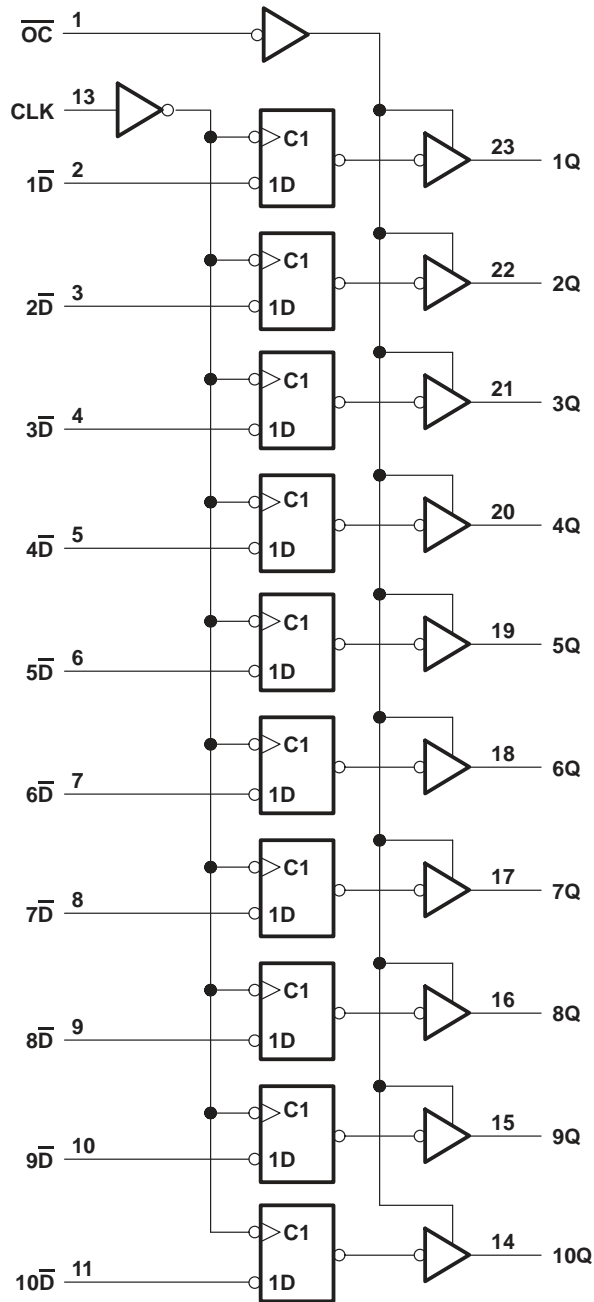
## 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS230 – D2825, DECEMBER 1983 – REVISED JANUARY 1986

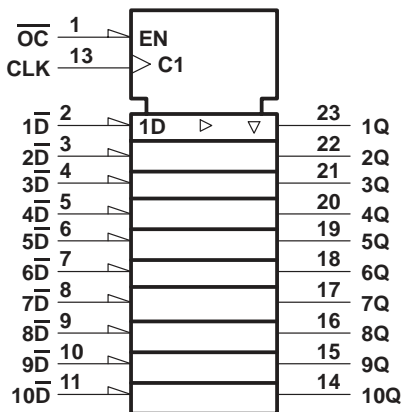
'AS822 FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
OC	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

'AS822 logic diagram positive logic



'AS822 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

# SN54AS821, SN54AS822, SN74AS821, SN74AS822

## 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS821, SN54AS822	-55°C to 125°C
SN74AS821, SN74AS822	0°C to 70°C
Storage temperature range	-65°C to 150°C

### recommended operating conditions

		SN54AS821 SN54AS822			SN74AS821 SN74AS822			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-24			-24	mA
$I_{OL}$	Low-level output current			32			48	mA
$t_w$	Pulse duration, CLK high or low	9			8			ns
$t_{su}$	Setup time, data before CLK $\uparrow$	7			6			ns
$t_h$	Hold time, data after CLK $\uparrow$	0			0			ns
$T_A$	Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS821 SN54AS822			SN74AS821 SN74AS822			UNIT
		MIN	TYP $\ddagger$	MAX	MIN	TYP $\ddagger$	MAX	
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -15$ mA	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5$ V, $I_{OH} = -24$ mA	2			2			
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 32$ mA		0.25	0.5				V
	$V_{CC} = 4.5$ V, $I_{OL} = 48$ mA				0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50			50	$\mu$ A
$I_{OZL}$	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			-50			-50	$\mu$ A
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	$\mu$ A
$I_{IL}$	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.5			-0.5	mA
$I_{O\ddagger}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	-30		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5$ V	'AS821	Outputs high	55	88	55	88	mA
			Outputs low	68	109	68	109	
		'AS822	Outputs disabled	70	113	70	113	
			Outputs high	55	88	55	88	
			Outputs low	68	109	68	109	
			Outputs disabled	70	113	70	113	

$\dagger$  All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ$ C.

$\ddagger$  The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



# SN54AS821, SN54AS822, SN74AS821, SN74AS822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_1 = 500 \ \Omega,$ $R_2 = 500 \ \Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT
			SN54AS821 SN54AS822		SN74AS821 SN74AS822		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	CLK	Any Q	3.5	9	3.5	7.5	ns
t <sub>PHL</sub>			3.5	11.5	3.5	10.5	
t <sub>PZH</sub>	OC	Any Q	4	12	4	11	ns
t <sub>PZL</sub>			4	13	4	12	
t <sub>PHZ</sub>	OC	Any Q	2	10	2	8	ns
t <sub>PZL</sub>			2	10	2	8	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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