

# MOSFET

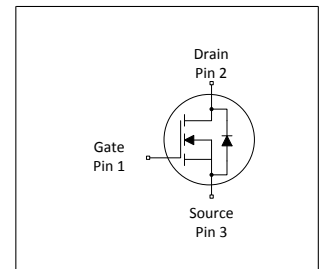
## StrongIRFET™

### Features

- Very low  $R_{DS(on)}$
- Excellent gate charge x  $R_{DS(on)}$  (FOM)
- Optimized  $Q_{rr}$
- 175°C operating temperature
- Product validation according to JEDEC standard
- Optimized for broadest availability from distribution partners

### Benefits

- Reduced conduction losses
- Ideal for high switching frequency
- Lower overshoot voltage
- Increased reliability versus 150°C rated parts
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	150	V
$R_{DS(on),typ}$	2.3	mΩ
$R_{DS(on),max}$	2.7	mΩ
$I_D(Silicon\ Limited)$	316	A
$I_D(Package\ Limited)$	203	A
$Q_G(0V..10V)$	160	nC



Type / Ordering Code	Package	Marking	Related Links
IRF150P220	PG-TO247-3	IRF150P220	-

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**1 Maximum ratings**  
at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	203 316 224	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ (silicon limited) $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ (silicon limited) <sup>1)</sup>
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	812	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	-	-	834	mJ	$I_D=100\text{ A}$ , $R_{GS}=50\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	556 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{THJA}=40\text{ °C/W}^3)$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

**2 Thermal characteristics**

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case <sup>4)</sup>	$R_{thJC}$	-	-	0.27	°C/W	-
Thermal resistance, junction -Ambient	$R_{thJA}$	-	-	40	°C/W	-
Case-to-Sink, Flat Greased Surface	$R_{thCS}$	-	0.24	-	°C/W	-

<sup>1)</sup> See Diagram 3 for more detailed information

<sup>2)</sup> See Diagram 13 for more detailed information

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>4)</sup>  $R_{thJC}$  is measured at  $T_j$  approximately 90°C.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	50	-	mV/°C	$I_D=2\text{ mA}$ , referenced to $25\text{ °C}$
Gate threshold voltage	$V_{GS(th)}$	3	-	4.6	V	$V_{DS}=V_{GS}$ , $I_D=265\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	-	1 100	$\mu\text{A}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.3	2.7	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	0.5	-	$\Omega$	-
Transconductance	$g_{fs}$	-	200	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=100\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	12000	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	3000	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	65	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	33	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Rise time	$t_r$	-	100	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	50	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Fall time	$t_f$	-	85	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	65	-	nC	$V_{DD}=75\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	46	-	nC	$V_{DD}=75\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	32	-	nC	$V_{DD}=75\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	51	-	nC	$V_{DD}=75\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	160	200	nC	$V_{DD}=75\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=75\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	128	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>2)</sup>	$Q_{oss}$	-	451	-	nC	$V_{DD}=75\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

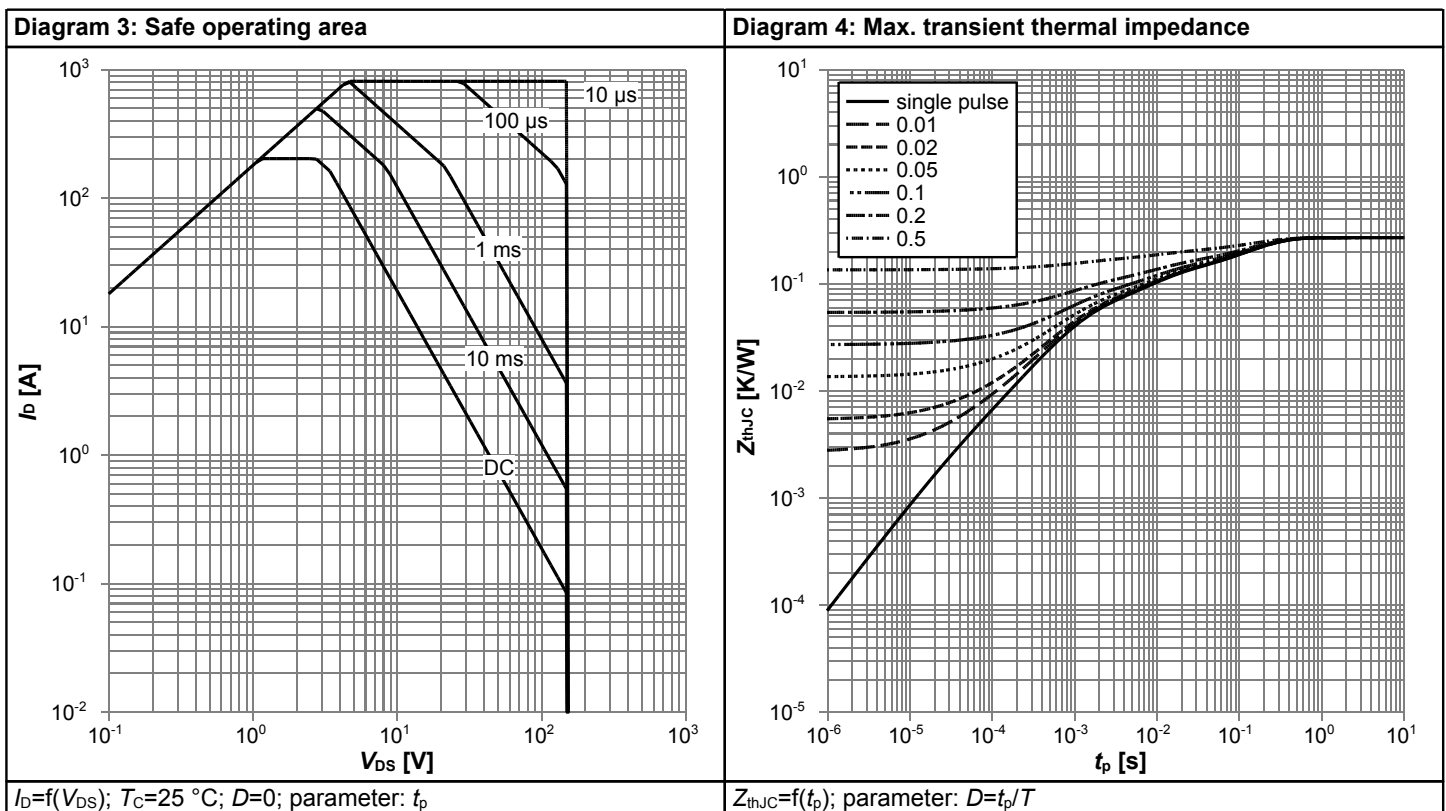
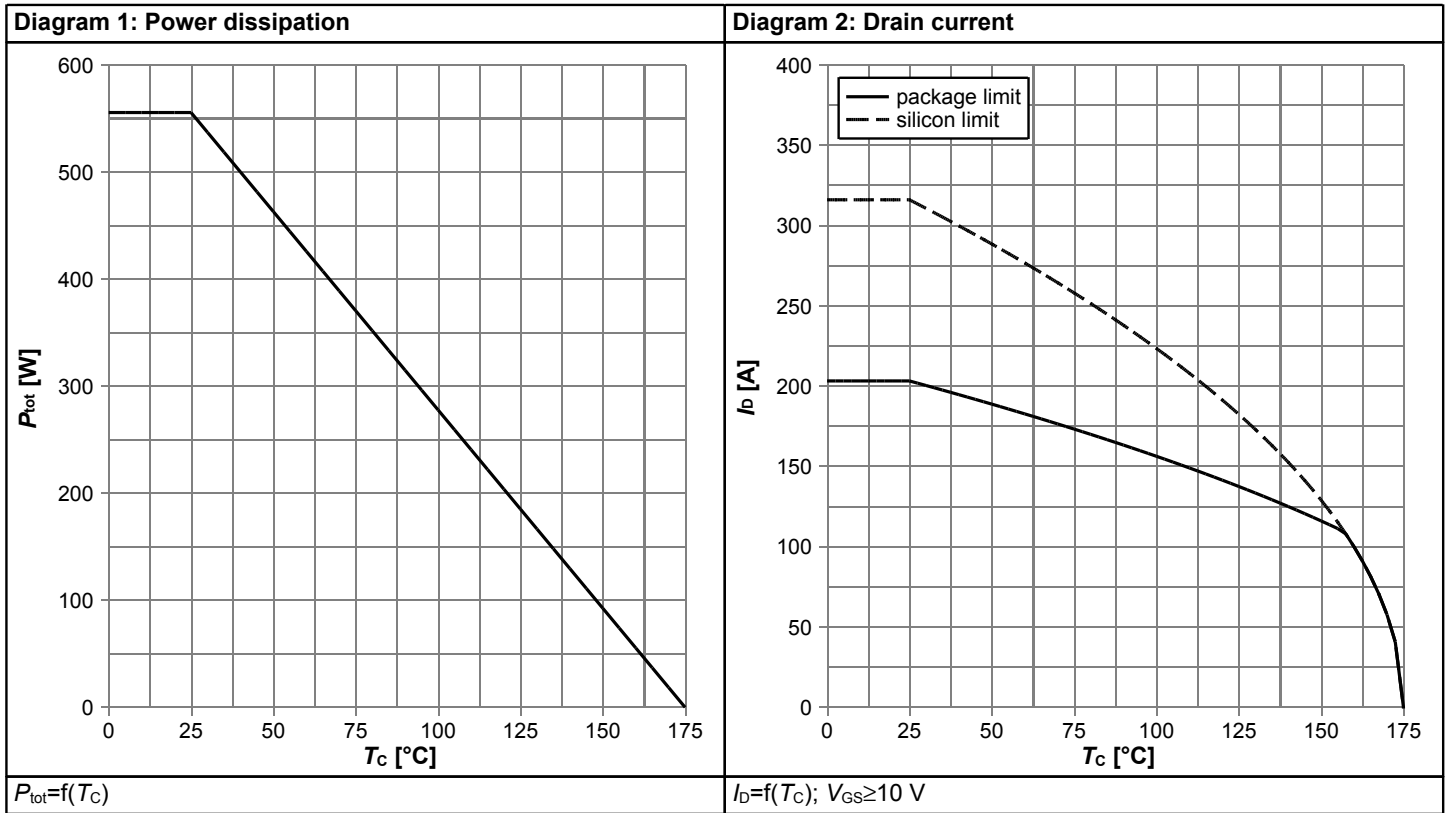
<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

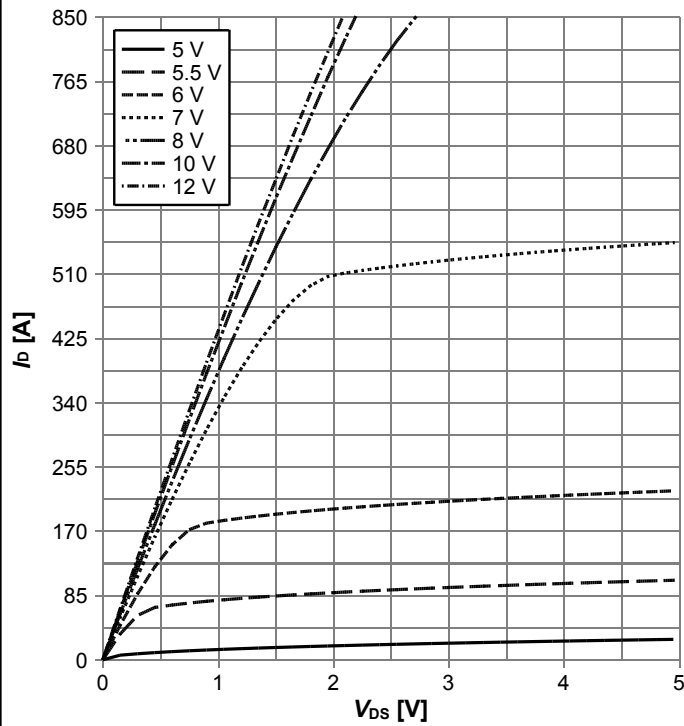
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	203	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	812	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	-	1.1	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	110	-	ns	$V_R=128\text{ V}, I_F=100\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	250	-	nC	$V_R=128\text{ V}, I_F=100\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

## 4 Electrical characteristics diagrams

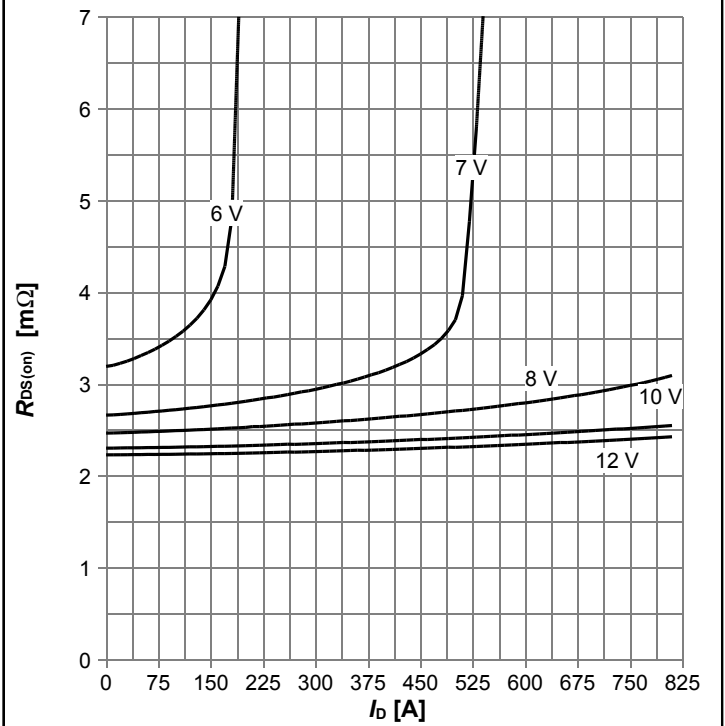


**Diagram 5: Typ. output characteristics**



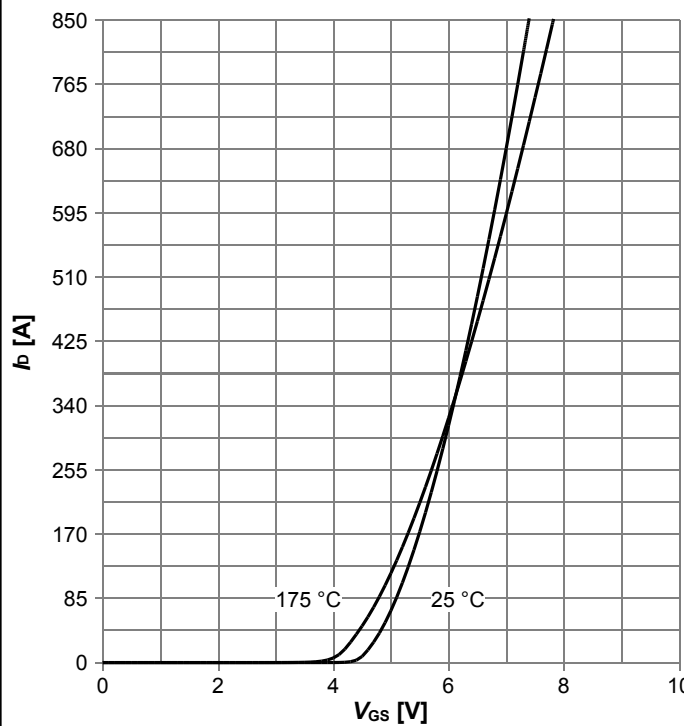
$I_D = f(V_{DS})$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



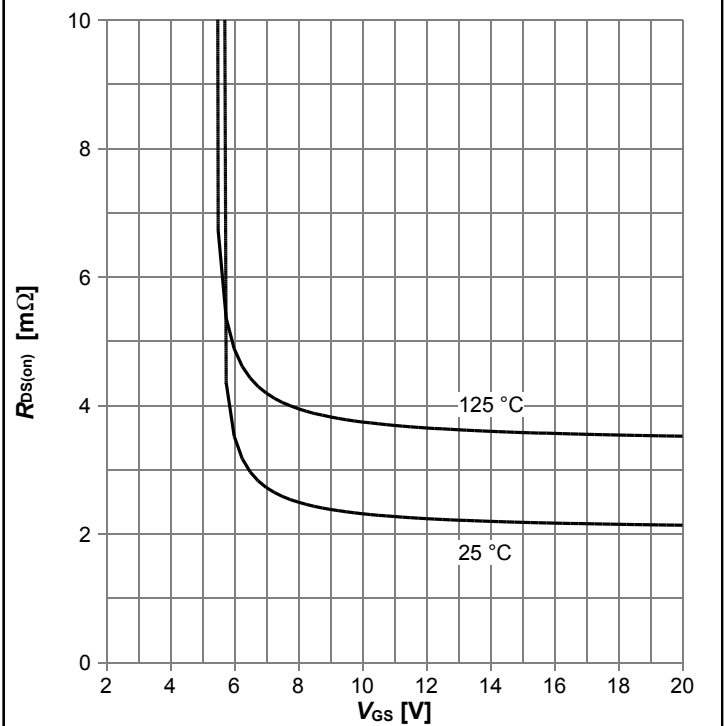
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



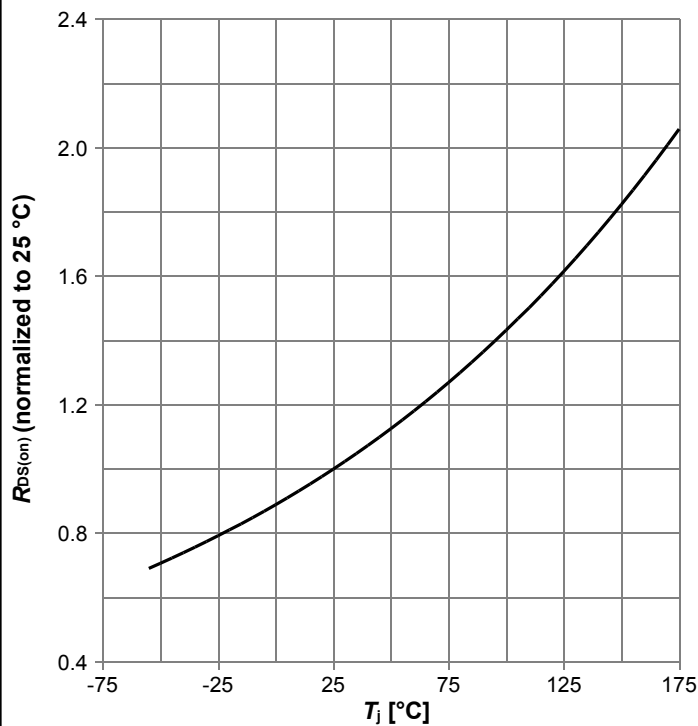
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**



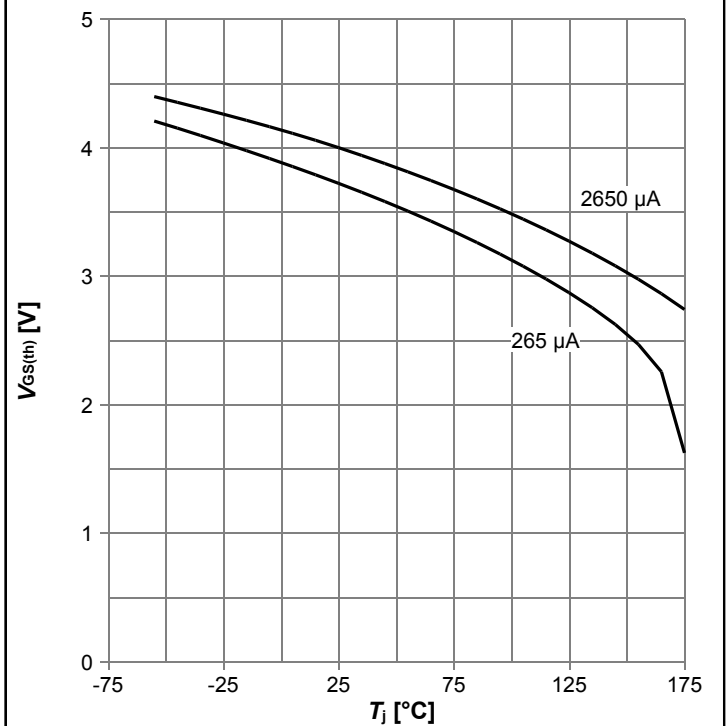
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 100\text{ A}$ ; parameter:  $T_j$

**Diagram 9: Normalized drain-source on resistance**



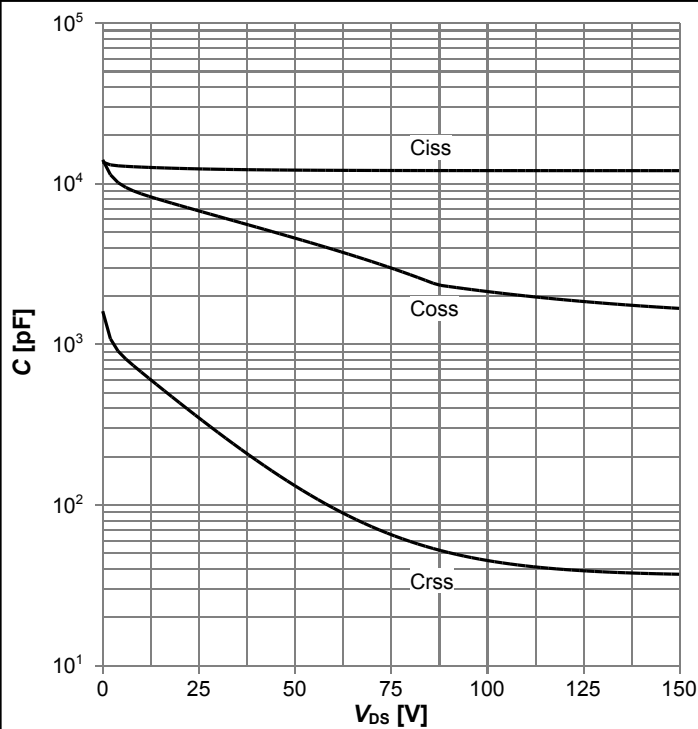
$R_{DS(on)}=f(T_j)$ ,  $I_D=100$  A,  $V_{GS}=10$  V

**Diagram 10: Typ. gate threshold voltage**



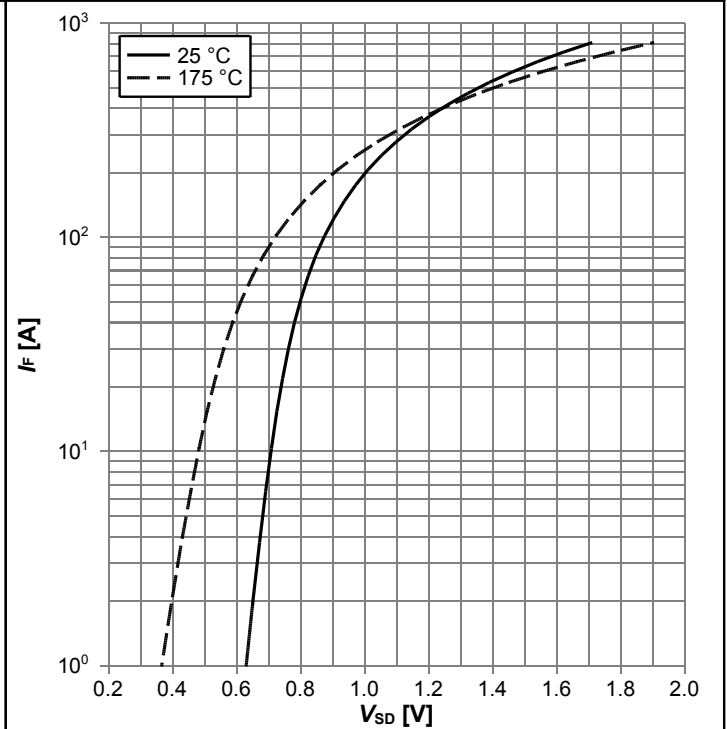
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

**Diagram 11: Typ. capacitances**



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

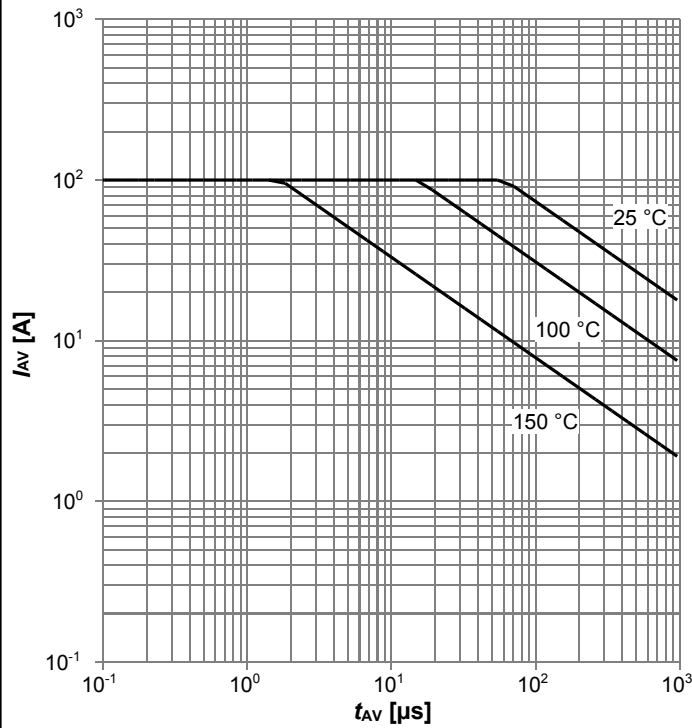
**Diagram 12: Forward characteristics of reverse diode**



$I_F=f(V_{SD})$ ; parameter:  $T_j$

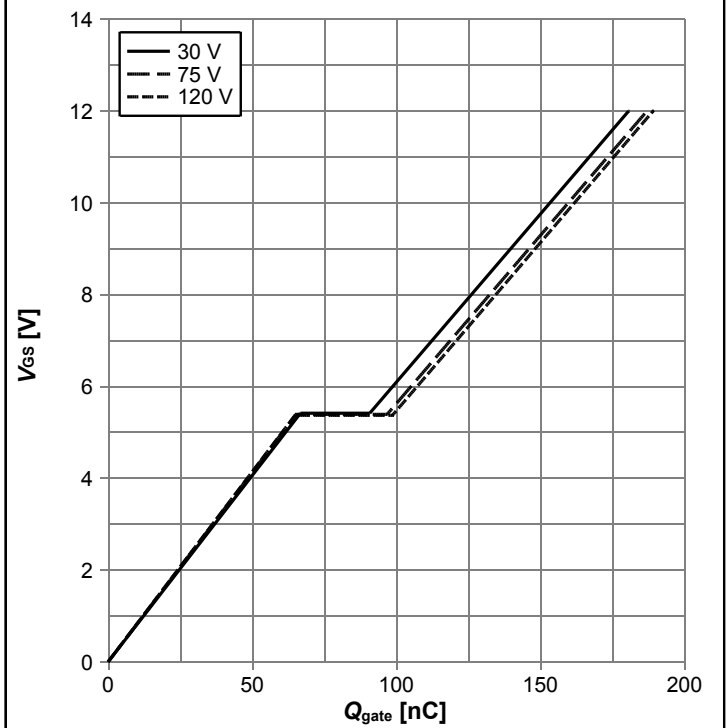


**Diagram 13: Avalanche characteristics**



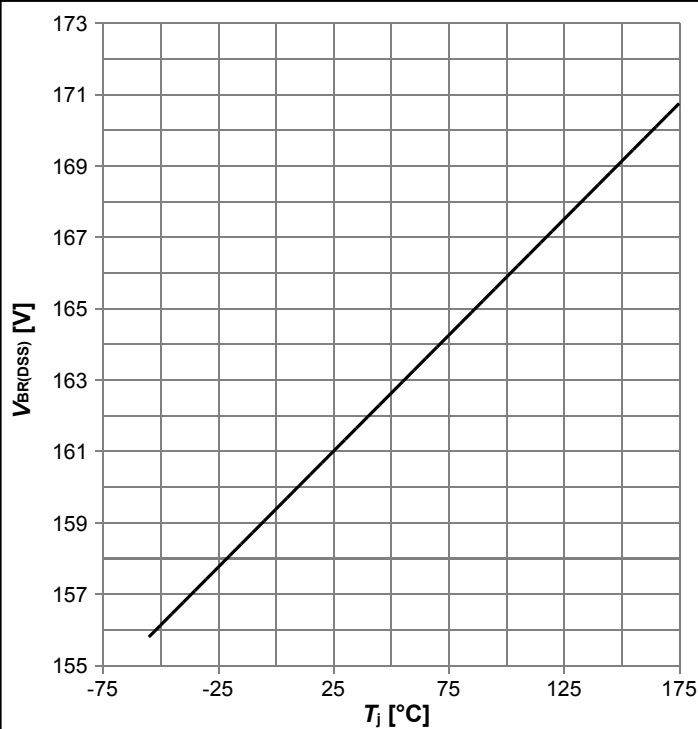
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



$V_{GS}=f(Q_{gate}), I_D=100 \text{ A pulsed}, T_j=25 \text{ °C}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

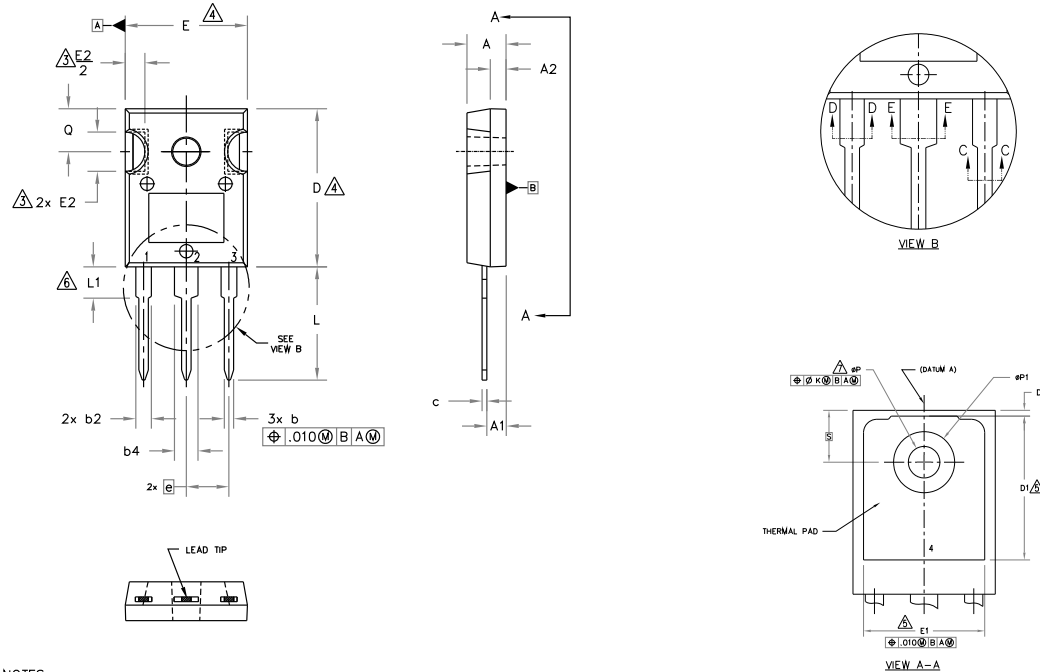


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram Gate charge waveforms**



## 5 Package Outlines



**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
$\phi k$	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
$\phi P$	.140	.144	3.56	3.66	
$\phi P1$	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFET**

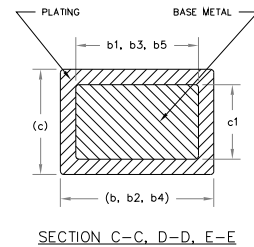
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE



**Figure 1 Outline PG-TO247-3, dimensions in mm/inches**

## Revision History

IRF150P220

**Revision: 2020-02-03, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2018-09-21	Release of preliminary version
2.0	2018-09-21	Release of final version
2.1	2020-02-03	Update from IR MOSFT/StrongIRFET™ to StrongIRFET™

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