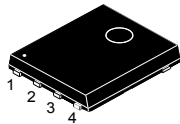
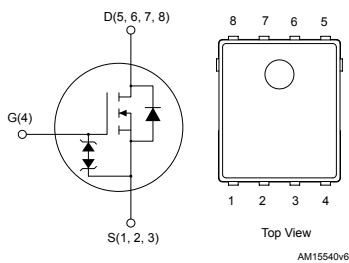


Automotive-grade N-channel 650 V, 0.95 Ω typ., 5 A, MDmesh K5 Power MOSFET in a PowerFLAT 5x6 VHV package



PowerFLAT 5x6 VHV



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL7LN65K5AG	650 V	1.15 Ω	5 A



- AEC-Q101 qualified
- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



Product status link

[STL7LN65K5AG](#)

Product summary

Order code	STL7LN65K5AG
Marking	7LN65K5
Package	PowerFLAT 5x6 VHV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.4	A
$I_D^{(2)}$	Drain current (pulsed)	20	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	79	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	- 55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 5\text{ A}$, di/dt 100 A/ μs ; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 520\text{ V}$.
- $V_{DS} \leq 520\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance, junction-to-case	1.58	$^\circ\text{C/W}$
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	59	$^\circ\text{C/W}$

- When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{Jmax})	1.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200	mJ

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}, T_C = 125\text{ }^\circ\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		0.95	1.15	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	270	-	pF
C_{oss}	Output capacitance		-	22	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(er)}$ ⁽¹⁾	Equivalent capacitance energy related	$V_{DS} = 0\text{ to }520\text{ V}, V_{GS} = 0\text{ V}$	-	20	-	nC
$C_{o(tr)}$ ⁽²⁾	Equivalent capacitance time related		-	57	-	nC
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	7.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 5\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	11.7	-	nC
Q_{gs}	Gate-source charge		-	2.7	-	nC
Q_{gd}	Gate-drain charge		-	7.3	-	nC

1. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

2. Time related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 2.5\text{ A}$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	7.4	-	ns
t_r	Rise time		-	9.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	19.8	-	ns
t_f	Fall time		-	16.4	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	282		ns
Q_{rr}	Reverse recovery charge		-	1.97		μC
I_{RRM}	Reverse recovery current		-	14		A
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	415		ns
Q_{rr}	Reverse recovery charge		-	2.70		μC
I_{RRM}	Reverse recovery current		-	13		A

1. Pulse width is limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30		-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

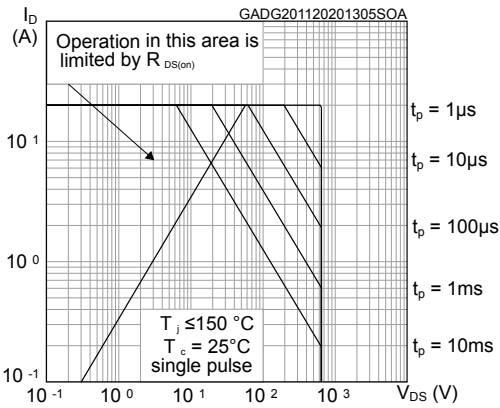


Figure 2. Maximum transient thermal impedance

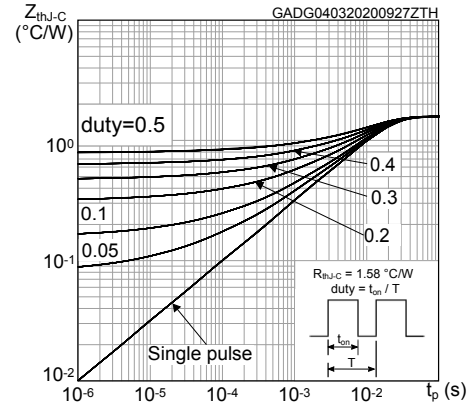


Figure 3. Typical output characteristics

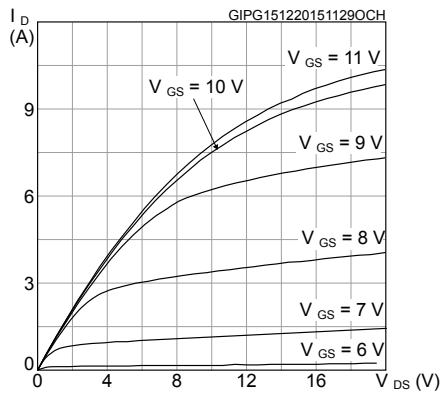


Figure 4. Typical transfer characteristics

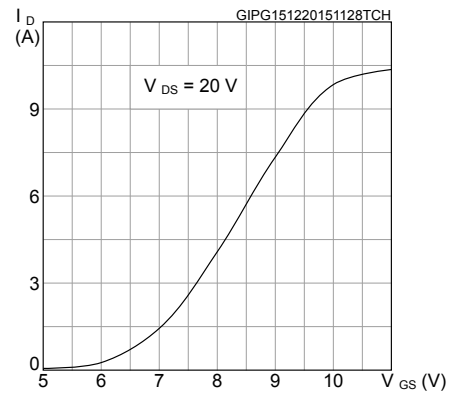


Figure 5. Typical gate charge characteristics

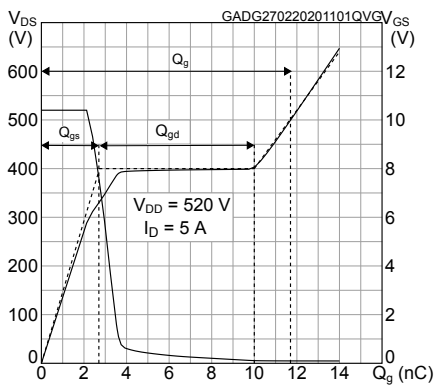


Figure 6. Typical drain-source on-resistance

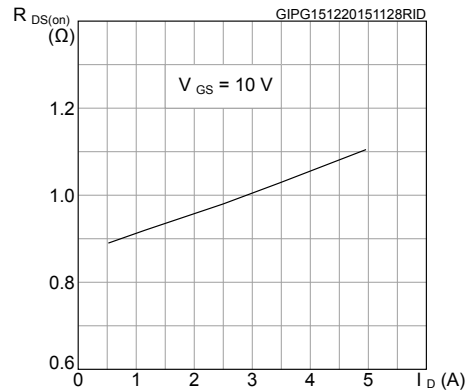


Figure 7. Typical capacitance characteristics

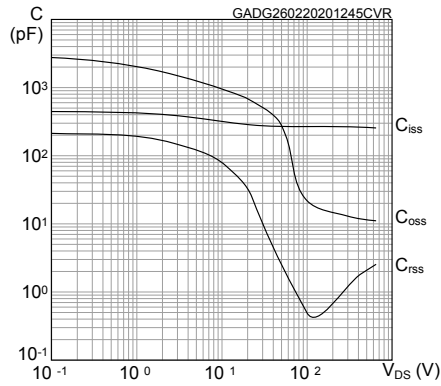


Figure 8. Normalized gate threshold vs temperature

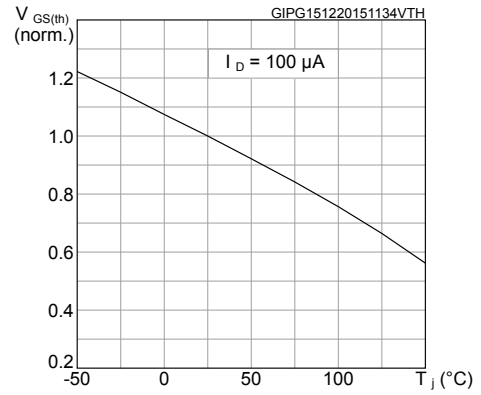


Figure 9. Normalized breakdown voltage vs temperature

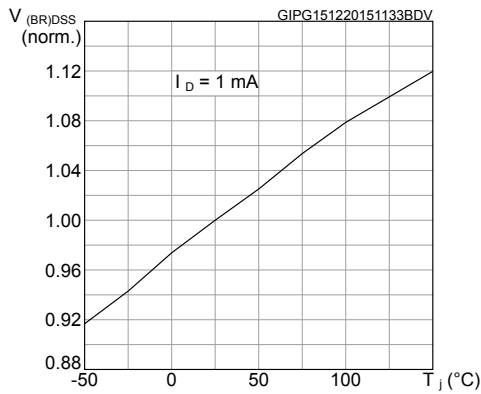


Figure 10. Normalized on-resistance vs temperature

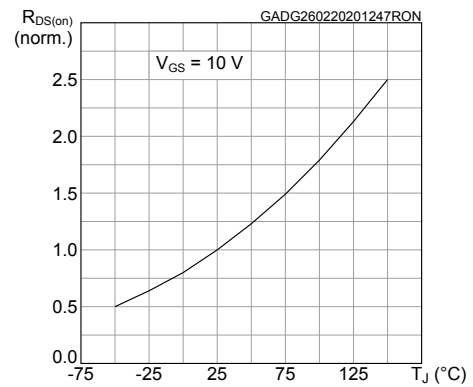


Figure 11. Typical reverse diode forward characteristics

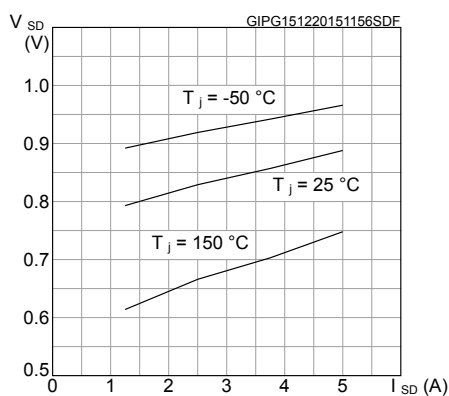
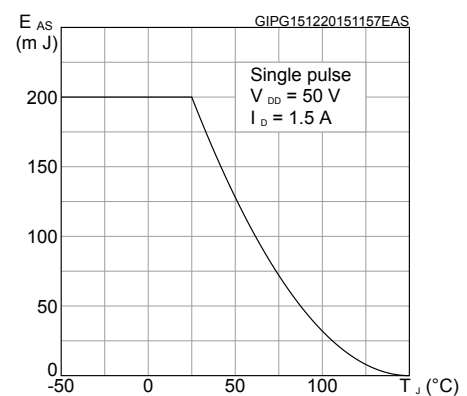
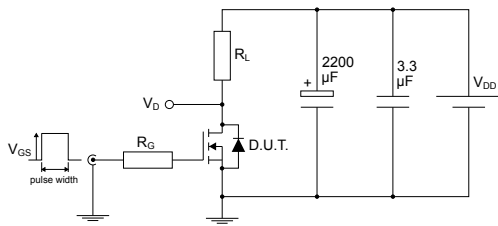


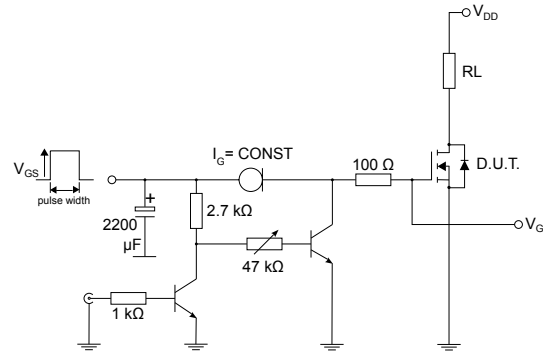
Figure 12. Maximum avalanche energy vs temperature



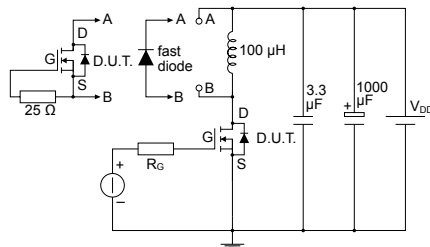
3 Test circuits

Figure 13. Test circuit for resistive load switching times


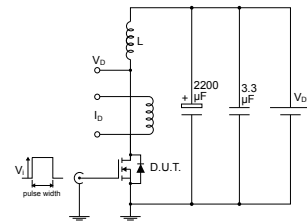
AM01468v1

Figure 14. Test circuit for gate charge behavior


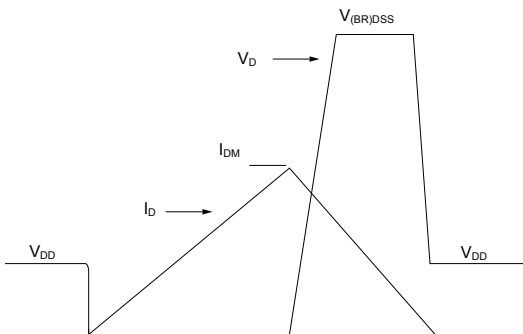
AM01469v10

Figure 15. Test circuit for inductive load switching and diode recovery times


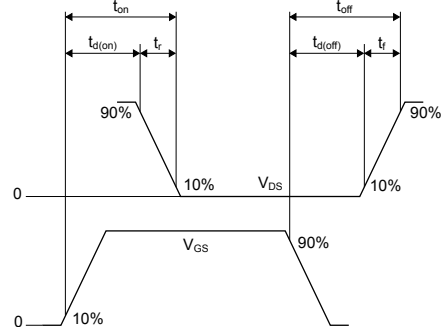
AM01470v1

Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


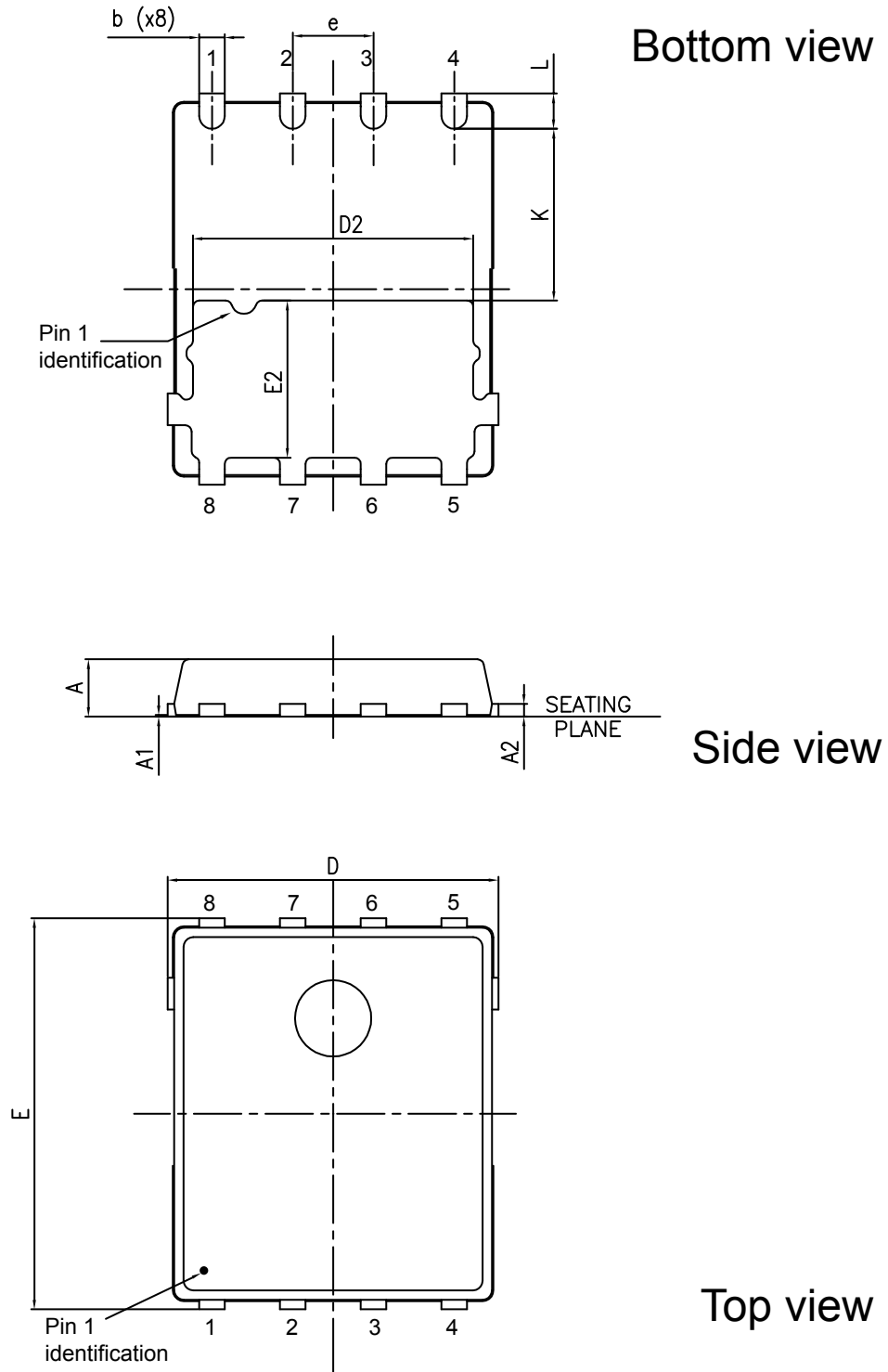
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 VHV mechanical data

Figure 19. PowerFLAT 5x6 VHV package outline

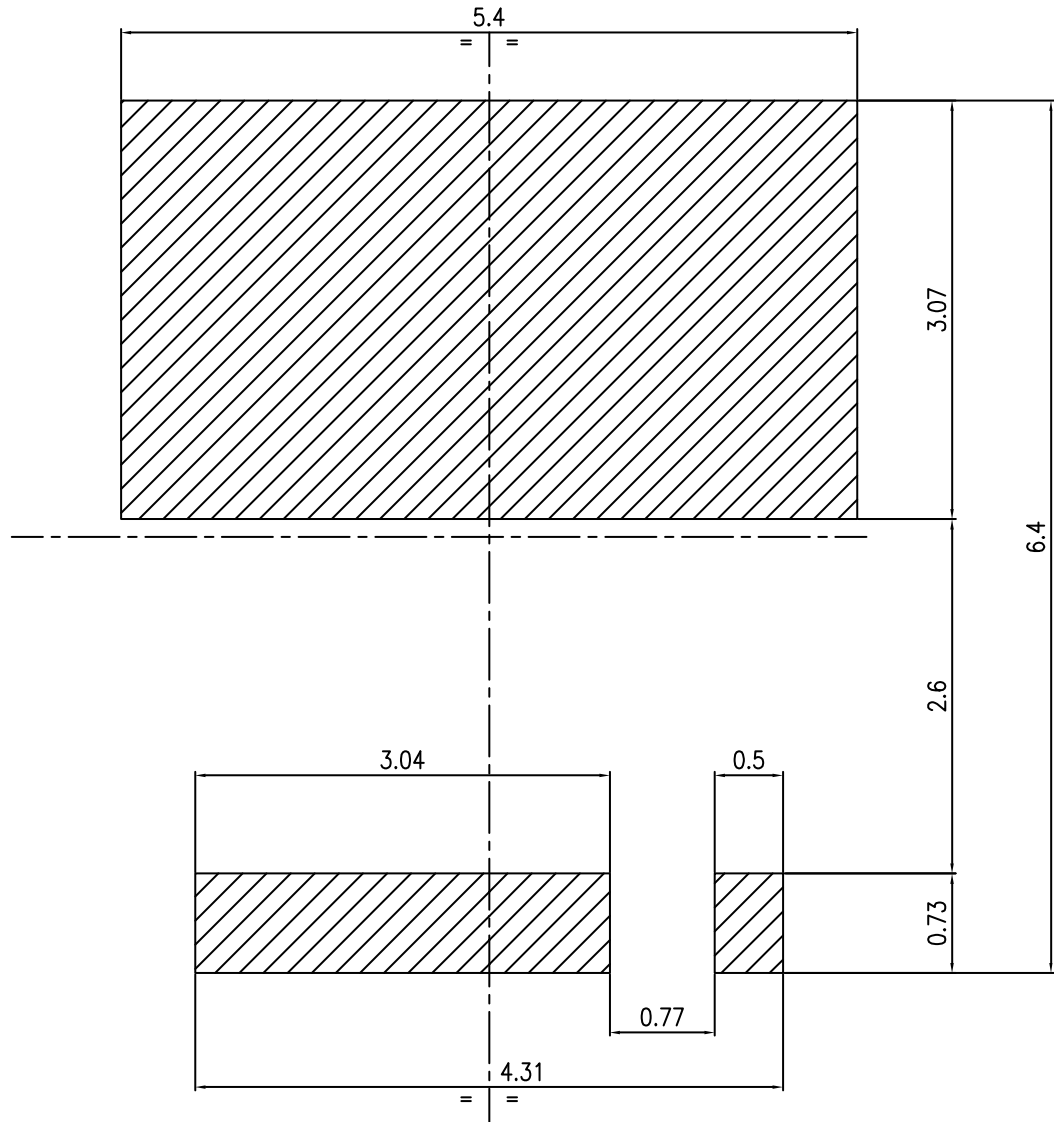


8368144_REV_3

Table 9. PowerFLAT 5x6 VHV package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	2.40	2.50	2.60
e		1.27	
L	0.50	0.55	0.60
K	2.60	2.70	2.80

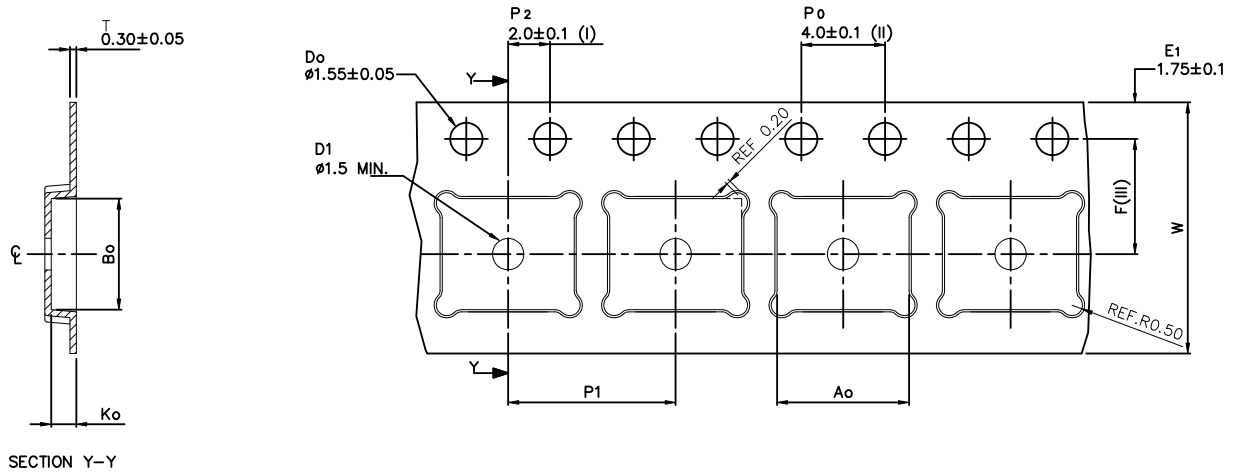
Figure 20. PowerFLAT 5x6 VHV recommended footprint (dimensions are in mm)



8368144_REV_3_footprint

4.2 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



A_0	6.30	+/- 0.1
B_0	5.30	+/- 0.1
K_0	1.20	+/- 0.1
F	5.50	+/- 0.1
P_1	8.00	+/- 0.1
W	12.00	+/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape

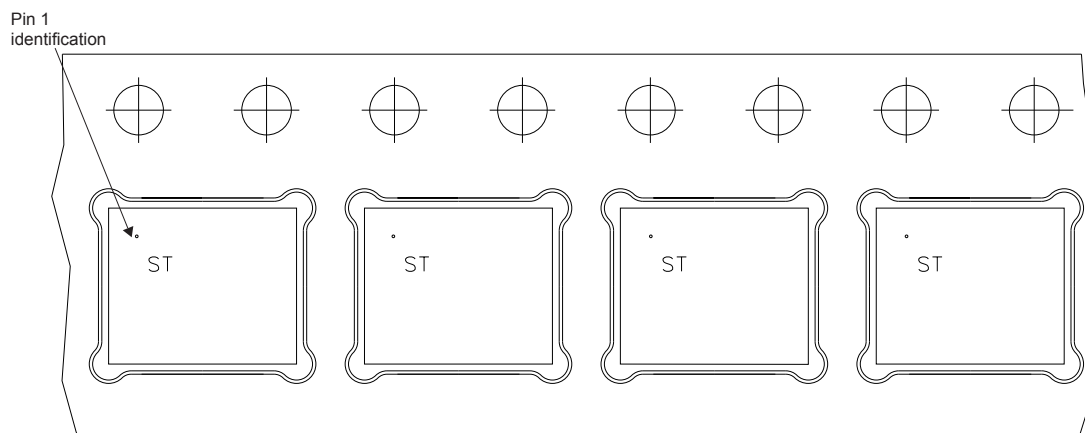
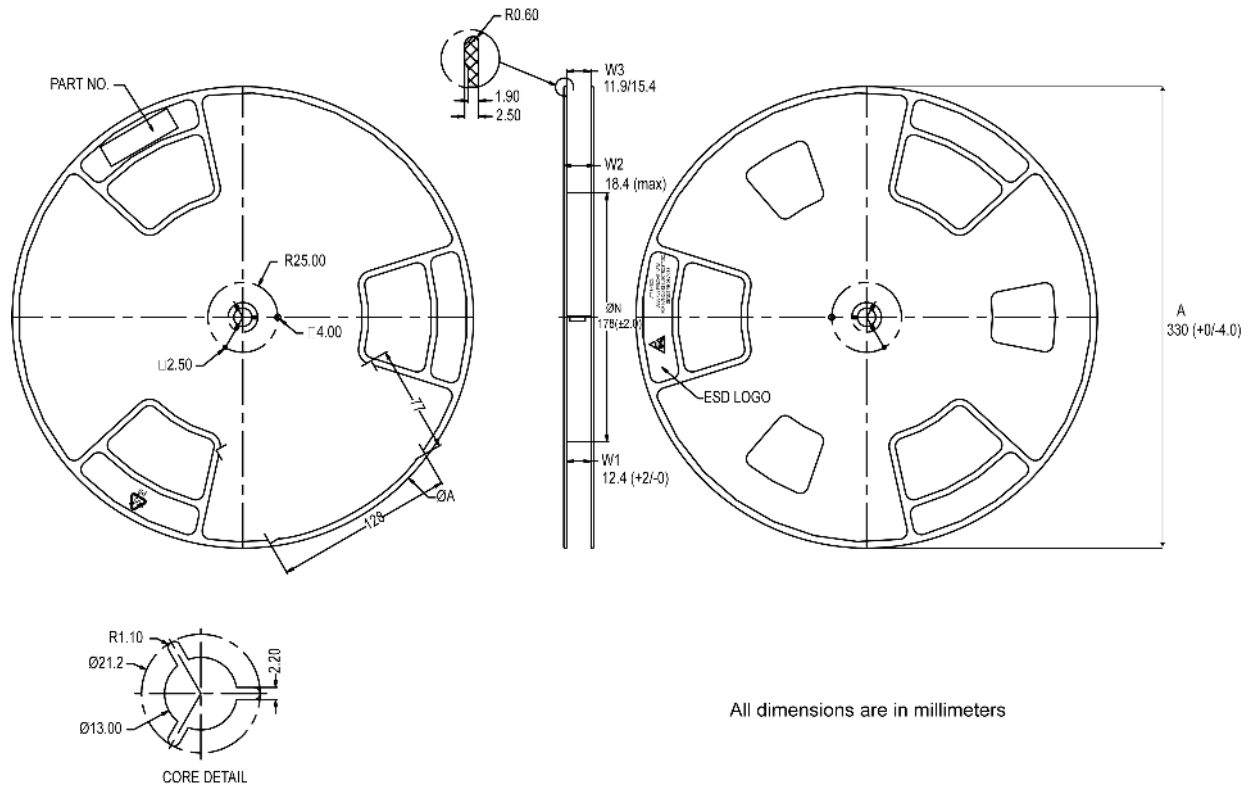


Figure 23. PowerFLAT 5x6 reel



8234350_Reel_rev_C

Revision history

Table 10. Document revision history

Date	Version	Changes
04-Mar-2020	1	First release.
20-Nov-2020	2	Updated Figure 1. Safe operating area. Minor text changes.

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