Laser Printer System Frequency Synthesizer

Features

- **Employs Cypress's proprietary Spread Spectrum technology for EMI suppression**
- **Reduces measured EMI by as much as 10 dB**
- **Four skew-controlled copies of CPU output**
- **Twelve skew-controlled copies of SDRAM output**
- **One copy of 14.31818-MHz Reference output**
- **Separate SS enable pins for Ethernet output and CPU/SDRAM outputs**
- **Selectable SSFTG modulation width**
- **Available in 48-pin SSOP**

Key Specifications

Supply Voltage: ..... V_{DD} = 3.3V ± 10%

CPU Clock Cycle to Cycle Jitter: ..... 250 ps

CPU0:3, SDRAM0:11 Clock Skew: ..... 250 ps

CPU, SDRAM Output on Resistance: 15Ω

Logic inputs have 250 kΩ pull-up resistors

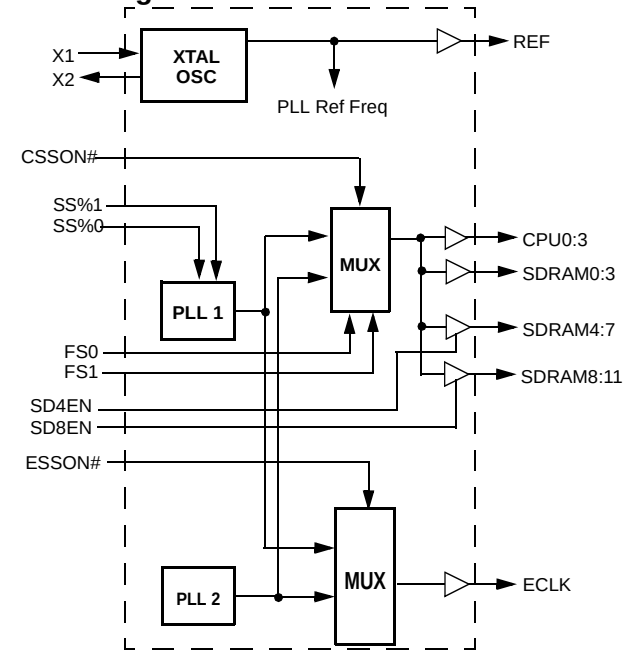
Table 1. Pin-selectable Frequency

FS1	FS0	CPU(0:3), SDRAM(0:11)	ECLK
0	0	reserved	reserved
0	1	100 MHz	50 MHz
1	0	66.6 MHz	50 MHz
1	1	50 MHz	50 MHz

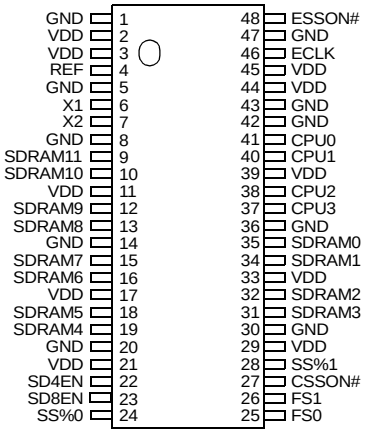
Table 2. Spread Characteristics

SS%1	SS%0	ESSON#	CSSON#	CPU(0:3), SDRAM(0:11)	ECLK
0	0	0	0	–0.5%	–0.5%
0	0	0	1	0 (off)	–0.5%
0	0	1	0	–0.5%	0 (off)
0	0	1	1	0 (off)	0 (off)
0	1	0	0	–1.0%	–1.0%
0	1	0	1	0 (off)	–1.0%
0	1	1	0	–1.0%	0 (off)
0	1	1	1	0 (off)	0 (off)
1	0	0	0	–2.5%	–2.5%
1	0	0	1	0 (off)	–2.5%
1	0	1	0	–2.5%	0 (off)
1	0	1	1	0 (off)	0 (off)
1	1	0	0	–3.75%	–3.75%
1	1	0	1	0 (off)	–3.75%
1	1	1	0	–3.75%	0 (off)
1	1	1	1	0 (off)	0 (off)

Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	41, 40, 38, 37	O	***CPU Clock Outputs:*** These four outputs run at a frequency set by FS0:1. The width of the Spread Spectrum Modulation is enabled by pin CSSON#, and selected by pins SS%0:1.
SDRAM0:11	35, 34, 32, 31, 19, 18, 16, 15, 13, 12, 10, 9	O	***SDRAM Outputs:*** These twelve SDRAM clock outputs run synchronously to the CPU clock. Modulation and frequency follow the CPU outputs.
FS0:1	25, 26	I	***Frequency Selection Inputs:*** Selects CPU clock frequency as shown in *Table 1*.
SS%0:1	24, 28	I	***Modulation Width Selection Inputs:*** These inputs select the width of the Spread Spectrum feature when it is enabled by either CSSON# or ESSON#. See *Table 2*.
ECLK	46	O	***Ethernet Output:*** Timing signal running at 50 MHz when a 14.318-MHz frequency is provided as the reference. The width of the Spread Spectrum Modulation is enabled by pin ESSON# and selected by pins SS%0:1
CSSON#	27	I	***CPU Spread Spectrum Enable Input:*** When this pin is pulled LOW, outputs CPU0:3 and SDRAM0:11 will have the Spread Spectrum Feature enabled.
ESSON#	48	I	***Ethernet Spread Spectrum Enable Input:*** When this pin is pulled LOW, output ECLK will have the Spread Spectrum Feature enabled.
REF	4	O	***Reference Output:*** This output will be equal in frequency to the reference signal provided at X1/X2.
SD4EN	22	I	***SDRAM Bank Disable Input:*** When this pin is pulled LOW, outputs SDRAM4:7 will be disabled to a low state.
SD8EN	23	I	***SDRAM Bank Disable Input:*** When this pin is pulled LOW, outputs SDRAM8:11 will be disabled to a low state.
X1	6	I	***Crystal Connection or External Reference Frequency Input:*** Connect to either a 14.318-MHz crystal or other reference signal.
X2	7	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDD	2, 3, 11, 17, 21, 29, 33, 39, 44, 45	P	***Power Connection:*** Power supply. Connect to 3.3V supply.
GND	1, 5, 8, 14, 20, 30, 36, 42, 43, 47	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is specified in *Table 2*. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for CSSON# and ESSON#. Refer to *Table 2* for more details.

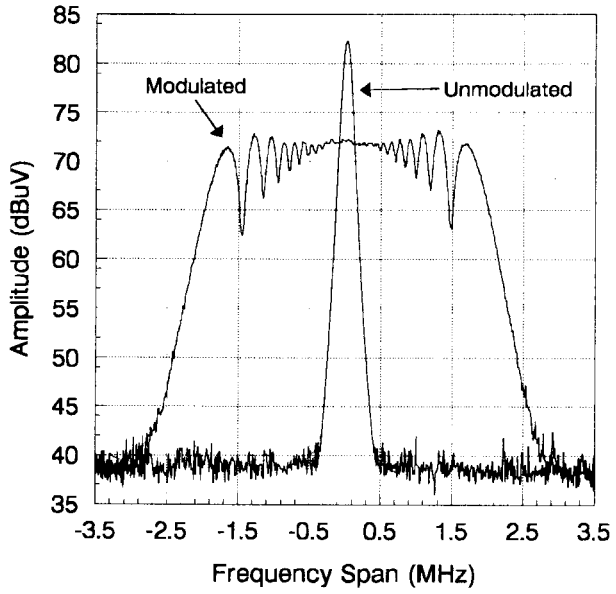


Figure 1. Clock Harmonic With and Without SSCG Modulation Frequency Domain Representation

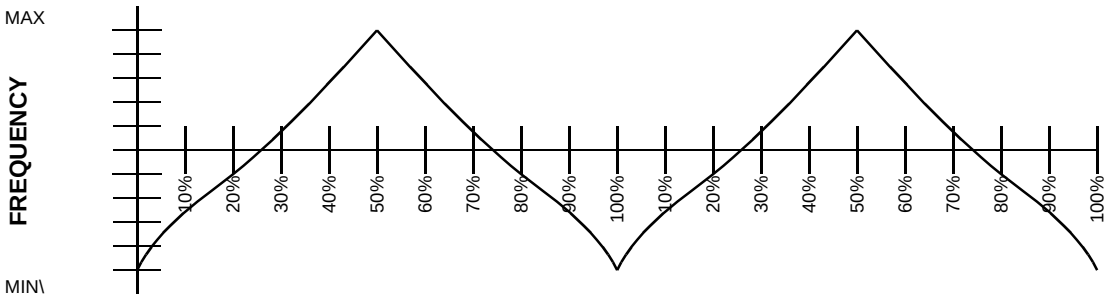


Figure 2. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on Any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DD}	Combined 3.3V Supply Current		CPU0:3 =100 MHz Outputs Loaded[1]		85		mA
Logic Inputs							
V_{IL}	Input Low Voltage			GND – 0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[2]					–25	µA
I_{IH}	Input High Current[2]					10	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage	CPU0:1/IOAPIC	I_{OL} = 1 mA	2.2			V
Crystal Oscillator							
V_{TH}	X1 Input Threshold Voltage[3]				1.5		V
C_{LOAD}	Load Capacitance, as seen by External Crystal[4]				14		pF
$C_{IN,X1}$	X1 Input Capacitance[5]		Pin X2 unconnected		28		pF
Pin Capacitance/Inductance							
C_{IN}	Input Pin Capacitance		Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance					6	pF
L_{IN}	Input Pin Inductance					7	nH

Notes:

1. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
2. W154 logic inputs have internal pull-up resistors.
3. X1 input threshold voltage (typical) is $V_{DD}/2$.
4. The W154 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A = 0°C to +70°C; V_{DD} = 3.3V±5%; f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs CPU0:3 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25.	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V.	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V.	5.0			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V.	0.4		1.6	0.4		1.6	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V.	0.4		1.6	0.4		1.6	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V.	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V.			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

SDRAM Clock Outputs SDRAM0:11 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25.	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V.	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V.	5.0			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V.	0.4		1.6	0.4		1.6	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V.	0.4		1.6	0.4		1.6	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V.	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V.			250			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

REF Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator.		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V.	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V.	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V.	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

ECLK Output (Lump Capacitance Test Load = 20 pF)

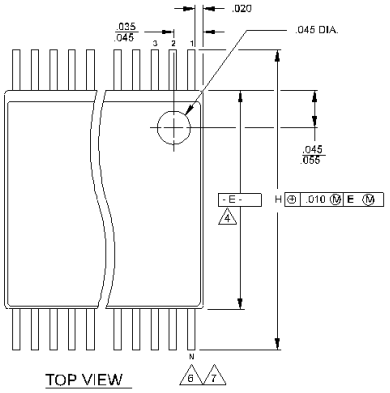
Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V.	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V.	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V.	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

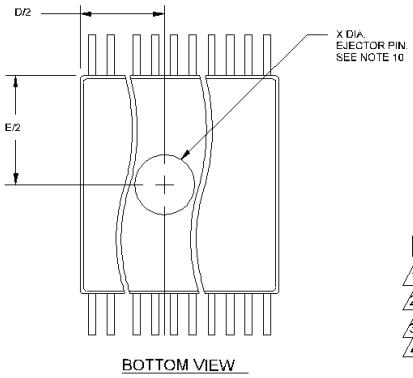
Ordering Information

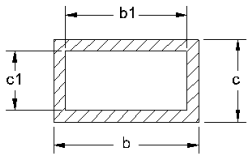
Ordering Code	Package Name	Package Type
W154	H	48-pin SSOP

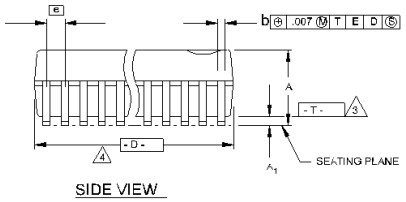
Package Diagram

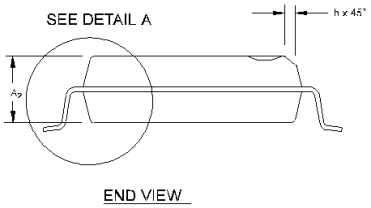
48-pin Shrink Small Outline Package (SSOP, 300 mils)

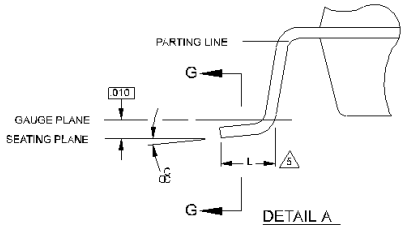












NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .005 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS				NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D			N
						MIN.	NOM.	MAX.	
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
θ	0°	5°	8°						

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS				NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D			N
						MIN.	NOM.	MAX.	
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
θ	0°	5°	8°						

THIS TABLE IN MILLIMETERS

Document Title: W154 Laser Printer System Frequency Synthesizer Document Number: 38-07314				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113223	04/04/02	IKA	Convert from ICW format to Cypress format