

General Description

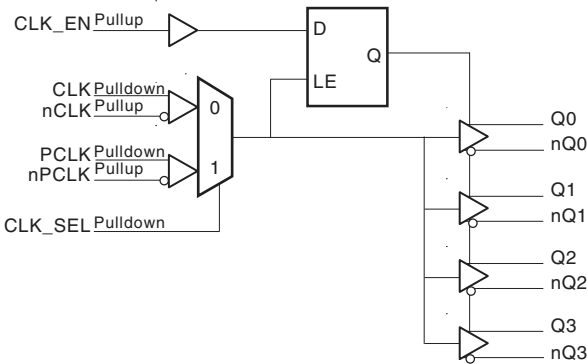
The 8523 is a low skew, high performance 1-to-4 Differential-to-HSTL Fanout Buffer. The 8523 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 8523 ideal for those applications demanding well defined performance and repeatability.

Features

- Four differential output HSTL compatible outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSSL, SSTL
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to HSTL levels with resistor bias on nCLK input
- Additive phase jitter, RMS: 0.082ps (typical), 100MHz f_{OUT}
- Additive phase jitter, RMS: 0.190ps (typical), 120MHz f_{OUT}
- Output skew: 30ps (maximum)
- Part-to-part skew: 200ps (maximum)
- 3.3V core, 1.8V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment

| | | | |
|---------|----|----|------|
| GND | 1 | 20 | Q0 |
| CLK_EN | 2 | 19 | nQ0 |
| CLK_SEL | 3 | 18 | VDDO |
| CLK | 4 | 17 | Q1 |
| nCLK | 5 | 16 | nQ1 |
| PCLK | 6 | 15 | Q2 |
| nPCLK | 7 | 14 | nQ2 |
| nc | 8 | 13 | VDDO |
| nc | 9 | 12 | Q3 |
| VDD | 10 | 11 | nQ3 |

8523
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|--------|------------------|--------|----------|--|
| 1 | GND | Power | | Power supply ground. |
| 2 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS / LVTTTL interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects differential PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTTL interface levels. |
| 4 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 5 | nCLK | Input | Pullup | Inverting differential clock input. |
| 6 | PCLK | Input | Pulldown | Non-inverting differential LVPECL clock input. |
| 7 | nPCLK | Input | Pullup | Inverting differential LVPECL clock input. |
| 8, 9 | nc | Unused | | No connect. |
| 10 | V _{DD} | Power | | Positive supply pin. |
| 11, 12 | nQ3, Q3 | Output | | Differential output pair. HSTL interface levels. |
| 13, 18 | V _{DDO} | Power | | Output supply pins. |
| 14, 15 | nQ2, Q2 | Output | | Differential output pair. HSTL interface levels. |
| 16, 17 | nQ1, Q1 | Output | | Differential output pair. HSTL interface levels. |
| 19, 20 | nQ0, Q0 | Output | | Differential output pair. HSTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

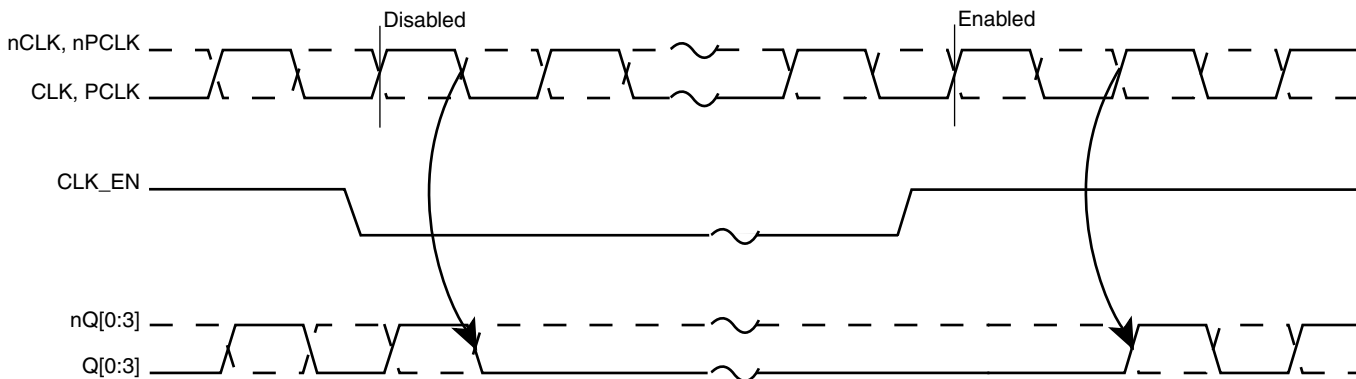
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

Function Tables

Table 3A. Control Input Function Table

| Inputs | | | Outputs | |
|--------|---------|-----------------|---------------|----------------|
| CLK_EN | CLK_SEL | Selected Source | Q[0:3] | nQ[0:3] |
| 0 | 0 | CLK, nCLK | Disabled; LOW | Disabled; HIGH |
| 0 | 1 | PCLK, nPCLK | Disabled; LOW | Disabled; HIGH |
| 1 | 0 | CLK, nCLK | Enabled | Enabled |
| 1 | 1 | PCLK, nPCLK | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.


Figure 1. CLK_EN Timing Diagram
Table 3B. Clock Input Function Table

| Inputs | | Outputs | | Input to Output Mode | Polarity |
|----------------|----------------|---------|---------|------------------------------|---------------|
| CLK or PCLK | nCLK or nPCLK | Q[0:3] | nQ[0:3] | | |
| 0 | 0 | LOW | HIGH | Differential to Differential | Non-Inverting |
| 1 | 1 | HIGH | LOW | Differential to Differential | Non-Inverting |
| 0 | Biased; NOTE 1 | LOW | HIGH | Single-Ended to Differential | Non-Inverting |
| 1 | Biased; NOTE 1 | HIGH | LOW | Single-Ended to Differential | Non-Inverting |
| Biased; NOTE 1 | 0 | HIGH | LOW | Single-Ended to Differential | Inverting |
| Biased; NOTE 1 | 1 | LOW | HIGH | Single-Ended to Differential | Inverting |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 73.2°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 1.6 | 1.8 | 2.0 | V |
| I_{DD} | Power Supply Current | | | | 50 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-----------------|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK_EN | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| | | CLK_SEL | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | CLK_EN | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |
| | | CLK_SEL | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |

Table 4C. Differential DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|-----------------|--------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | nCLK | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| | | CLK | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | nCLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |
| | | CLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |
| V_{PP} | Peak-to-Peak Voltage; NOTE 1 | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | 0.5 | | $V_{DD} - 0.85$ | V |

NOTE 1: V_{IL} should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as V_{IH} .

Table 4D. LVPECL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------------------|-----------------|--------------------------------|---------|----------|---------|
| I_{IH} | Input High Current | nPCLK | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| | | PCLK | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | nPCLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |
| | | PCLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |
| V_{PP} | Peak-to-Peak Voltage | | 0.3 | | 1.0 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1 | | 1.5 | | V_{DD} | V |

NOTE 1: Common mode input voltage is defined as V_{IH} .

Table 4E. HSTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|--------------------------------------|--|---------|---------|--|-------|
| V_{OH} | Output High Current; NOTE 1 | | 0.9 | | 1.4 | V |
| V_{OL} | Output Low Current; NOTE 1 | | 0 | | 0.4 | V |
| V_{OX} | Output Crossover Voltage | $40\% \times (V_{OH} - V_{OL}) + V_{OL}$ | | | $60\% \times (V_{OH} - V_{OL}) + V_{OL}$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.75 | | 1.25 | V |

NOTE 1: Outputs termination with 50Ω to ground.

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---|---|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | | | 650 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | $f \leq 650MHz$ | 1.0 | | 1.6 | ns |
| τ_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | $f_{OUT} = 100MHz,$ Integration Range: 12kHz - 20MHz | | 0.082 | | ps |
| | | $f_{OUT} = 120MHz,$ Integration Range: 12kHz - 20MHz | | 0.190 | | ps |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | | | | 30 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | | 200 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% @ 50MHz | 250 | | 700 | ps |
| odc | Output Duty Cycle | | 45 | | 55 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at 500MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at output differential cross points.

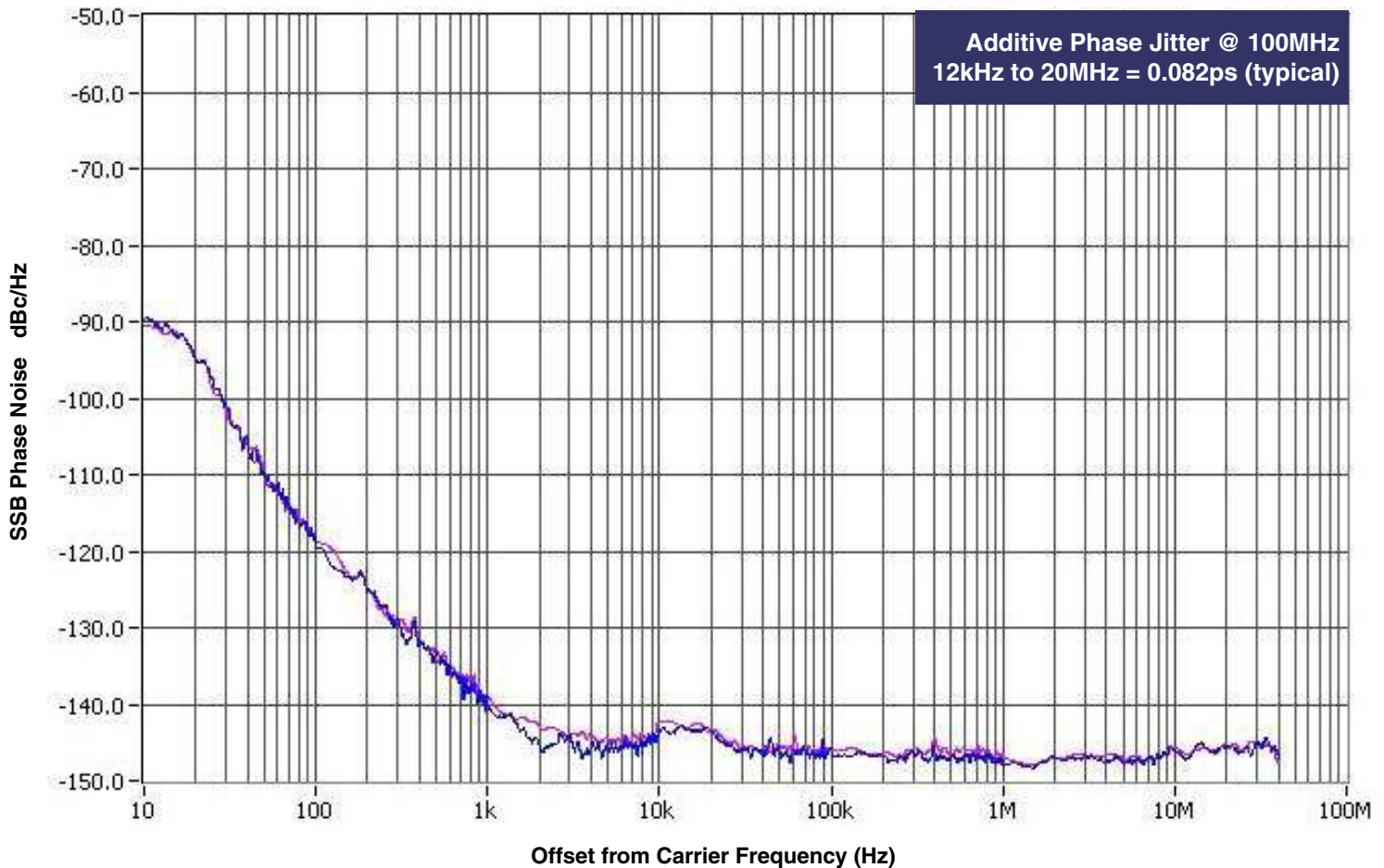
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

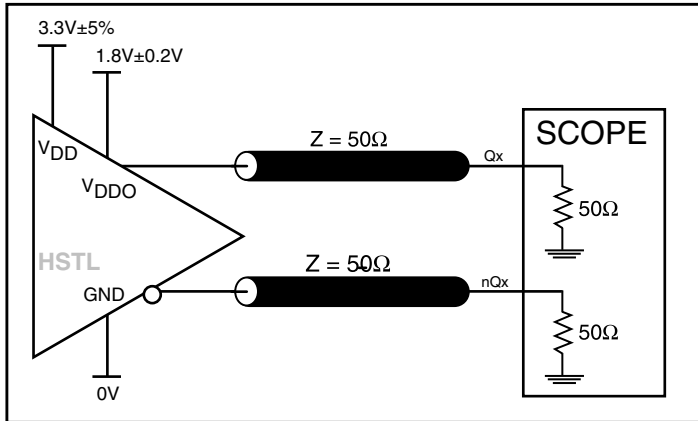
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



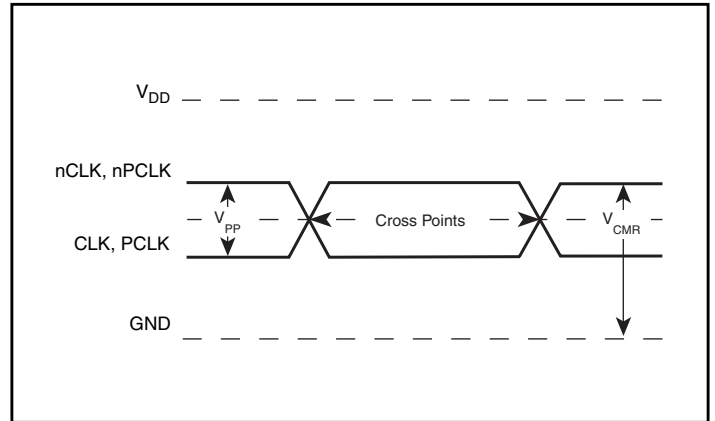
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator used is, "IFR2042 into a Hewlett Packard 8133A 3GHz Pulse Generator".

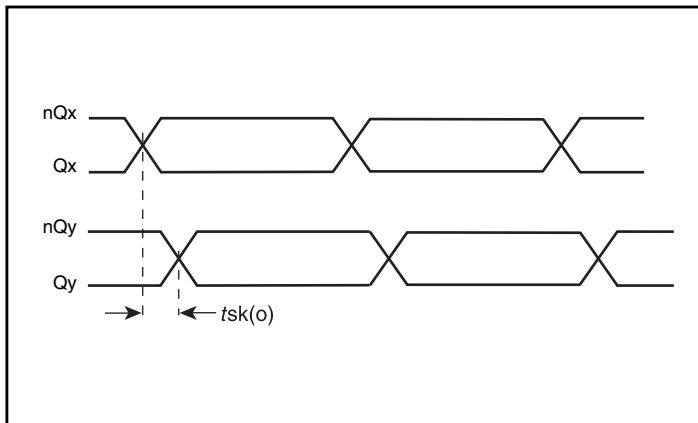
Parameter Measurement Information



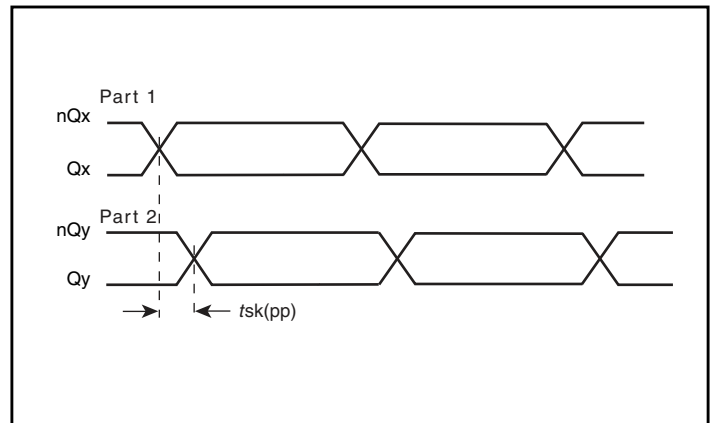
3.3V/1.8V Output Load AC Test Circuit



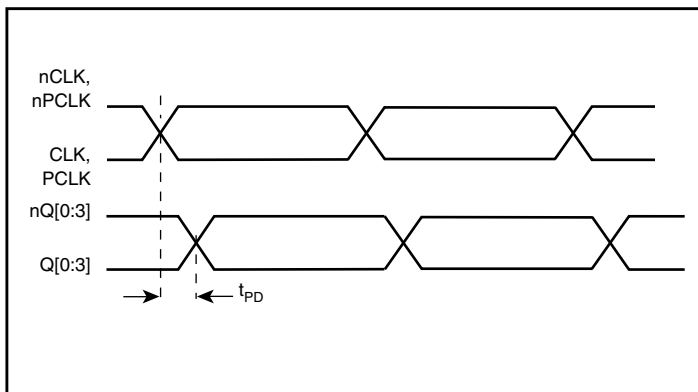
Differential Input Level



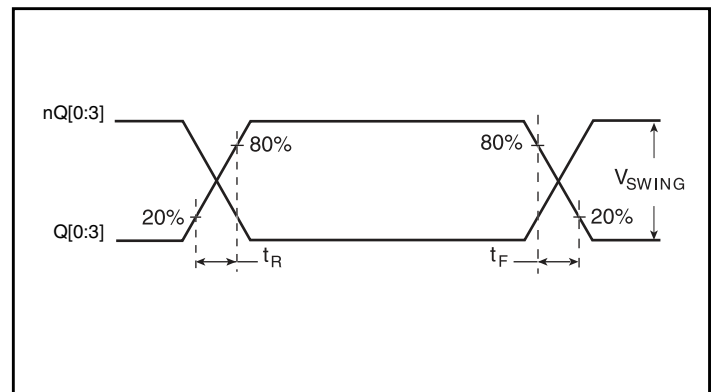
Output Skew



Part-to-Part Skew

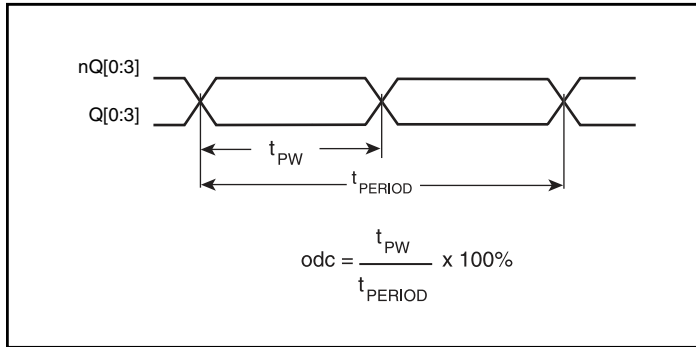


Propagation Delay



Output Rise/Fall Time

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than $V_{CC} + 0.3V$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

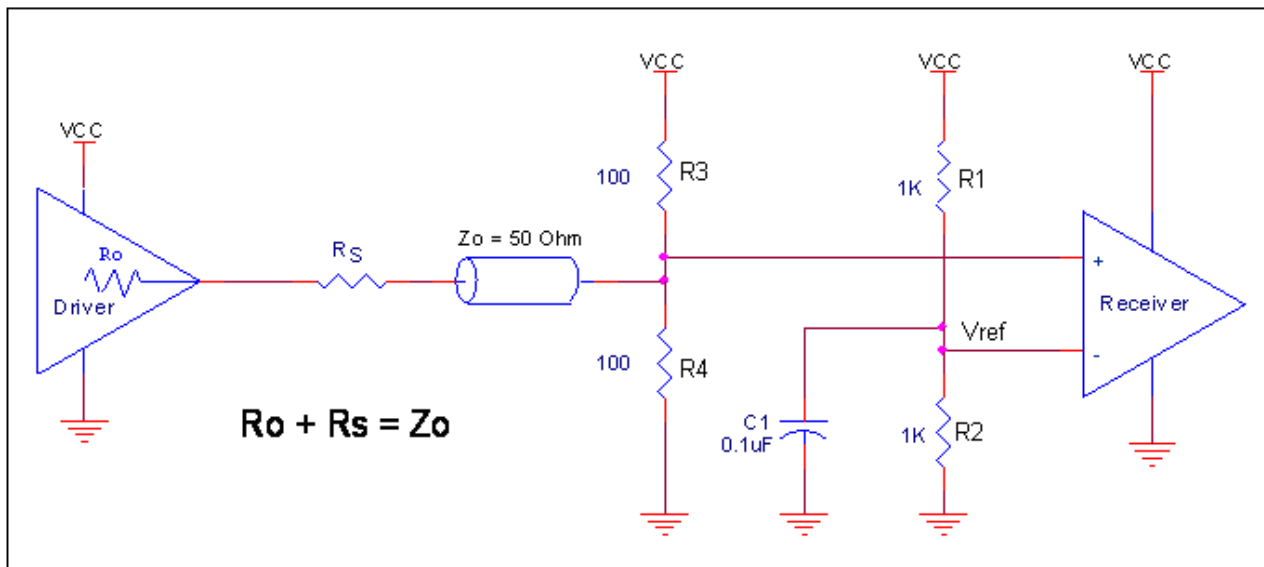


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

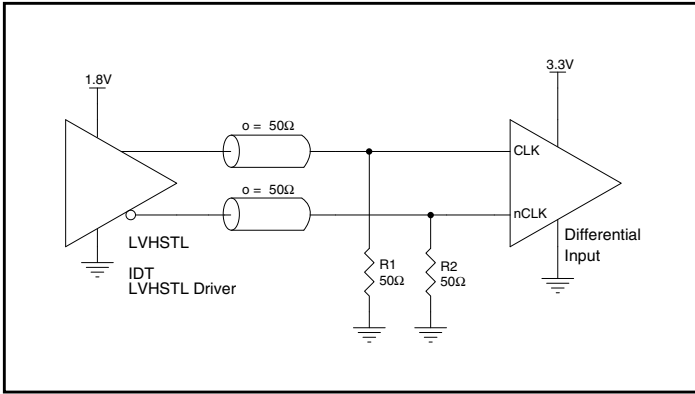


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

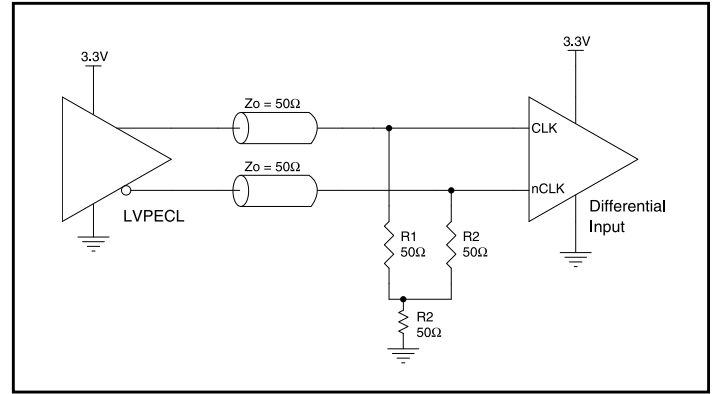


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

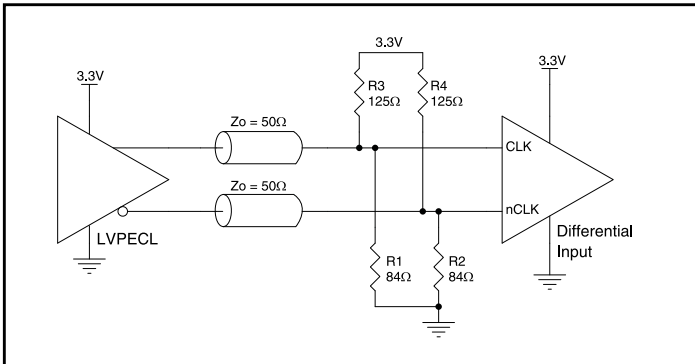


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

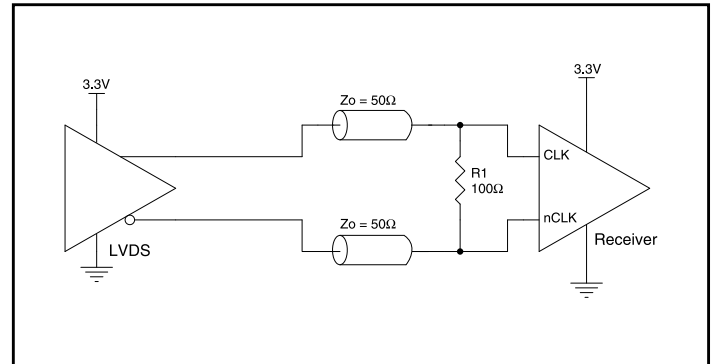


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

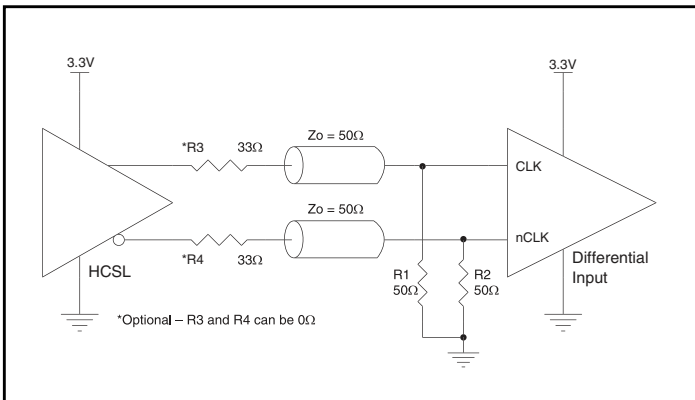


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

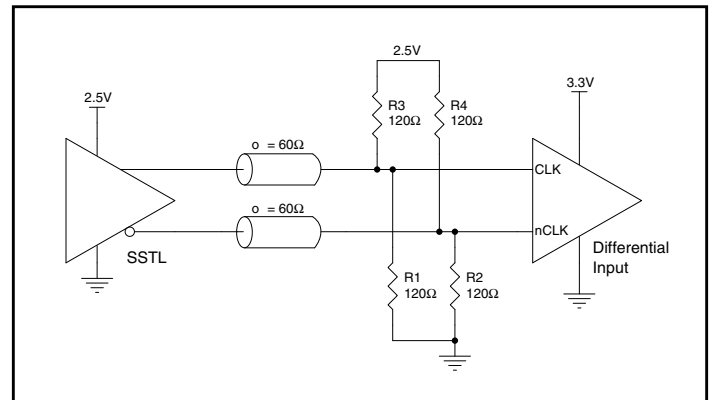


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

3.3V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

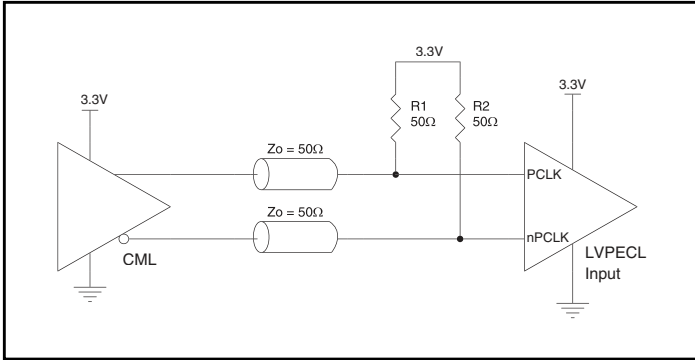


Figure 4A. PCLK/nPCLK Input Driven by a CML Driver

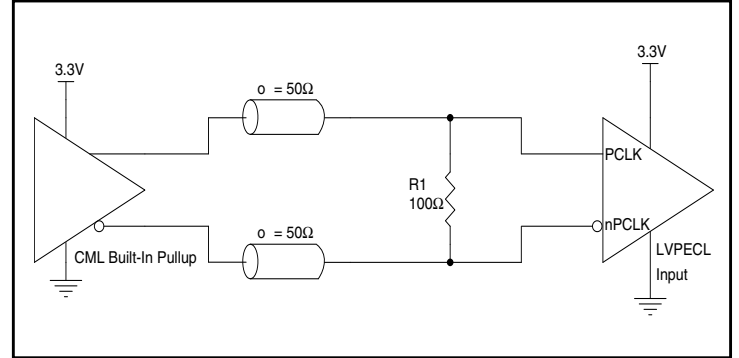


Figure 4B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

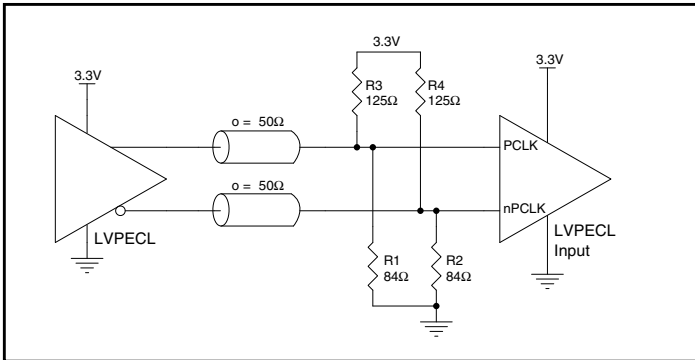


Figure 4C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

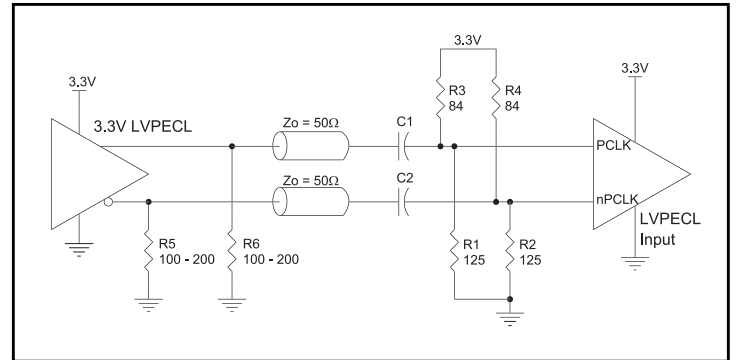


Figure 4D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

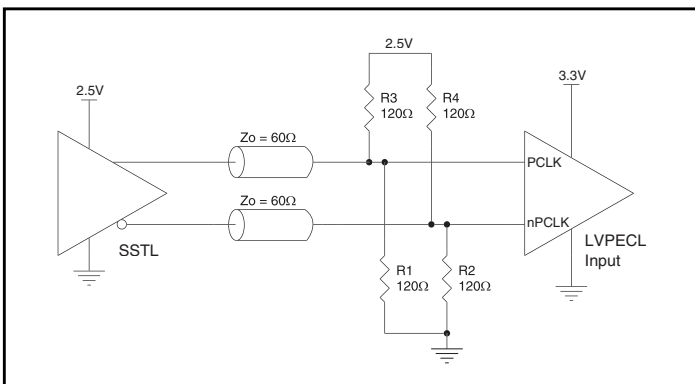


Figure 4E. PCLK/nPCLK Input Driven by an SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from CLK to ground.

PCLK/nPCLK Inputs

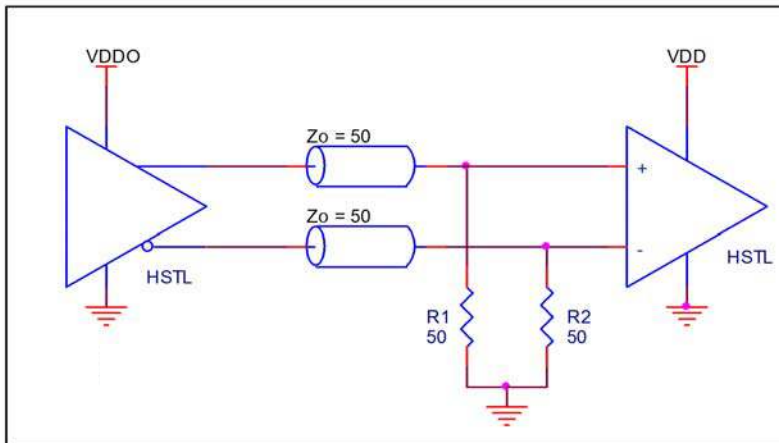
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from PCLK to ground.

Outputs:

HSTL Outputs

All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

HSTL Output Termination



Schematic Example

Figure 5 shows a schematic example of the 8523. In this example, the input is driven by an IDT HSTL driver. The decoupling capacitors

should be physically located near the power pin. For 8523, the unused clock outputs can be left floating.

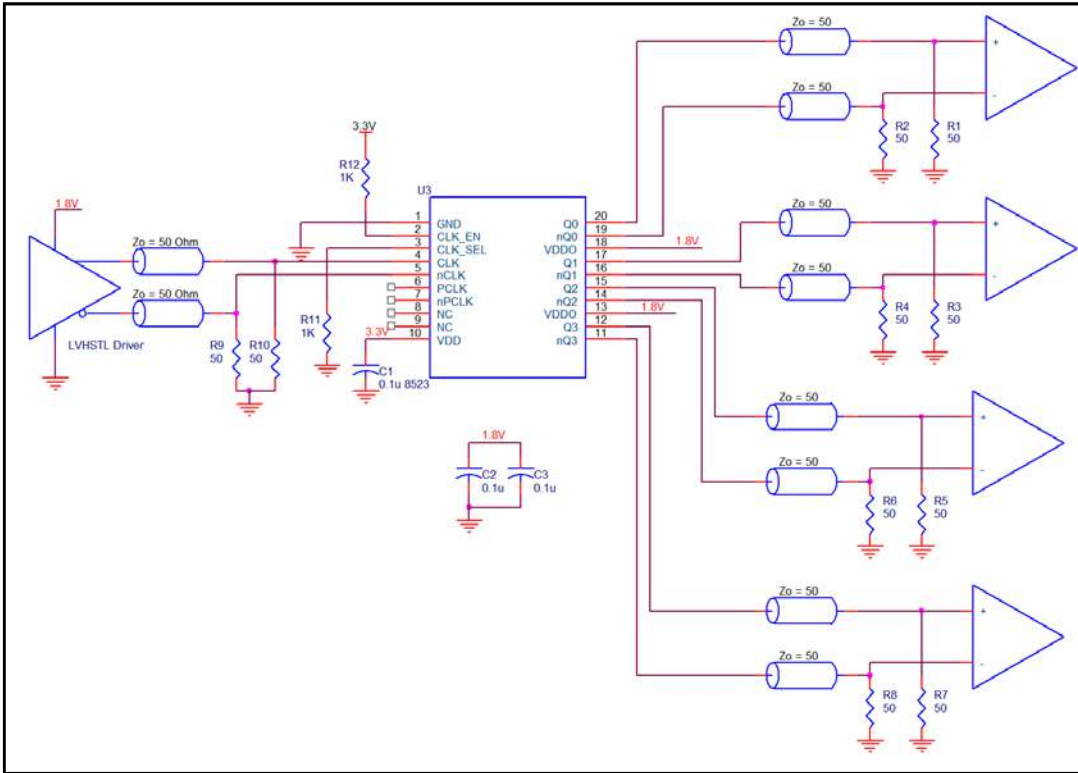


Figure 5. 8523 HSTL Buffer Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8523. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8523 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.465V * 50mA = 173.3mW$
- Power (outputs)_{MAX} = **32.6mW/Loaded Output pair**
If all outputs are loaded, the total power is $4 * 32.6mW = 130.4mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $173.3mW + 130.4mW = 303.7mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.304W * 66.6^\circ C/W = 90.2^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

| Linear Feet per Minute | θ_{JA} by Velocity | | |
|--|---------------------------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the HSTL output pair.

HSTL output driver circuit and termination are shown in *Figure 6*.

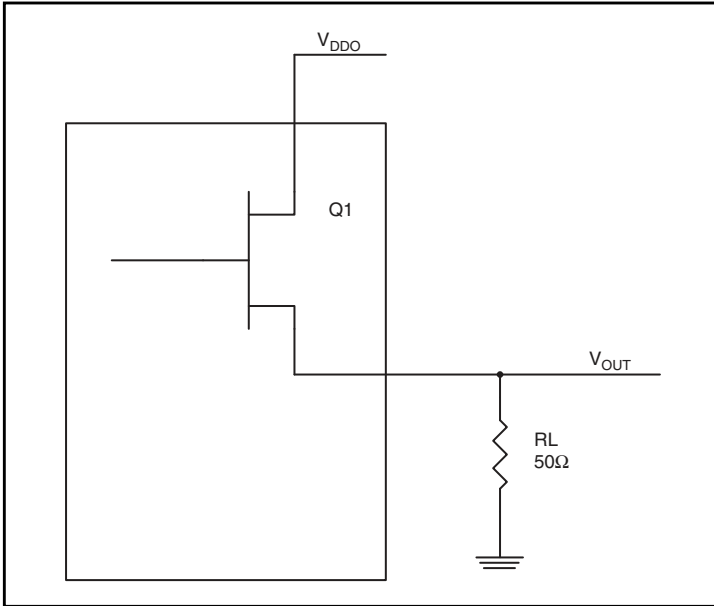


Figure 6. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH_MAX} / R_L) * (V_{DDO_MAX} - V_{OH_MAX})$$

$$Pd_L = (V_{OL_MAX} / R_L) * (V_{DDO_MAX} - V_{OL_MAX})$$

$$Pd_H = (0.9V / 50\Omega) * (2V - 0.9V) = \mathbf{19.8mW}$$

$$Pd_L = (0.4V / 50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{32.6mW}$$

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

| Linear Feet per Minute | θ_{JA} by Velocity | | |
|--|---------------------------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

Transistor Count

The transistor count for 8523 is: 472

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

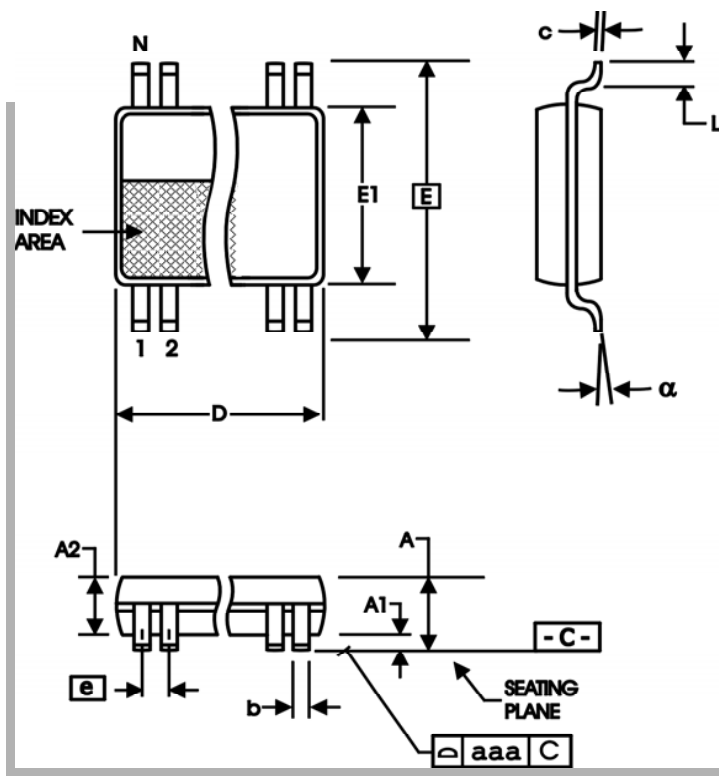


Table 8. Package Dimensions

| All Dimensions in Millimeters | | |
|-------------------------------|------------|---------|
| Symbol | Minimum | Maximum |
| N | 20 | |
| A | | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 Basic | |
| E1 | 4.30 | 4.50 |
| e | 0.65 Basic | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|-------------|---------------------------|--------------------|-------------|
| 8523CGLF | ICS8523CGLF | "Lead-Free" 20 Lead TSSOP | Tube | 0°C to 70°C |
| 8523CGLFT | ICS8523CGLF | "Lead-Free" 20 Lead TSSOP | 2500 Tape & Reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|---|---------|---|----------|
| B | T4D | 5 | HSTL table - added V_{SWING} row to HSTL DC Characteristics Table. | 7/31/01 |
| | T5 | 5 | AC Characteristics table - t_{PD} row, added value of 1.3ns to Min.; changed Max. from 2.0ns to 1.6ns. | |
| B | | 3 | Updated Figure 1, CLK_EN Timing Diagram. | 10/17/01 |
| B | | 3 | Updated Figure 1, CLK_EN Timing Diagram. | 11/2/01 |
| C | T5 | 5 | AC Characteristics table - t_{PD} row, changed Min. from 1.3ns to 1.0ns. $t_{sk(pp)}$ row, changed Max. from 150ps to 200ps. | 1/11/02 |
| C | | 1 | Revised Features section, Bullet 1,6 - took out 1.8V | 5/6/02 |
| C | | 8-10 | In the Application Information section, added Schematic Examples. | 10/25/02 |
| C | T2 | 2 | Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. | 6/20/03 |
| | T4D | 4 | Absolute Maximum Ratings - changed Output rating. | |
| | | 5 | HSTL DC Characteristics Table - changed V_{OH} 1V min. to 0.9V min. | |
| | | 11 - 12 | Power Considerations - changed Total Power Dissipation to reflect V_{OH} change. Calculations changed due to new Total Power Dissipation. Changed LVHSTL to HSTL throughout data sheet. | |
| C | T9 | 1 | Features section - added Lead-Free bullet. | 9/13/04 |
| | | 9 | Updated LVPECL Clock Input Interface section. | |
| | | 15 | Added Lead-Free marking to Ordering Information table. | |
| C | T8 | 16 | Ordering Information Table - in the <i>Part/Order Number</i> and <i>Marking</i> columns, changed die revision from "B" to "C". | 3/2/07 |
| D | T5 | 6 | AC Characteristics Table - changed t_{R}/t_{F} minimum from 300ps to 250ps. | 3/13/07 |
| E | T4C T4D T5 | 1 | Features Section - added Additive Phase Jitter bullets. Pin Assignment has nCLK, nPCLK. Changed \overline{CLK} , \overline{PCLK} to nCLK, nPCLK throughout the datasheet. | 1/24/11 |
| | | 4 | Absolute Maximum Ratings - corrected Outputs Rating. | |
| | | 4 | Differential DC Characteristics Table - updated notes. | |
| | | 5 | LVPECL DC Characteristics Table - updated notes. | |
| | | 5 | AC Characteristics Table - added Buffer Additive Phase Jitter specs. Add thermal note and updated NOTE 4. | |
| | | 6 | Added Additive Phase Jitter plot. | |
| | | 8 | Corrected Output Duty Cycle/Pulse Width/Period diagram. | |
| | | 8 | Updated <i>Wiring the Differential Input to Accept Single-ended Levels</i> application note. | |
| | | 9 | Updated <i>3.3V Differential Clock Input Interface</i> application note. | |
| | | 10 | Updated <i>3.3V LVPECL Clock Input Interface</i> application note. | |
| 11 | Added <i>HSTL Output Termination</i> diagram. | | | |
| E | T9 | 16 | Ordering Information - removed leaded devices. | 6/15/15 |
| | | 1 | Features section - removed bullet referencing leaded devices. Updated data sheet format. | |



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com

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