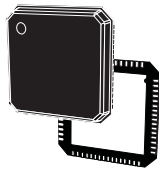



## AM/FM/HD-Radio™/DAB automotive digital output tuner



VFQFPN64 (9 x 9 x 1.0 mm)

### Features

- AEC-Q100 qualified 
- Full automotive grade RFCMOS design
- Quad-band:
  - AM/FM Band
  - Band-III
  - Band-L
- Two independent reception channels
- Integrated RF switch matrix in FM
- Software configurable digital base-band interface (I2S or JESD204B)
- Compatible with digital radio standards: DAB, DRM, and HD-Radio™
- Software programmable
- Very high dynamic range built-in  $\Sigma\Delta$  ADC
- Very low external component count (no pin diodes, transformers or varicap)
- RoHS compliant small footprint package

### Description

The **STA710** is a single chip, full CMOS, quad-band, dual channel front-end tuner specifically tailored to Software-Defined-Radio (SDR) systems.

When paired with an application processor, STA710 enables the implementation of a SDR solution to receive analog (AM/FM/WX) and digital terrestrial broadcasting standards (e.g. HD-Radio™/DAB/DRM).

The STA710 features front-end low-noise amplifiers (LNAs) covering AM band (LW/MW/SW), FM and WX bands, DAB band-III and band-L.

After on-chip IF filtering, the STA710 digitizes the signal with a high dynamic range  $\Sigma\Delta$  ADC ahead of the complex phase-quadrature base-band signal down conversion to provide a stable digital base-band output to the companion application processor.

The digital base-band signal is transmitted to the application processor via a flexible and configurable serial digital interface operating either as single-ended I2S, LVDS I2S or JESD204B.

The STA710 dual channel architecture enables a straightforward implementation of audio/data foreground-background reception strategies and multipath interference mitigation algorithms such as FM phase-diversity, DAB/DRM Maximal-Ratio-Combining (MRC) inside the companion application processor.

The STA710 offers automotive grade and state-of-art RF performances with minimum external component count.

#### Product status link

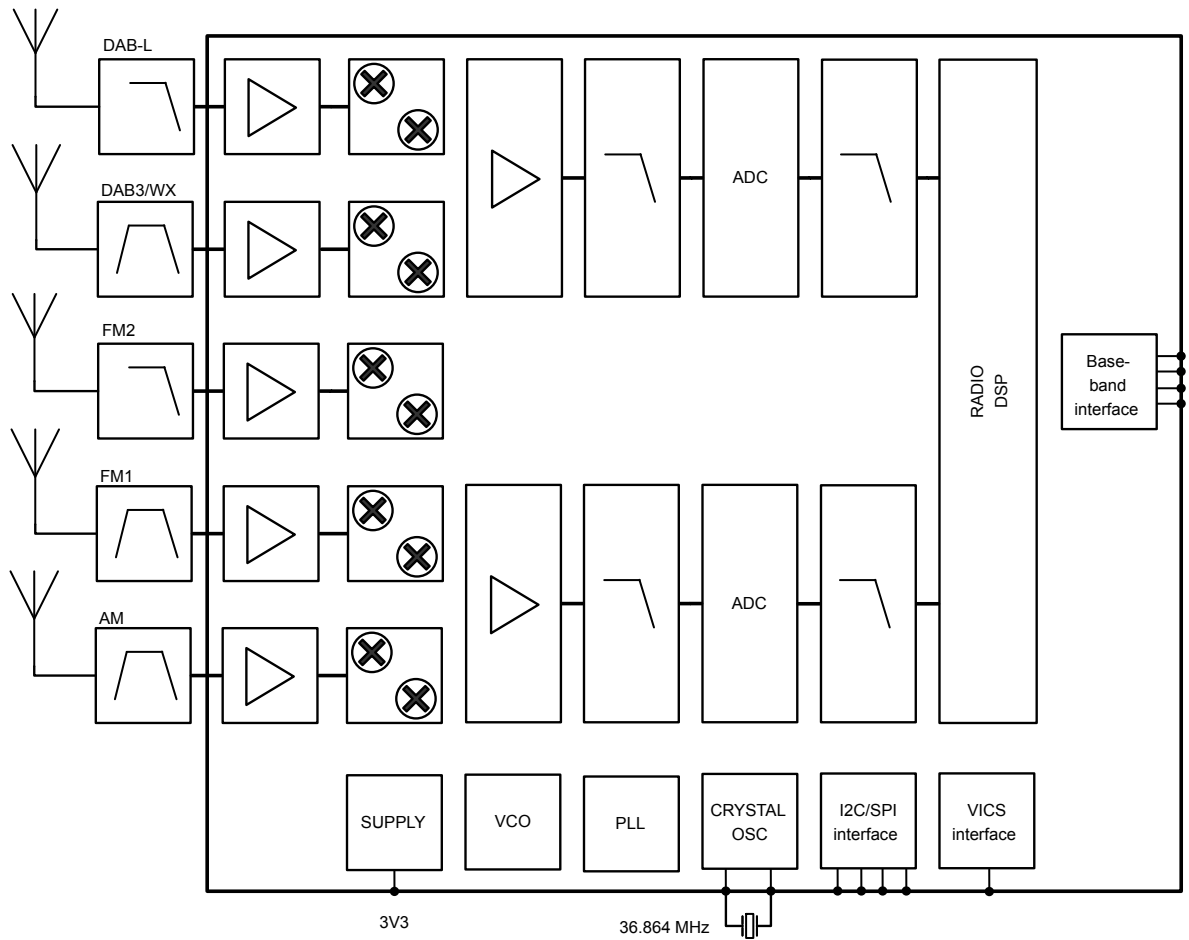
[STA710](#)

#### Product summary

| Order code | Package    | Packing     |
|------------|------------|-------------|
| STA710EC   | VFQFPN64   | Tray        |
| STA710ECTR | (9x9x1 mm) | Tape & Reel |

# 1 Block diagram

Figure 1. Block diagram



## 2 Electrical specification

### 2.1 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

| Symbol           | Parameter                                               | Test condition                    | Min                     | Typ | Max | Units |
|------------------|---------------------------------------------------------|-----------------------------------|-------------------------|-----|-----|-------|
| V <sub>CC</sub>  | Abs. supply voltage                                     | -                                 | -0.5                    | -   | 3.6 | V     |
| T <sub>stg</sub> | Storage temperature                                     | -                                 | -55                     | -   | 150 | °C    |
| V <sub>ESD</sub> | ESD absolute minimum withstand voltage                  | Human Body model                  | > ±2000  <sup>(1)</sup> |     |     | V     |
|                  |                                                         | Charged device model              | > ±500  <sup>(2)</sup>  |     |     |       |
|                  |                                                         | Charged device model, corner pins | > ±750                  |     |     |       |
| -                | Max. input current at any pin (latch-up characteristic) | I <sub>INMAX</sub>                | ±100                    |     |     | mA    |

1. |±1000| on AM\_IN pin

2. |±400| on AM\_IN pin

### 2.2 Thermal data

**Table 2. Thermal data**

| Symbol                | Parameter                              | Test Condition                            | Value | Units  |
|-----------------------|----------------------------------------|-------------------------------------------|-------|--------|
| R <sub>th j-amb</sub> | Thermal Resistance junction-to-ambient | Multilayer 2s2p as per JEDEC JESD51-7     | 27    | °C / W |
|                       |                                        | Thermally optimized multilayer 2s2p board | 22    |        |

### 2.3 General key parameters

**Table 3. General key parameters**

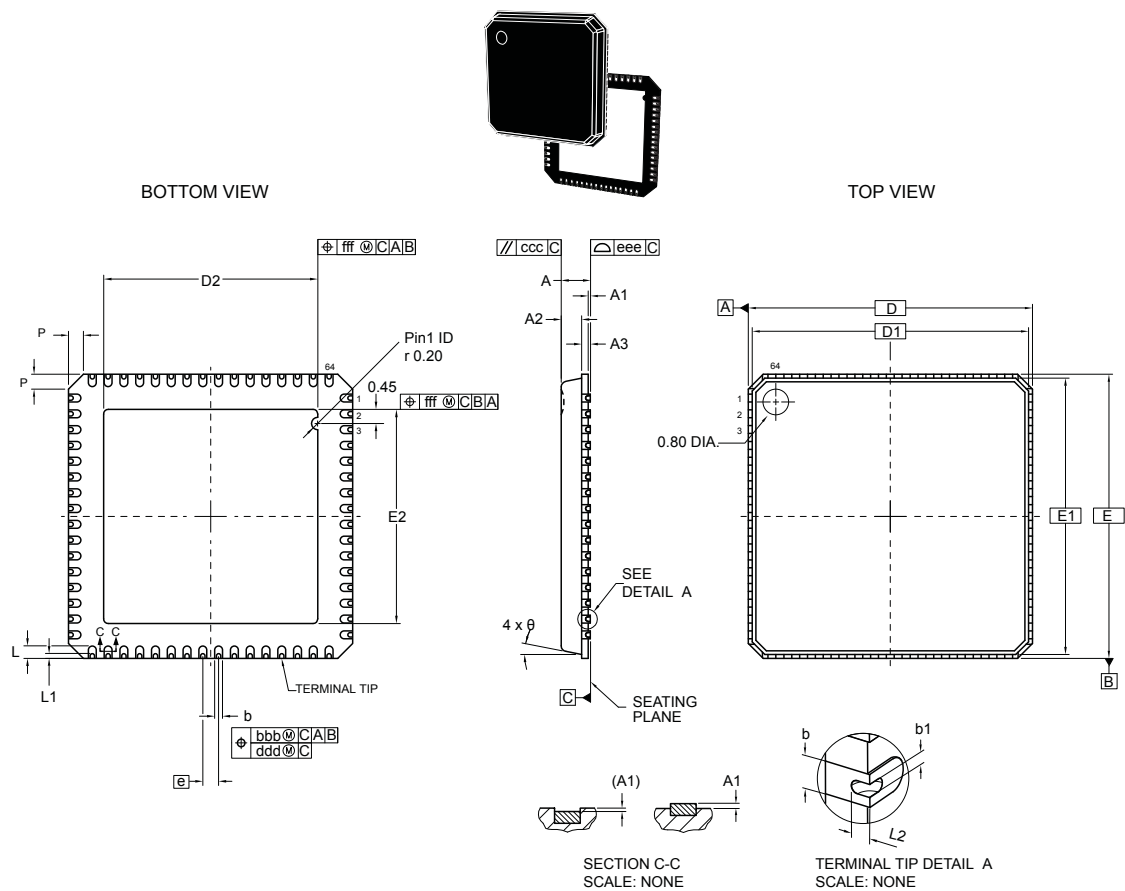
| Symbol              | Parameter                 | Test Condition                                                                              | Min  | Typ | Max  | Units |
|---------------------|---------------------------|---------------------------------------------------------------------------------------------|------|-----|------|-------|
| V <sub>CC</sub>     | 3.3 V supply voltage      |                                                                                             | 3.15 | 3.3 | 3.45 | V     |
| I <sub>CC</sub>     | Supply current            | Two active RF channels, I2S baseband interface activated, V <sub>CC</sub> = 3.45 V          | -    | -   | 483  | mA    |
|                     |                           | Two active RF channels, JESD204b interface activated (10 pF load), V <sub>CC</sub> = 3.45 V | -    | -   | 504  |       |
| T <sub>amb</sub>    | Ambient Temperature Range | -                                                                                           | -40  | -   | 85   | °C    |
| T <sub>j_oper</sub> | Operative Junction Temp   | -                                                                                           | -    | -   | 125  | °C    |
| P <sub>diss</sub>   | Dissipated power          | Two active RF channels, R <sub>ext</sub> = 12 Ohm, I2S baseband interface activated         | -    | -   | 1.4  | W     |
|                     |                           | Two active RF channels, R <sub>ext</sub> = 12 Ohm, JESD204b interface activated             | -    | -   | 1.5  |       |

### 3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

#### 3.1 VFQFPN-64 (9x9x1.0mm) package information

Figure 2. VFQFPN-64 (9x9x1.0 mm) package outline



8511068\_B\_A02G

GAPGPS03460

Table 4. VFQFPN-64 (9x9x1.0 mm) package mechanical data

| Ref.             | Dimensions in mm |      |      |
|------------------|------------------|------|------|
|                  | Min.             | Typ. | Max. |
| $\Theta$         | -                | -    | 14   |
| A                | -                | -    | 1.0  |
| A1               | 0.00             | -    | 0.05 |
| A2               | 0.55             | -    | 0.80 |
| A3               | 0.20 REF         |      |      |
| b <sup>(1)</sup> | 0.18             | 0.25 | 0.30 |

| Ref.                                  | Dimensions in mm |      |      |
|---------------------------------------|------------------|------|------|
|                                       | Min.             | Typ. | Max. |
| b1                                    | -                | 0.15 | -    |
| D                                     | 9.00 BSC         |      |      |
| D1 <sup>(2)</sup>                     | 8.75 BSC         |      |      |
| D2                                    | -                | 6.70 | -    |
| e                                     | 0.50 BSC         |      |      |
| E                                     | 9.00 BSC         |      |      |
| E1 <sup>(2)</sup>                     | 8.75 BSC         |      |      |
| E2                                    | -                | 6.70 | -    |
| L                                     | 0.30             | -    | 0.50 |
| L1                                    | 0.15 REF         |      |      |
| L2                                    | -                | 0.10 | -    |
| P                                     | -                | -    | 0.60 |
| <b>Tolerance of form and position</b> |                  |      |      |
| aaa                                   | 0.15             |      |      |
| bbb                                   | 0.10             |      |      |
| ccc                                   | 0.10             |      |      |
| ddd                                   | 0.05             |      |      |
| eee                                   | 0.08             |      |      |
| fff                                   | 0.10             |      |      |

1. Maximum allowable burr is 0.076 mm in all directions.

2. D1 and E1 are Maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm (0.0098 inch)" per side.

**Note:** The package is compliant to IPC/JEDEC J-STD-020D June 2007 standard Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices, MSL Level 3.

## Revision history

**Table 5. Document revision history**

| Date        | Version | Changes                                          |
|-------------|---------|--------------------------------------------------|
| 26-Feb-2019 | 1       | Initial release.                                 |
| 25-Nov-2019 | 2       | Updated <a href="#">Figure 1. Block diagram.</a> |

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