



## Features

- ESD Protect for 5 Lines with Uni-directional
- Provide ESD protection for the protected line to **IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 12\text{kV}$  (contact)**  
**IEC 61000-4-4 (EFT) 30A (5/50ns)**  
**Cable Discharge Event (CDE)**
- Small package saves board space
- Protect five I/O lines or five power lines
- Fast turn-on and Low clamping voltage
- Low operating voltage: 5.0V and below
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

## Applications

- Audio Interfaces Protection
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

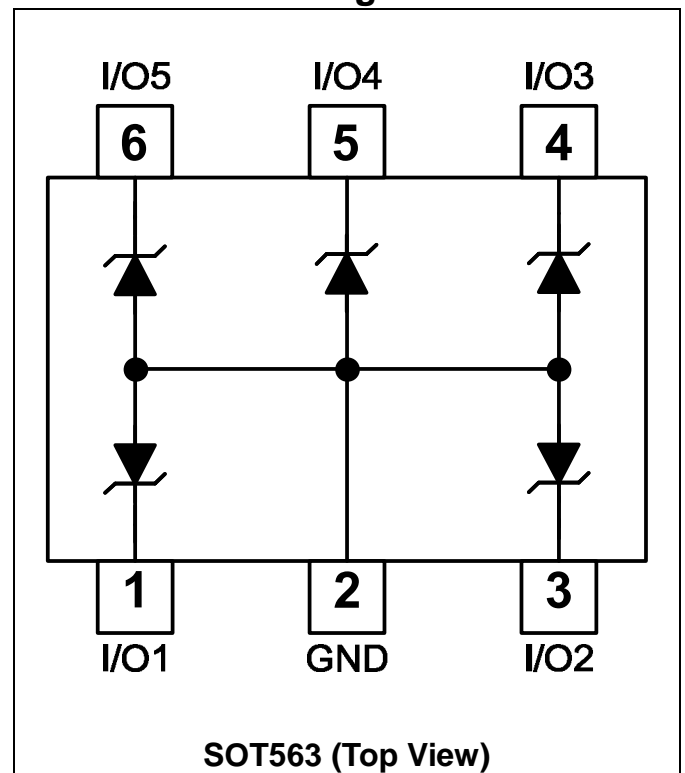
## Description

AZ2015-05R is a design which includes five uni-directional ESD rated clamping cells to protect five power lines, or five control lines, or five low speed data lines in an electronic systems. The AZ2013-05R has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

AZ2015-05R is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control/data lines, protecting any downstream components.

AZ2015-05R may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## SPECIFICATIONS

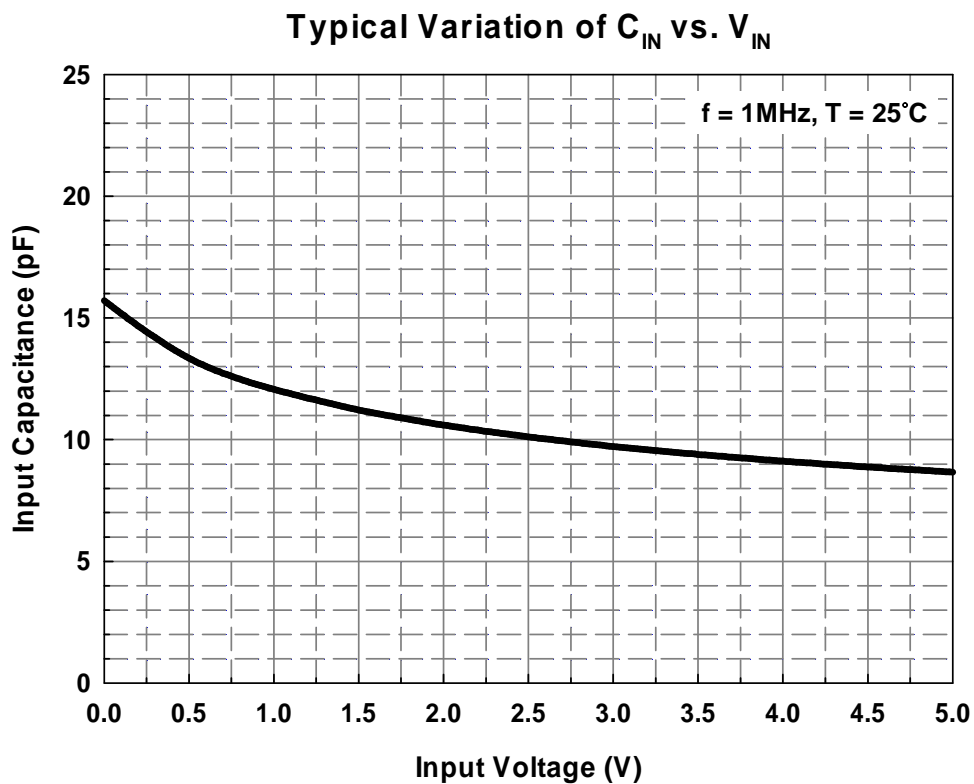
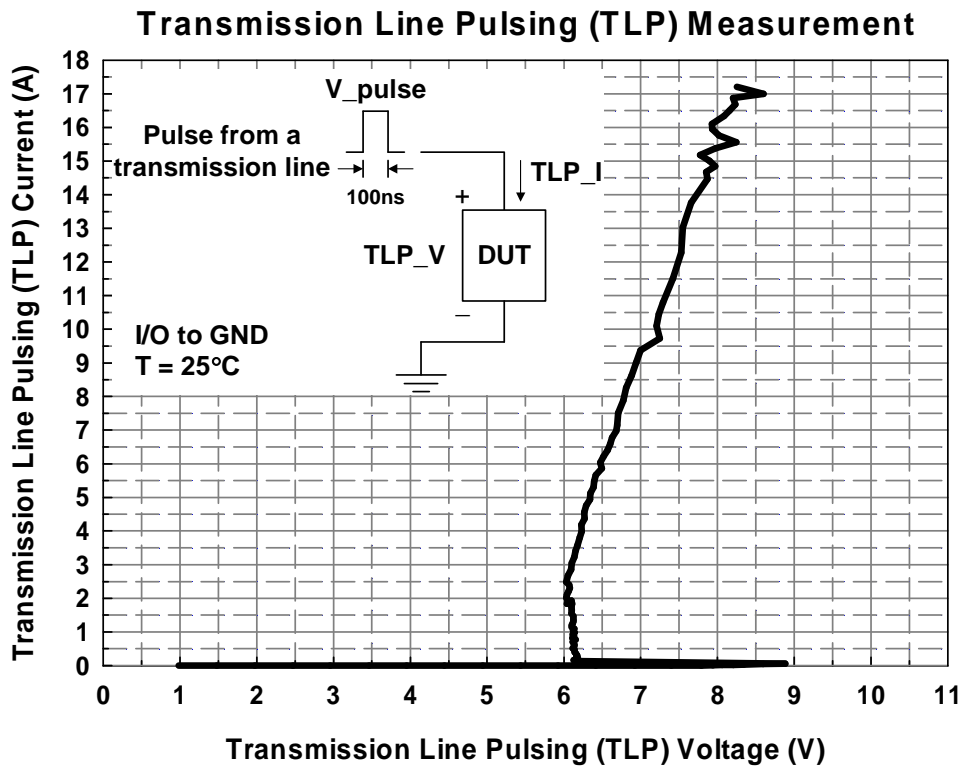
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Operating Supply Voltage	$V_{DC}$	5.5	V
ESD per IEC 61000-4-2 (Air)	$V_{ESD}$	±15	kV
ESD per IEC 61000-4-2 (Contact)		±12	kV
Lead Soldering Temperature	$T_{SOL}$	260 (10 sec.)	°C
Operating Temperature	$T_{OP}$	-55 to +85	°C
Storage Temperature	$T_{STO}$	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	$V_{RWM}$	Pin-1, -3, -4, -5, -6 to Pin-2, $T = 25\text{ }^{\circ}\text{C}$ .			5.0	V
Reverse Leakage Current	$I_{Leak}$	$V_{RWM} = 5.0\text{V}$ , $T = 25\text{ }^{\circ}\text{C}$ , Pin-1, -3, -4, -5, -6 to Pin-2.			1	$\mu\text{A}$
Reverse DC Breakdown Voltage	$V_{BV}$	$I_{BV} = 1\text{mA}$ , $T = 25\text{ }^{\circ}\text{C}$ , Pin-1, -3, -4, -5, -6 to Pin-2.	6.5		9.0	V
Forward Voltage	$V_F$	$I_F = 15\text{mA}$ , $T=25\text{ }^{\circ}\text{C}$ , Pin-2 to Pin-1, -3, -4, -5, -6.	0.6		1.0	V
ESD Clamping Voltage (Note 1)	$V_{clamp}$	IEC 61000-4-2 +8kV ( $I_{TLP} = 16\text{A}$ ), Contact mode, $T=25\text{ }^{\circ}\text{C}$ , I/O pin to Ground.		8.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, $T=25\text{ }^{\circ}\text{C}$ , Contact mode, any I/O pin to Ground.		0.15		$\Omega$
Channel Input Capacitance	$C_{IN}$	$V_R = 0\text{V}$ , $f = 1\text{MHz}$ , $T=25\text{ }^{\circ}\text{C}$ . Pin-1, -3, -4, -5, -6 to Pin-2.		16	19	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions:  $Z_0 = 50\Omega$ ,  $t_p = 100\text{ns}$ ,  $t_r = 1\text{ns}$ .

## Typical Characteristics



## Applications Information

The AZ2015-05R is designed to protect five lines against System ESD/EFT/CDE pulses by clamping them to an acceptable reference.

The usage of the AZ2015-05R is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1, 3, 4, 5 and 6. The pin2 should be connected directly to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ2015-05R should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical.

Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ2015-05R.
- Place the AZ2015-05R near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to PCB internal circuit.

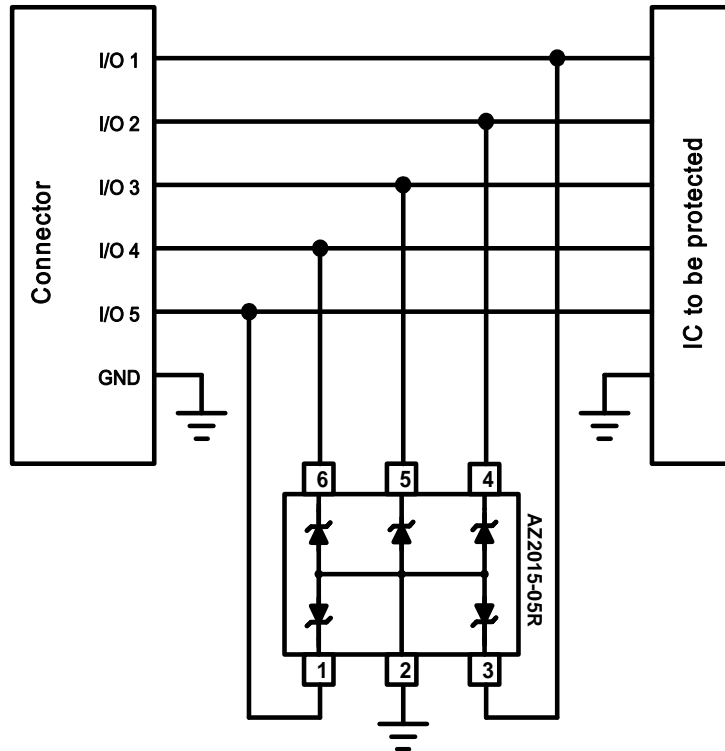


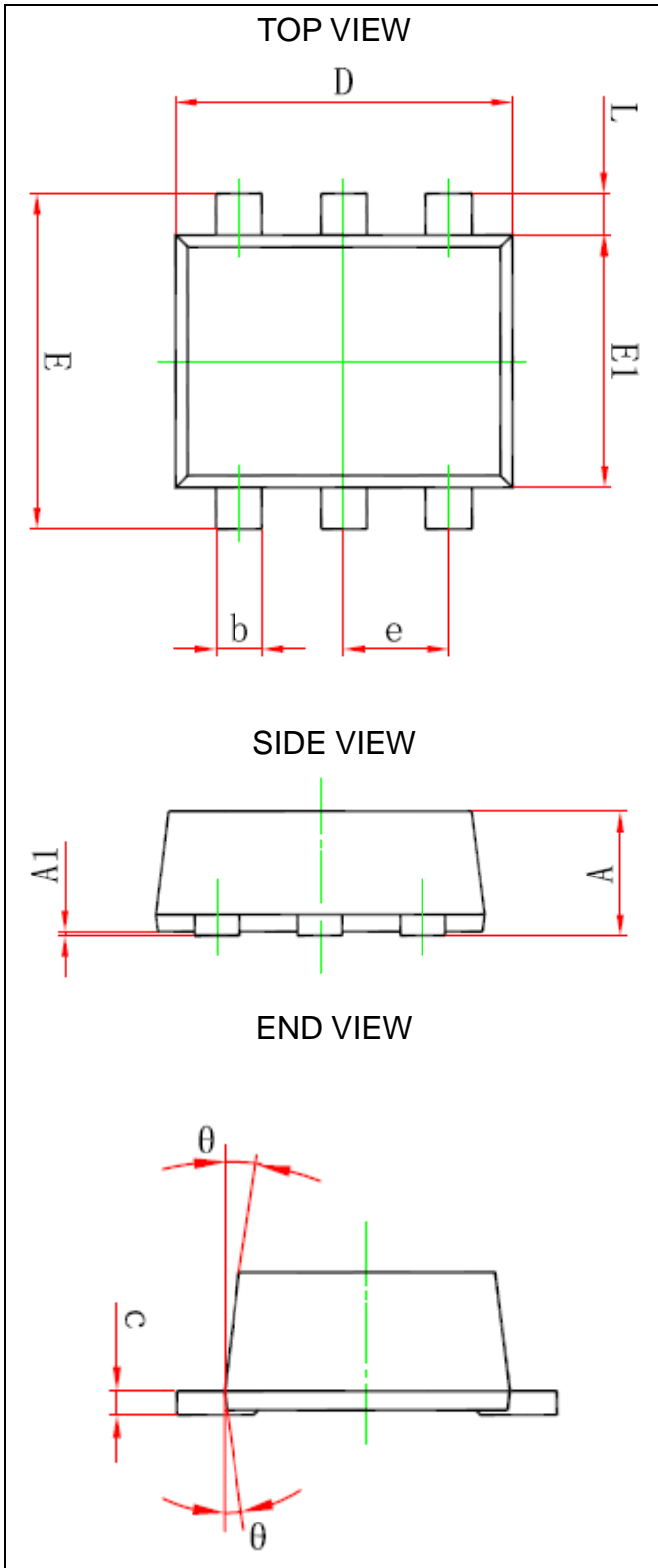
Fig. 1



## Mechanical Details

### SOT563

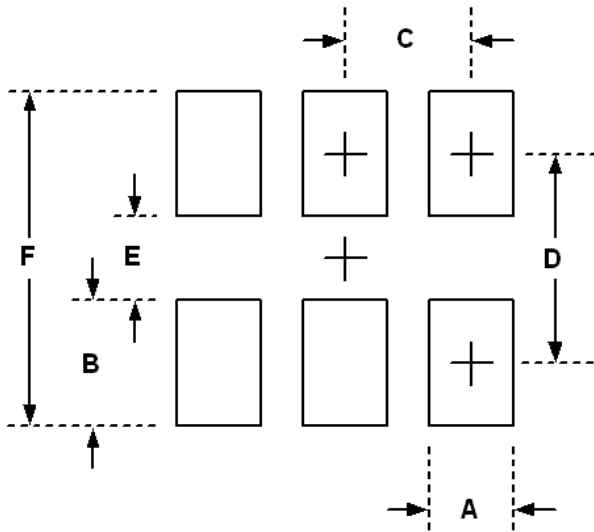
#### PACKAGE DIAGRAMS



#### PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN.	MAX.
A	0.525	0.60
A1	0	0.05
e	0.45	0.55
c	0.09	0.16
D	1.50	1.70
b	0.17	0.27
E1	1.10	1.30
E	1.50	1.70
L	0.10	0.30
$\theta$	7° REF	

## LAND LAYOUT

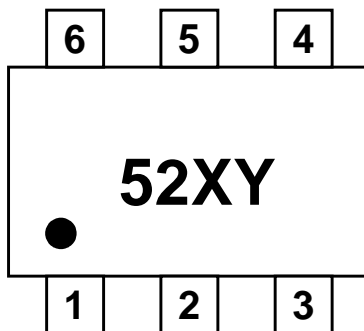


Dimensions	
Index	Millimeter
A	0.30
B	0.50
C	0.50
D	1.40
E	0.90
F	1.90

### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



Part Number	Marking Code
AZ2015-05R (Green Part)	52XY

Note. Green means Pb-free, RoHS, and Halogen free compliant.

52=Device Code

X=Date Code

Y=Control Code

## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ2015-05R.R7G	Green	T/R	7 inch	3,000/reel	4 reel = 12,000/box	6 box = 72,000/carton



## Revision History

Revision	Modification Description
Revision 2013/04/25	Preliminary release.
Revision 2016/06/30	1. Add the ESD Dynamic Turn-on Resistance. 2. Add the ordering information.
Revision 2016/08/22	Formal release.