



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

128-Kbit (16K × 8) Serial (I²C) F-RAM

Features

- 128-Kbit ferroelectric random access memory (F-RAM) logically organized as 16K × 8
 - High-endurance 100 trillion (10¹⁴) read/writes
 - 151-year data retention (See [Data Retention and Endurance on page 13](#))
 - NoDelay™ writes
 - Advanced high-reliability ferroelectric process
- Fast two-wire serial interface (I²C)
 - Up to 3.4-MHz frequency^[1]
 - Direct hardware replacement for serial EEPROM
 - Supports legacy timings for 100 kHz and 400 kHz
- Device ID
 - Manufacturer ID and Product ID
- Low power consumption
 - 175-μA active current at 100 kHz
 - 150-μA standby current
 - 8-μA sleep mode current
- Low-voltage operation: V_{DD} = 2.0 V to 3.6 V
- Industrial temperature: -40 °C to +85 °C
- 8-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The FM24V01A is a 128-Kbit nonvolatile memory employing an advanced ferroelectric process. An F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by EEPROM and other nonvolatile memories.

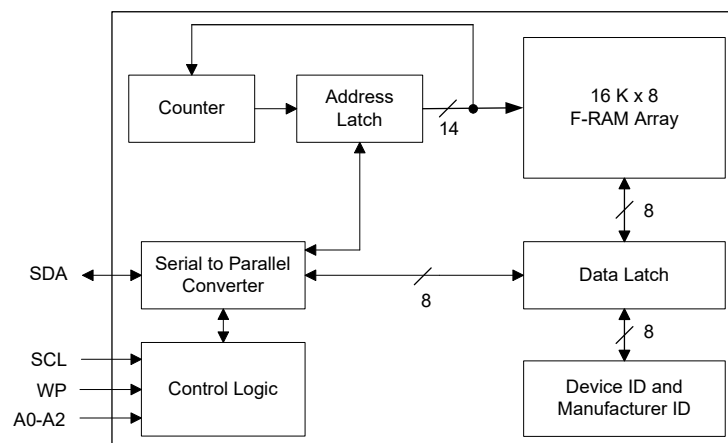
Unlike EEPROM, the FM24V01A performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. F-RAM also exhibits much lower power during writes than EEPROM because write operations do not require an internally elevated power supply voltage for write circuits. The FM24V01A is capable of supporting 10¹⁴ read/write cycles, or 100 million times more write cycles than EEPROM.

These capabilities make the FM24V01A ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data logging, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows more frequent data writing with less overhead for the system.

The FM24V01A provides substantial benefits to users of serial EEPROM as a hardware drop-in replacement. The device incorporates a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision. The device specifications are guaranteed over an industrial temperature range of -40 °C to +85 °C.

For a complete list of related resources, [click here](#).

Logic Block Diagram



Note

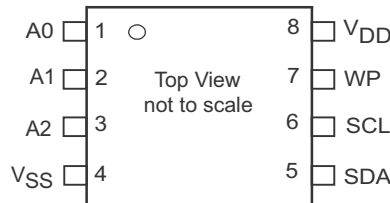
1. The FM24V01A does not meet the NXP I²C specification in the Fast-mode Plus (Fm+, 1 MHz) for I_{OL} and in the High Speed Mode (Hs-mode, 3.4 MHz) for V_{hys}. Refer to [DC Electrical Characteristics on page 12](#) for more details.

Contents

Pinout	3	Data Retention and Endurance	13
Pin Definitions	3	Capacitance	13
Functional Overview	4	Thermal Resistance	13
Memory Architecture	4	AC Test Loads and Waveforms	13
Two-wire Interface	4	AC Test Conditions	13
STOP Condition (P)	5	AC Switching Characteristics	14
START Condition (S)	5	Power Cycle Timing	15
Data/Address Transfer	5	Ordering Information	16
Acknowledge/No-acknowledge	6	Ordering Code Definitions	16
High Speed Mode (Hs-mode)	6	Package Diagram	17
Slave Device Address	7	Acronyms	18
Addressing Overview	7	Document Conventions	18
Data Transfer	7	Units of Measure	18
Memory Operation	8	Document History Page	19
Write Operation	8	Sales, Solutions, and Legal Information	21
Read Operation	9	Worldwide Sales and Design Support	21
Sleep Mode	10	Products	21
Device ID	11	PSoC® Solutions	21
Maximum Ratings	12	Cypress Developer Community	21
Operating Range	12	Technical Support	21
DC Electrical Characteristics	12		

Pinout

Figure 1. 8-pin SOIC Pinout



Pin Definitions

Pin Name	I/O Type	Description
A0–A2	Input	Device Select Address 0–2. These pins are used to select one of up to eight devices of the same type on the same two-wire bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	Input/Output	Serial Data Address. This is a bidirectional pin for the two-wire interface. It is open-drain and is intended to be wire-AND'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	Serial Clock. The serial clock pin for the two-wire interface. Data is clocked out of the part on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
WP	Input	Write Protect. When tied to V_{DD} , addresses in the entire memory map will be write-protected. When WP is connected to ground, all addresses are write enabled. This pin is pulled down internally.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Functional Overview

The FM24V01A is a serial F-RAM memory. The memory array is logically organized as 16,384 × 8 bits and is accessed using a two-wire (I²C) interface. The functional operation of the F-RAM is similar to serial EEPROM. The major difference between the FM24V01A and a serial EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

Memory Architecture

When accessing the FM24V01A, the user addresses 16K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the two-wire protocol, which includes a slave address (to distinguish other non-memory devices) and a two-byte address. The upper 2 bits of the address range are 'don't care' values. The complete address of 14 bits specifies each byte address uniquely.

The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the two-wire bus. Unlike a serial EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write

operation is complete. This is explained in more detail in the [Memory Operation on page 8](#).

Two-wire Interface

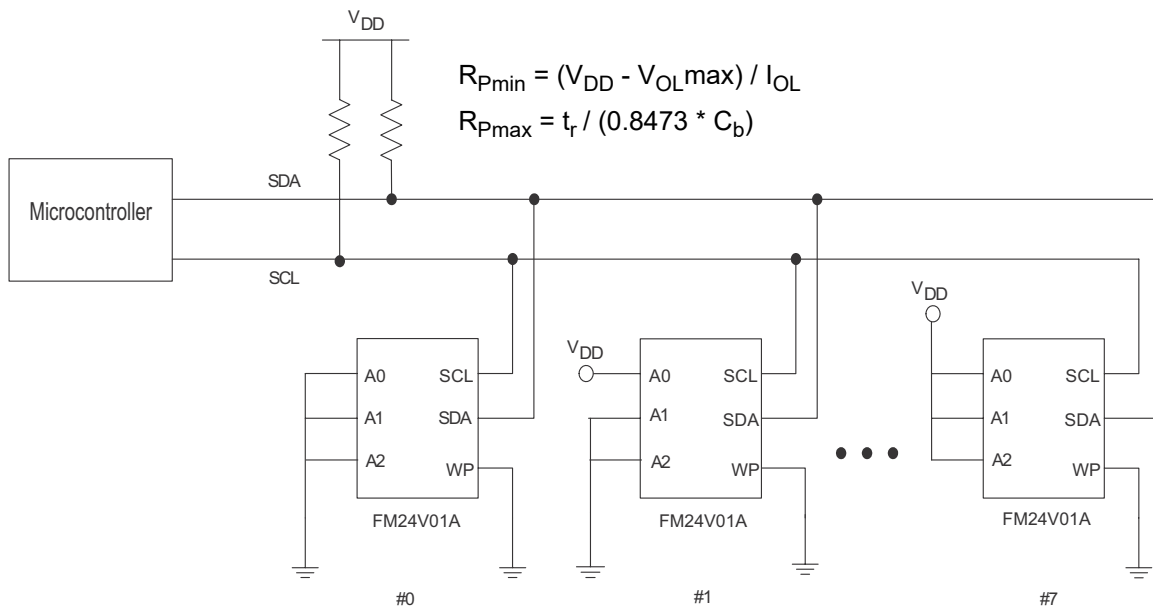
The FM24V01A employs a bidirectional two-wire bus protocol using few pins or board space. [Figure 2](#) illustrates a typical system configuration using the FM24V01A in a microcontroller-based system. The two-wire bus is familiar to many users but is described in this section.

By convention, any device that is sending data to the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM24V01A is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. [Figure 3 on page 5](#) and [Figure 4 on page 5](#) illustrate the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

The FM24V01A does not meet the NXP I²C specification in the Fast-mode Plus (Fm+, 1 MHz) for I_{OL} and in the High Speed Mode (Hs-mode, 3.4 MHz) for V_{hys}. Refer to [DC Electrical Characteristics on page 12](#) for more details.

Figure 2. System Configuration Using Serial (I²C) F-RAM



STOP Condition (P)

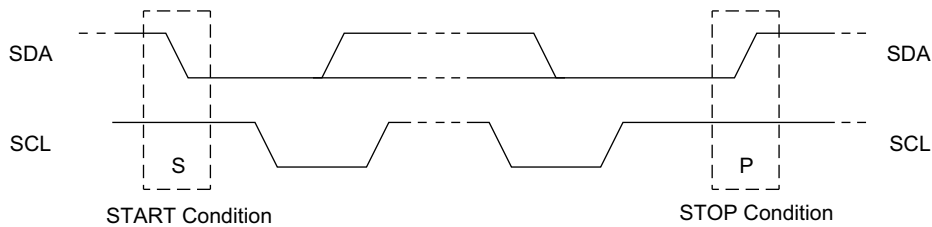
A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations using the FM24V01A should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of the SDA (not a memory read) to assert a STOP condition.

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the FM24V01A for a new operation.

If during operation the power supply drops below the specified V_{DD} minimum, the system should issue a START condition prior to performing another operation.

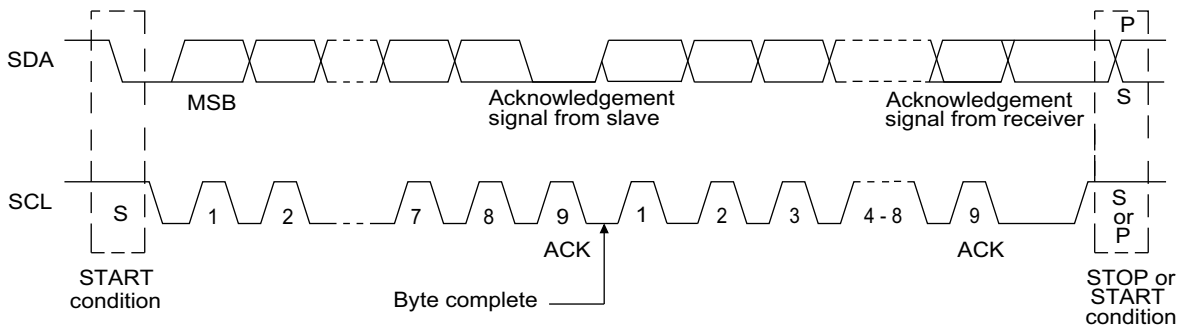
Figure 3. START and STOP Conditions



Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

Figure 4. Data Transfer on the I²C Bus



Acknowledge/No-acknowledge

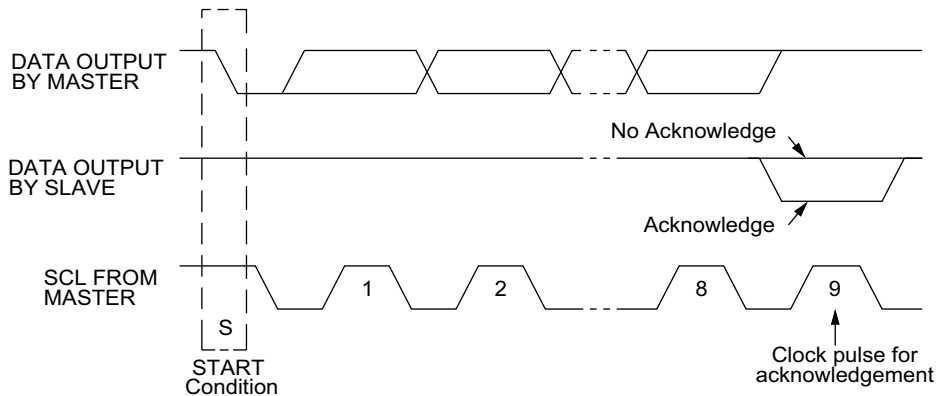
The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state, the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver will fail to acknowledge for two distinct reasons, the first being that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the part

can be addressed again. This allows the last byte to be recovered in the event of a communication error.

The second and most common reason is that, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM24V01A will continue to place data on the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this causes the FM24V01A to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

Figure 5. Acknowledge on the I²C Bus

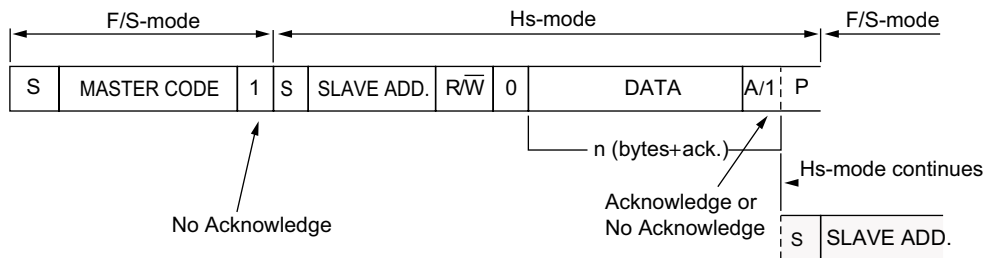


High Speed Mode (Hs-mode)

The FM24V01A supports a 3.4-MHz high-speed mode. A master code (00001XXXb) must be issued to place the device into the

high-speed mode. Communication between master and slave will then be enabled for speeds up to 3.4 MHz. A STOP condition will exit Hs-mode. Single- and multiple-byte reads and writes are supported.

Figure 6. Data Transfer Format in Hs-Mode

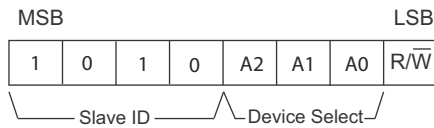


Slave Device Address

The first byte that the FM24V01A expects after a START condition is the slave address. As shown in Figure 7, the slave address contains the device type or slave ID, the device select address bits, and a bit that specifies if the transaction is a read or a write.

Bits 7–4 are the device type (slave ID) and should be set to 1010b for the FM24V01A. These bits allow other function types to reside on the two-wire bus within an identical address range. Bits 3–1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to eight FM24V01A devices can reside on the same two-wire bus by assigning a different address to each. Bit 0 is the read/write bit (R/W). R/W = '1' indicates a read operation and R/W = '0' indicates a write operation.

Figure 7. Memory Slave Device Address



Addressing Overview

After the FM24V01A (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The

complete 14-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as power remains or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24V01A increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (3FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Data Transfer

After the address bytes have been transmitted, data transfer between the bus master and the FM24V01A can begin. For a read operation the FM24V01A will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM24V01A will transfer the next sequential byte. If the acknowledge is not sent, the FM24V01A will end the read operation. For a write operation, the FM24V01A will accept 8 data bits from the master then sends an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24V01A is designed to operate in a manner very similar to other two-wire interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM24V01A and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained in the following sections.

Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/W bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 3FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle

occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The FM24V01A uses no page buffering.

The memory array can be write-protected using the WP pin. Setting the WP pin to a HIGH condition (V_{DD}) will write-protect all addresses. The FM24V01A will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a LOW state (V_{SS}) will disable the write protect. WP is pulled down internally.

Figure 8 and Figure 9 illustrate a single-byte and multiple-byte write cycles in Fast-mode Plus (Fm+). Figure 10 illustrates a single-byte write cycles in Hs mode.

Figure 8. Single-Byte Write

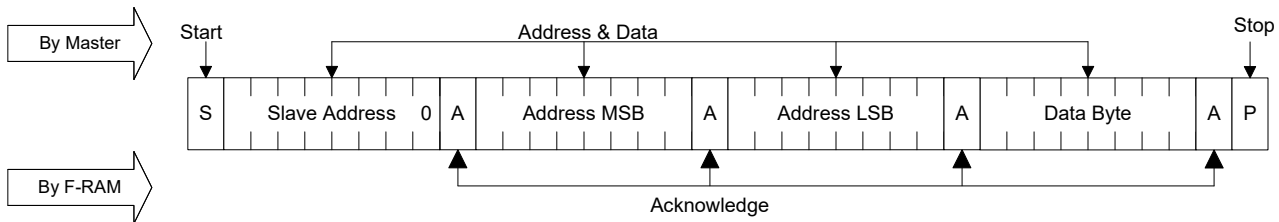


Figure 9. Multi-Byte Write

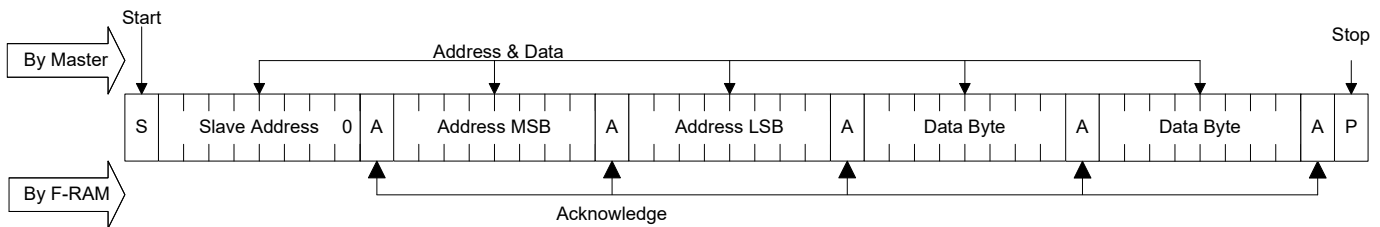
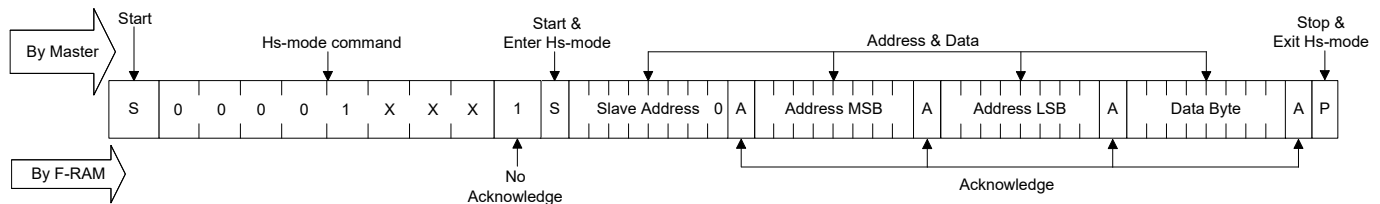


Figure 10. Hs-Mode Byte Write



Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM24V01A uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned in the previous paragraph, the FM24V01A uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM24V01A will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Note Each time the bus master acknowledges a byte, this indicates that the FM24V01A should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24V01A attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the following diagrams. This method is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

Figure 11. Current Address Read

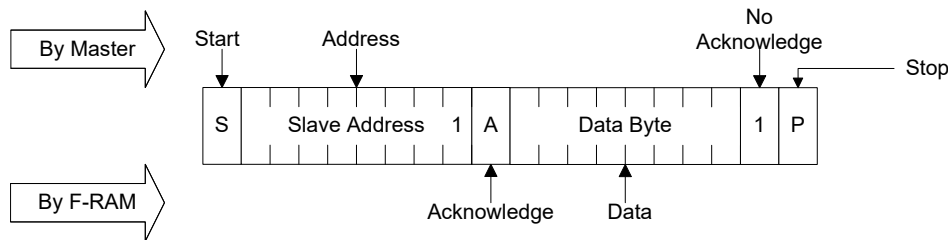


Figure 12. Sequential Read

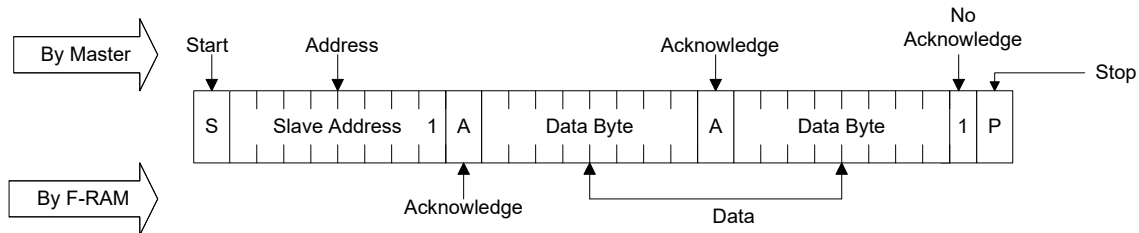
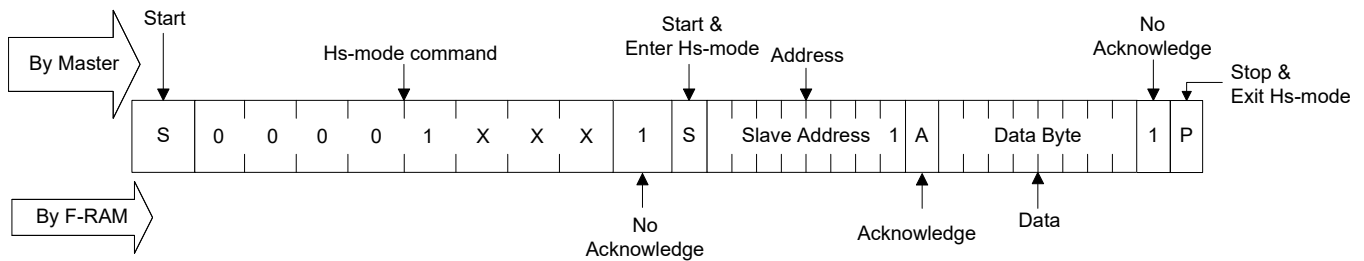


Figure 13. Hs-Mode Current Address Read

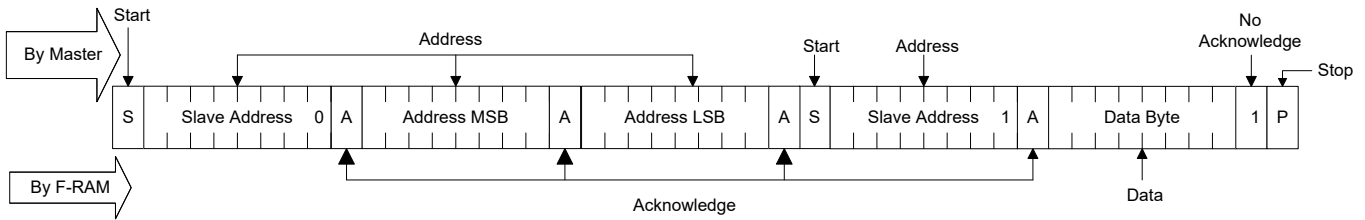


Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB (R/W) set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM24V01A acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

Figure 14. Selective (Random) Read



Sleep Mode

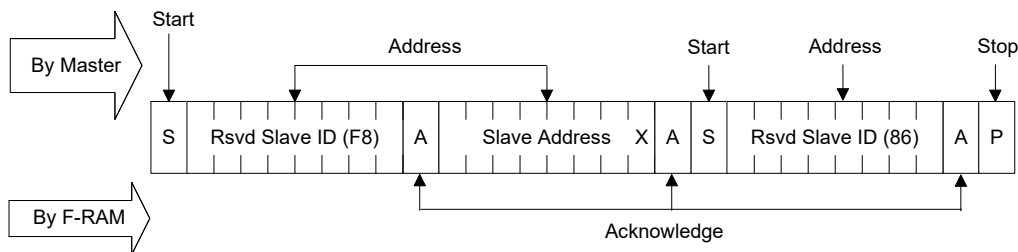
A low-power mode called Sleep Mode is implemented on the FM24V01A device. The device will enter this low power state when the Sleep command 86h is clocked-in. Sleep Mode entry can be entered as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID 0xF8.
3. The FM24V01A sends an ACK.
4. The master sends the I²C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (R/W bit). Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
5. The FM24V01A sends an ACK.

6. The master sends a Re-START command.
7. The master sends Reserved Slave ID 0x86.
8. The FM24V01A sends an ACK.
9. The master sends STOP to ensure the device enters sleep mode.

Once in sleep mode, the device draws I_{ZZ} current, but the device continues to monitor the I²C pins. Once the master sends a Slave Address that the FM24V01A identifies, it will "wake-up" and be ready for normal operation within t_{REC} (400 μs max.). As an alternative method of determining when the device is ready, the master can send read or write commands and look for an ACK. While the device is waking up, it will NACK the master until it is ready.

Figure 15. Sleep Mode Entry



Device ID

The FM24V01A device incorporates a means of identifying the device by providing three bytes of data, which are manufacturer, product ID, and die revision. The Device ID is read-only. It can be accessed as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID 0xF8.
3. The FM24V01A sends an ACK.
4. The master sends the I²C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (R/W bit). Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
5. The FM24V01A sends an ACK.
6. The master sends a Re-START command.
7. The master sends Reserved Slave ID 0xF9.
8. The FM24V01A sends an ACK.
9. The Device ID Read can be done, starting with the 12 manufacturer bits, followed by the 9 part identification bits, and then the 3 die revision bits.
10. The master ends the Device ID read sequence by NACKING the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

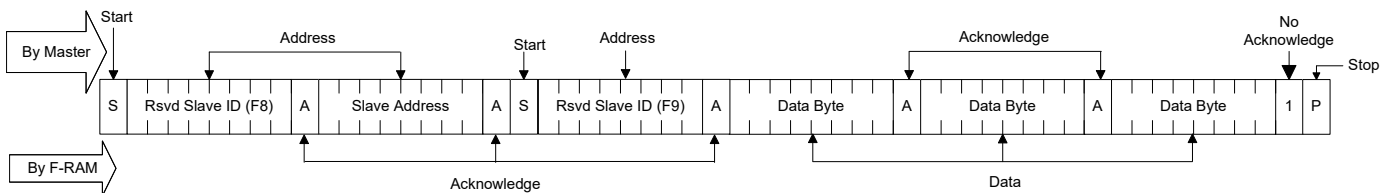
Note The reading of the Device ID can be stopped anytime by sending a NACK command.

Table 1. Device ID

Device ID (3 bytes)	Device ID Description			
	23–12 (12 bits)	11–8 (4 bits)	7–3 (5 bits)	2–0 (3 bits)
	Manufacturer ID	Product ID		
		Density	Variation	Die Rev
004101h	00000000100	0001	00000	001

Note Product ID bits 0 and 4 are reserved.

Figure 16. Read Device ID



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +125 °C
Maximum accumulated storage time	
At 125 °C ambient temperature 1000 h
At 85 °C ambient temperature 10 Years
Ambient temperature	
with power applied -55 °C to +125 °C
Supply voltage on V _{DD} relative to V _{SS} -1.0 V to +4.5 V
Input voltage* -1.0 V to +4.5 V and V _{IN} < V _{DD} + 1.0 V
DC voltage applied to outputs	
in HI-Z state -0.5 V to V _{DD} + 0.5 V
Transient voltage (< 20 ns)	
on any pin to ground potential -2.0 V to V _{DD} + 2.0 V

Package power dissipation capability	
(T _A = 25 °C) 1.0 W
Surface mount lead soldering temperature	
(3 seconds) +260 °C
Electrostatic discharge voltage	
Human Body Model (JEDEC Std JESD22-A114-B) 2 kV
Charged Device Model (JEDEC Std JESD22-C101-A) 500 V
Latch-up current > 140 mA

* Exception: The "V_{IN} < V_{DD} + 1.0 V" restriction does not apply to the SCL and SDA inputs.

Operating Range

Range	Ambient Temperature (T _A)	V _{DD}
Industrial	-40 °C to +85 °C	2.0 V to 3.6 V

DC Electrical Characteristics

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ ^[2]	Max	Unit
V _{DD}	Power supply		2.0	3.3	3.6	V
I _{DD}	Average V _{DD} current	SCL toggling between V _{DD} - 0.2 V and V _{SS} , other inputs V _{SS} or V _{DD} - 0.2 V.				
		f _{SCL} = 100 kHz	-	-	175	μA
		f _{SCL} = 1 MHz	-	-	400	μA
		f _{SCL} = 3.4 MHz	-	-	1000	μA
I _{SB}	V _{DD} standby current	SCL = SDA = V _{DD} . All other inputs V _{SS} or V _{DD} . Stop command issued.	-	90	150	μA
I _{ZZ}	Sleep mode current	SCL = SDA = V _{DD} . All other inputs V _{SS} or V _{DD} . Stop command issued.	-	5	8	μA
I _{LI}	Input leakage current (Except WP and A2-A0)	V _{SS} ≤ V _{IN} ≤ V _{DD}	-1	-	+1	μA
	Input leakage current (for WP and A2-A0)	V _{SS} ≤ V _{IN} ≤ V _{DD}	-1	-	+100	μA
I _{LO}	Output leakage current	V _{SS} ≤ V _{OUT} ≤ V _{DD}	-1	-	+1	μA
V _{IH}	Input HIGH voltage (SDL, SDA)		0.7 × V _{DD}	-	V _{DD(max)} + 0.3	V
	Input HIGH voltage (WP, A2-A0)		0.7 × V _{DD}	-	V _{DD} + 0.3	V
V _{IL}	Input LOW voltage		-0.3	-	0.3 × V _{DD}	V
V _{OL} ^[3]	Output LOW voltage	I _{OL} = 3 mA	-	-	0.4	V
		I _{OL} = 6 mA	-	-	0.6	V
R _{in} ^[4]	Input resistance (WP, A2-A0)	For V _{IN} = V _{IL(Max)}	50	-	-	kΩ
		For V _{IN} = V _{IH(Min)}	1	-	-	MΩ
V _{hys} ^[5]	Hysteresis of Schmitt Trigger inputs					
		f _{SCL} = 100 kHz, 400 kHz, 1 MHz	0.05 × V _{DD}	-	-	V
		f _{SCL} = 3.4 MHz	0.06 × V _{DD}	-	-	V

Notes

- Typical values are at 25 °C, V_{DD} = V_{DD(typ)}. Not 100% tested.
- The FM24V01A does not meet the NXP I²C specification in the Fast-mode Plus (Fm+, 1 MHz) for I_{OL} of 20 mA at a V_{OL} of 0.4 V.
- The input pull-down circuit is strong (50 kΩ) when the input voltage is below V_{IL} and weak (1 MΩ) when the input voltage is above V_{IH}.
- The FM24V01A does not meet the NXP I²C specification in the High Speed Mode (Hs-mode, 3.4 MHz) for V_{hys} of 0.1 × V_{DD}.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T _{DR}	Data retention	T _A = 85 °C	10	–	Years
		T _A = 75 °C	38	–	
		T _A = 65 °C	151	–	
NV _C	Endurance	Over operating temperature	10 ¹⁴	–	Cycles

Capacitance

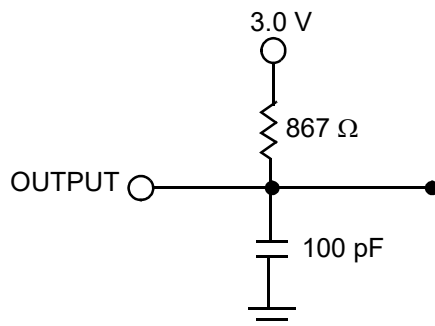
Parameter ^[6]	Description	Test Conditions	Max	Unit
C _{IO}	Input/Output pin capacitance (SDA)	T _A = 25 °C, f = 1 MHz, V _{DD} = V _{DD} (typ)	8	pF
C _I	Input pin capacitance		6	pF

Thermal Resistance

Parameter ^[6]	Description	Test Conditions	8-pin SOIC	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	146	°C/W
Θ _{JC}	Thermal resistance (junction to case)		48	°C/W

AC Test Loads and Waveforms

Figure 17. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels10% and 90% of V_{DD}
 Input rise and fall times 10 ns
 Input and output timing reference levels0.5 × V_{DD}
 Output load capacitance 100 pF

Note

6. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

Over the [Operating Range](#)

Parameters ^[7]		Description	Fast-mode Plus (Fm+) ^[9]		Hs-mode ^[9]		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	
f_{SCL} ^[8]		SCL clock frequency	–	1.0	–	3.4	MHz
$t_{SU;STA}$		Start condition setup for repeated Start	260	–	160	–	ns
$t_{HD;STA}$		Start condition hold time	260	–	160	–	ns
t_{LOW}		Clock LOW period	500	–	160	–	ns
t_{HIGH}		Clock HIGH period	260	–	60	–	ns
$t_{SU;DAT}$	$t_{SU;DATA}$	Data in setup	50	–	10	–	ns
$t_{HD;DAT}$	$t_{HD;DATA}$	Data in hold	0	–	0	70	ns
t_{DH}		Data output hold (from SCL at V_{IL})	0	–	0	–	ns
t_R ^[10]	t_r	Input rise time	–	120	10	80	ns
t_F ^[10]	t_f	Input fall time	$20 \times (V_{DD} / 5.5 V)$	120	10	80	ns
$t_{SU;STO}$		STOP condition setup	260	–	160	–	ns
t_{AA}	$t_{VD;DATA}$	SCL LOW to SDA Data Out Valid	–	450	–	130	ns
$t_{VD;ACK}$		ACK output valid time	–	450	–	130	ns
t_{OF} ^[10]		Output fall time from V_{IH} min to V_{IL} max	$20 \times (V_{DD} / 5.5 V)$	120	–	80	ns
t_{BUF}		Bus free before new transmission	500	–	300	–	ns
t_{SP}		Noise suppression time constant on SCL, SDA	0	50	–	5	ns

Figure 18. Read Bus Timing Diagram

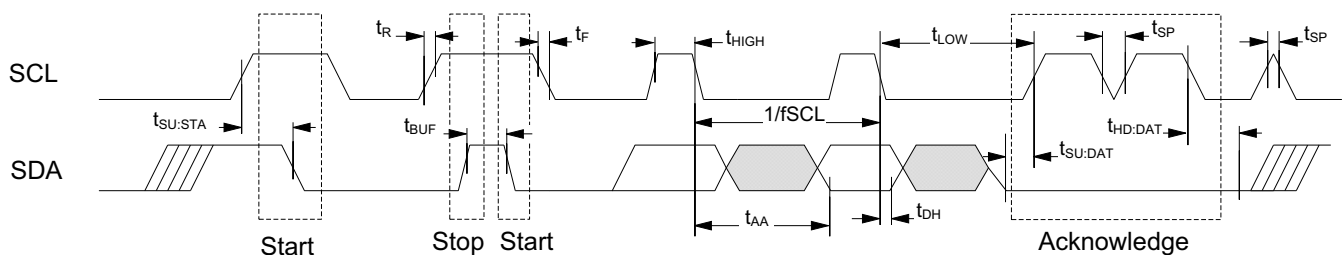
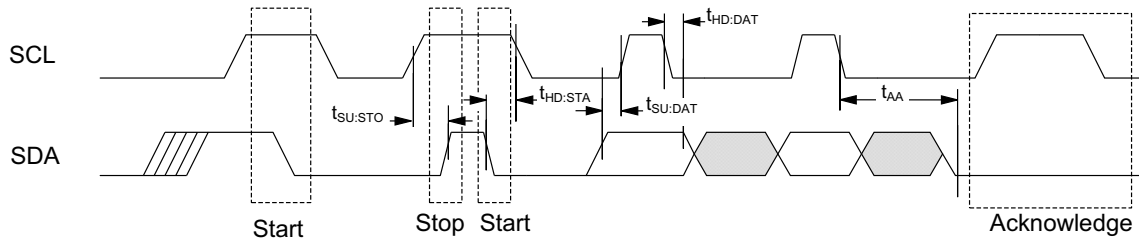


Figure 19. Write Bus Timing Diagram



Notes

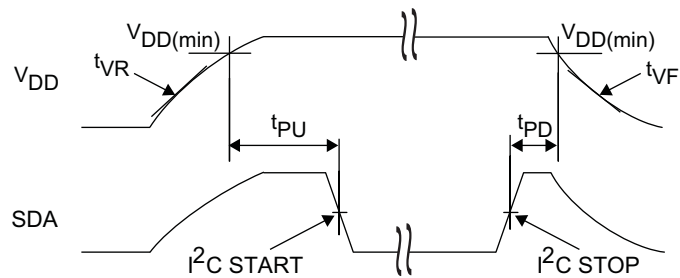
7. Test conditions assume signal transition time of 10 ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0 to V_{DD} (typ), and output loading of the specified I_{OL} and 100 pF load capacitance shown in [Figure 17 on page 13](#).
8. The speed-related specifications are guaranteed characteristic points along a continuous curve of operation from DC to $f_{SCL}(\text{max})$.
9. Bus Load (C_b) considerations; $C_b < 550$ pF for I²C clock frequency (SCL) 1 MHz; $C_b < 100$ pF for SCL at 3.4 MHz.
10. These parameters are guaranteed by design and are not tested.

Power Cycle Timing

Over the [Operating Range](#)

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up $V_{DD}(\text{min})$ to first access (START condition)	250	–	μs
t_{PD}	Last access (STOP condition) to power-down ($V_{DD}(\text{min})$)	0	–	μs
$t_{VR}^{[11, 12]}$	V_{DD} power-up ramp rate	50	–	$\mu\text{s/V}$
$t_{VF}^{[11, 12]}$	V_{DD} power-down ramp rate	100	–	$\mu\text{s/V}$
t_{REC}	Recovery time from sleep mode	–	400	μs

Figure 20. Power Cycle Timing



Notes

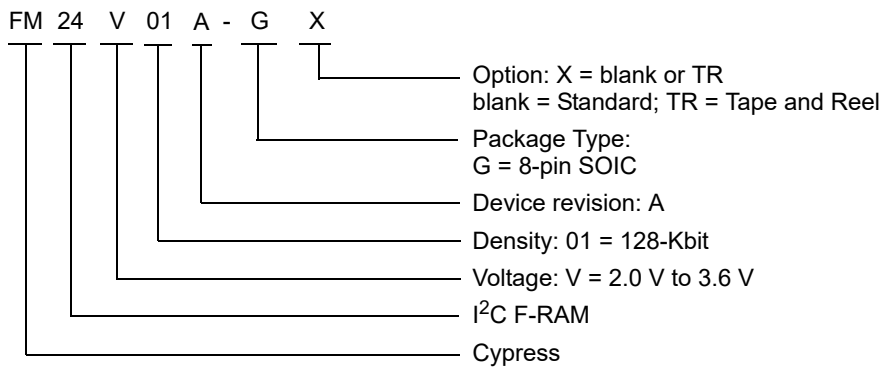
- 11. Slope measured at any point on the V_{DD} waveform.
- 12. These parameters are guaranteed by design and are not tested.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM24V01A-G	51-85066	8-pin SOIC	Industrial
FM24V01A-GTR	51-85066	8-pin SOIC	

All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

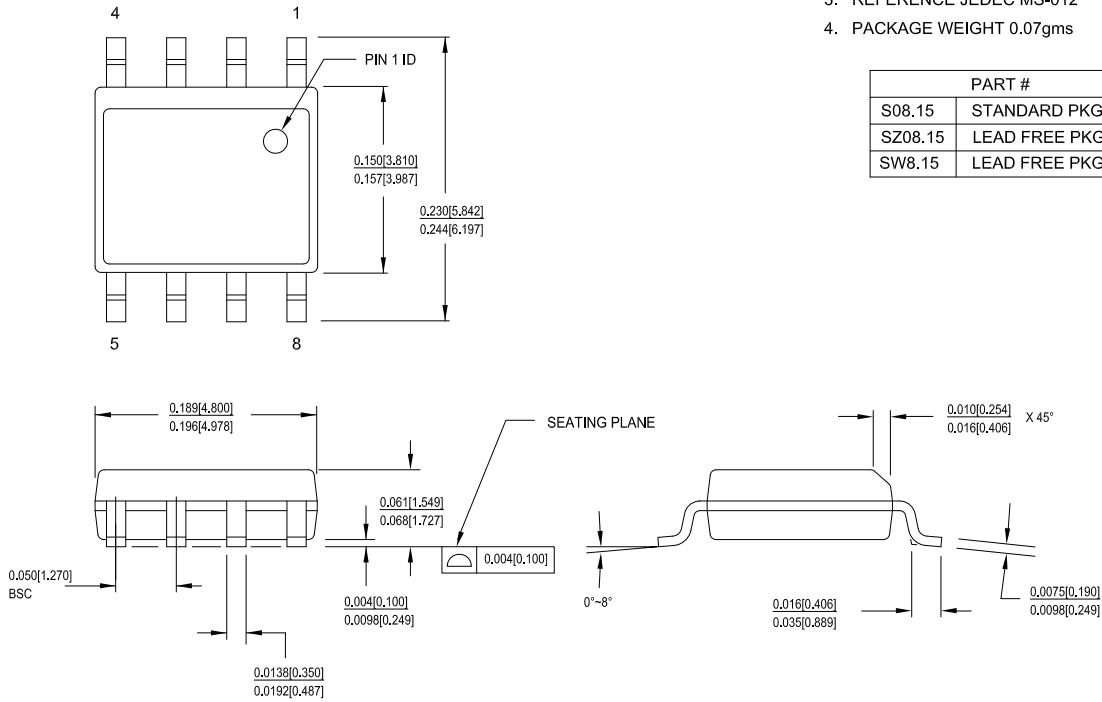


Package Diagram

Figure 21. 8-pin SOIC (150 Mils) Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *1

Acronyms

Acronym	Description
ACK	Acknowledge
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I ² C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LSB	Least Significant Bit
MSB	Most Significant Bit
NACK	No Acknowledge
RoHS	Restriction of Hazardous Substances
R \bar{W}	Read/Write
SCL	Serial Clock Line
SDA	Serial Data Access
SOIC	Small Outline Integrated Circuit
WP	Write Protect

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
Kb	1024 bit
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM24V01A, 128-Kbit (16K × 8) Serial (I ² C) F-RAM				
Document Number: 001-90869				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	4266210	GVCH	01/29/2014	New data sheet.
*A	4390913	GVCH	06/20/2014	<p>Changed status from Advance to Preliminary.</p> <p>Updated Maximum Ratings:</p> <p>Removed "Machine Model" under "Electrostatic Discharge Voltage".</p> <p>Updated DC Electrical Characteristics:</p> <p>Added typical values for I_{SB} and I_{ZZ} parameters.</p> <p>Splitted V_{IH} parameter into two rows namely "SDL, SDA" and "WP, A2-A0".</p> <p>Changed maximum value of V_{IH} parameter from "V_{DD} + 0.5 V" to "V_{DD}(max) + 0.3 V" corresponding to "SDL, SDA" and from "V_{DD} + 0.5 V" to "V_{DD} + 0.3 V" corresponding to "WP, A2-A0".</p> <p>Changed minimum value of V_{IL} parameter from -0.5 V to -0.3 V.</p> <p>Renamed V_{OL1} as V_{OL} parameter.</p> <p>Added details of V_{OL} parameter corresponding to Test Condition "I_{OL} = 6 mA".</p> <p>Removed V_{OL2} parameter and its details.</p> <p>Added V_{hys} parameter and its details.</p> <p>Updated Capacitance:</p> <p>Removed C_O parameter and its details.</p> <p>Added C_{IO} parameter and its details.</p> <p>Updated AC Switching Characteristics:</p> <p>Added maximum values for t_{AA}, t_{VD;ACK}, t_{OF}, t_{BUF} parameters corresponding to "Hs-mode".</p> <p>Removed Note "In Hs-mode and V_{DD} < 2.7 V, the t_{SU;DAT} (min.) spec is 15 ns." and its reference in t_{SU;DAT} parameter.</p>
*B	4512788	GVCH	09/24/2014	<p>Updated DC Electrical Characteristics:</p> <p>Added Note 3 and referred the same note in V_{OL} parameter.</p>
*C	4571858	GVCH	11/18/2014	<p>Updated DC Electrical Characteristics:</p> <p>Changed minimum value of V_{hys} parameter from "0.1 × V_{DD}" to "0.05 × V_{DD}" corresponding to Test Condition "f_{SCL} = 3.4 MHz".</p> <p>Added Note 5 and referred the same note in V_{hys} parameter.</p>
*D	4596783	GVCH	12/17/2014	<p>Updated Features:</p> <p>Added Note 1 and referred the same note in "Up to 3.4-MHz frequency".</p> <p>Updated Two-wire Interface:</p> <p>Updated description (Added description for the difference in I_{OL} and V_{hys} with respect to NXP I²C specification).</p> <p>Updated DC Electrical Characteristics:</p> <p>Changed minimum value of V_{hys} parameter from "0.05 × V_{DD}" to "0.06 × V_{DD}" corresponding to Test Condition "f_{SCL} = 3.4 MHz".</p> <p>Updated Note 3.</p> <p>Updated Note 5.</p> <p>Updated to new template.</p> <p>Completing Sunset Review.</p>
*E	4651363	ZSK	02/10/2015	<p>Changed status from Preliminary to Final.</p> <p>Updated Functional Description:</p> <p>Added "For a complete list of related resources, click here." at the end.</p> <p>Updated Package Diagram:</p> <p>spec 51-85066 – Changed revision from *F to *G.</p>

Document History Page (continued)

Document Title: FM24V01A, 128-Kbit (16K × 8) Serial (I ² C) F-RAM				
Document Number: 001-90869				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*F	4874478	ZSK / PSR	08/06/2015	Updated Maximum Ratings : Removed “Maximum junction temperature” and its corresponding details. Added “Maximum accumulated storage time” and its corresponding details. Added “Ambient temperature with power applied” and its corresponding details.
*G	5006363	GVCH	11/07/2015	Updated AC Switching Characteristics : Updated Figure 18 (Fixed typo (Changed the timing reference from t _{SU:SDA} to t _{SU:STA})). Updated Figure 19 (Made t _{HD:STA} parameter visible in diagram). Updated Package Diagram : spec 51-85066 – Changed revision from *G to *H. Completing Sunset Review.
*H	5085665	GVCH	01/14/2016	Updated Ordering Information : Updated part numbers.
*I	5452467	ZSK	09/28/2016	Updated Power Cycle Timing : Changed minimum value of t _{PU} parameter from 1 ms to 250 μs. Updated to new template.
*J	6083747	GVCH	02/28/2018	Updated Package Diagram : spec 51-85066 – Changed revision from *H to *I. Updated to new template.
*K	6422002	GVCH	12/26/2018	Updated Maximum Ratings : Replaced “–55 °C to +125 °C” with “–65 °C to +125 °C” in ratings corresponding to “Storage temperature”. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2014–2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.