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CYW4343W

Single-Chip 802.11 b/g/n MAC/Baseband/Radio with Bluetooth 4.1

The Cypress CYW4343W is a highly integrated single-chip solution and offers the lowest RBOM in the industry for wearables, Internet of Things (IoT) gateways, home automation, and a wide range of other portable devices. The chip includes a 2.4 GHz WLAN IEEE 802.11 b/g/n MAC/baseband/radio and Bluetooth 4.1 support. In addition, it integrates a power amplifier (PA) that meets the output power requirements of most handheld systems, a low-noise amplifier (LNA) for best-in-class receiver sensitivity, and an internal transmit/receive (iTR) RF switch, further reducing the overall solution cost and printed circuit board area.

The WLAN host interface supports SPI (gSPI)[1] and SDIO v2.0 modes, providing a raw data transfer rate up to 200 Mbps when operating in 4-bit mode at a 50 MHz bus frequency. An independent, high-speed UART is provided for the Bluetooth host interface. Using advanced design techniques and process technology to reduce active and idle power, the CYW4343W is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit that simplifies the system power topology and allows for operation directly from a rechargeable mobile platform battery while maximizing battery life.

The CYW4343W implements the world's most advanced Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative WLAN and Bluetooth coexistence.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4343W	CYW4343W
BCM4343WKUBG	CYW4343WKUBG

Features

IEEE 802.11x Key Features

- Single-band 2.4 GHz IEEE 802.11b/g/n.
- Support for 2.4 GHz TurboQAM® data rates (256-QAM) and 20 MHz channel bandwidth.
- Integrated iTR switch supports a single 2.4 GHz antenna shared between WLAN and Bluetooth.
- Supports explicit IEEE 802.11n transmit beamforming
- Tx and Rx Low-density Parity Check (LDPC) support for improved range and power efficiency.
- Supports standard SDIO v2.0 and gSPI[1] host interfaces.
- Supports Space-Time Block Coding (STBC) in the receiver.
- Integrated ARM Cortex-M3 processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field-upgrade with future features. On-chip memory includes 512 KB SRAM and 640 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as to future devices.

Bluetooth Features

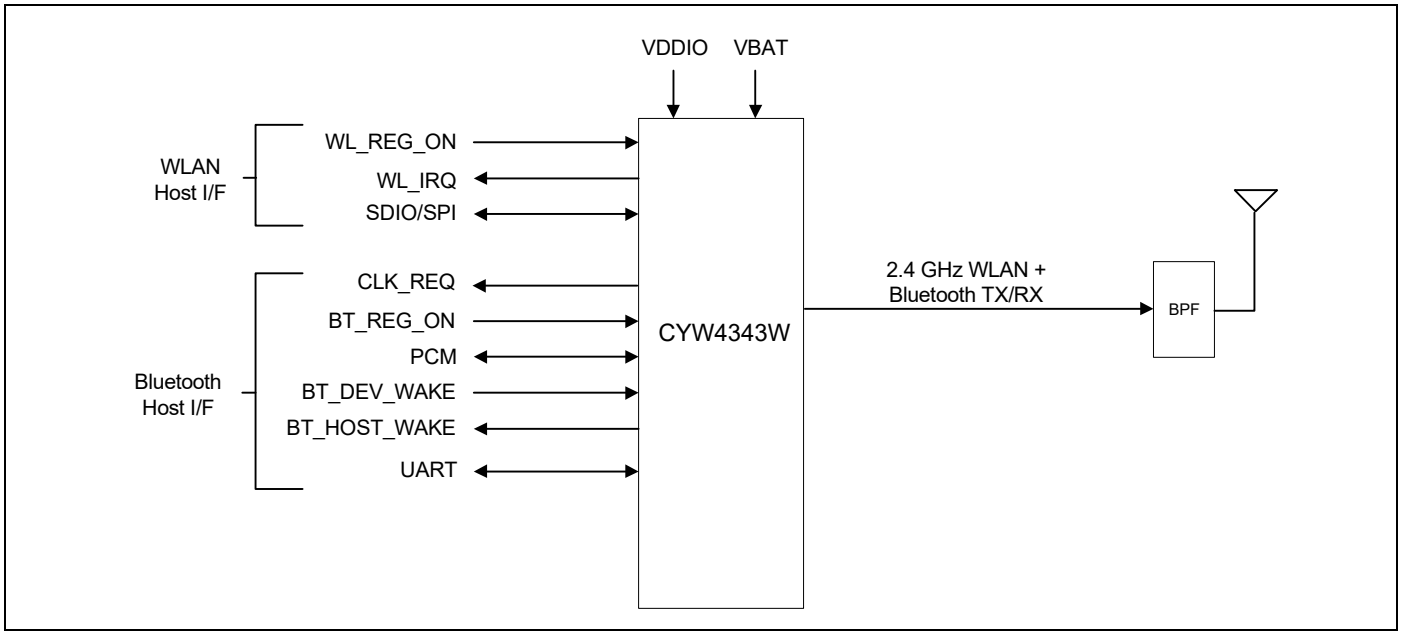
- Complies with Bluetooth Core Specification Version 4.1 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference.
- Interface support — Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data.
- Low-power consumption improves battery life of handheld devices.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.

Note
1. SPI availability may depend on module design. Check with the module manufacturer to confirm.

General Features

- Supports a battery voltage range from 3.0V to 4.8V with an internal switching regulator.
- Programmable dynamic power management.
- 4 Kbit One-Time Programmable (OTP) memory for storing board parameters.
- Can be routed on low-cost 1 x 1 PCB stack-ups.
- 74-ball[4343W+43CS4343W1]74-ball 63-ball WLBGA package (4.87 mm × 2.87 mm, 0.4 mm pitch).
- 153-bump WLCSP package (115 µm bump diameter, 180 µm bump pitch).
- Security:
  - WPA and WPA2 (Personal) support for powerful encryption and authentication.
  - AES in WLAN hardware for faster data encryption and IEEE 802.11i compatibility.
  - Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0).
  - Reference WLAN subsystem provides Wi–Fi Protected Setup (WPS).
- Worldwide regulatory support: Global products supported with worldwide homologated design.

Figure 1. CYW4343W System Block Diagram



Contents

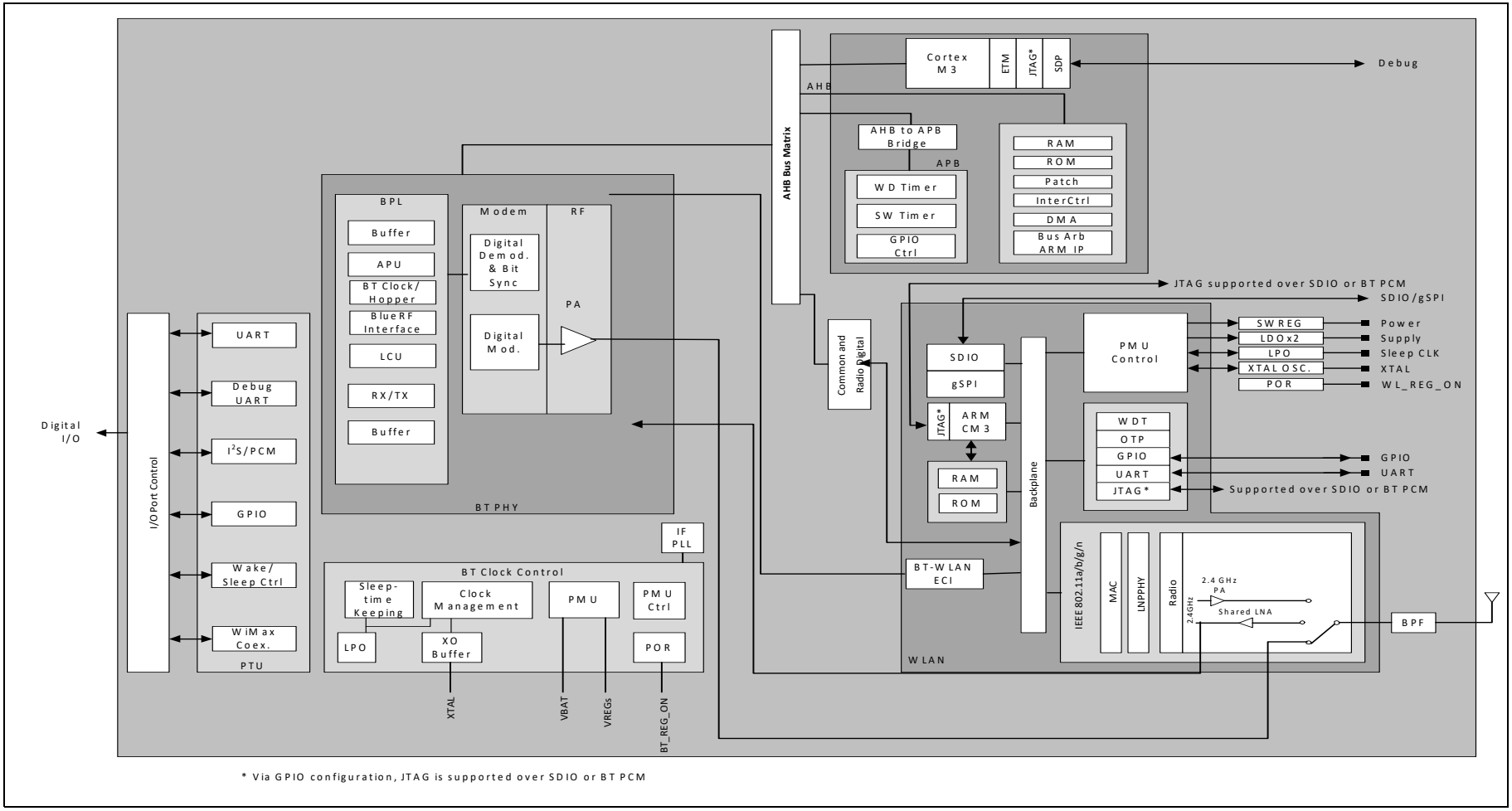
1. Overview

1.1 Overview

The CYW4343W provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 b/g/n. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. The CYW4343W is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnection of all the major physical blocks in the CYW4343W and their associated external interfaces, which are described in greater detail in subsequent sections.

Figure 2. CYW4343W Block Diagram



1.2 Features

The CYW4343W supports the following WLAN and Bluetooth features:

- IEEE 802.11b/g/n single-band radio with an internal power amplifier, LNA, and T/R switch
- Bluetooth v4.1 with integrated Class 1 PA
- Concurrent Bluetooth, and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Simultaneous BT/WLAN reception with a single antenna
- WLAN host interface options:
  - SDIO v2.0, including default and high-speed timing.
- BT UART (up to 4 Mbps) host digital interface that can be used concurrently with the above WLAN host interfaces.
- ECI—enhanced coexistence support, which coordinates BT SCO transmissions around WLAN receptions.
- I^2S/PCM for BT audio
- HCI high-speed UART (H4 and H5) transport support
- Wideband speech support (16 bits, 16 kHz sampling PCM, through I^2S and PCM interfaces)
- Bluetooth SmartAudio® technology improves voice and music quality to headsets.
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)

1.3 Standards Compliance

The CYW4343W supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0
- Bluetooth 4.1 (Bluetooth Low Energy)
- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The CYW4343W will support the following future drafts/standards:

- IEEE 802.11r — Fast Roaming (between APs)
- IEEE 802.11k — Resource Management
- IEEE 802.11w — Secure Management Frames
- IEEE 802.11 Extensions:
- IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
- IEEE 802.11i MAC Enhancements
- IEEE 802.11r Fast Roaming Support
- IEEE 802.11k Radio Resource Measurement

The CYW4343W supports the following security features and proprietary protocols:

- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
- IEEE 802.15.2 Coexistence Compliance — on silicon solution compliant with IEEE 3-wire requirements.

2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW4343W. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

A single VBAT (3.0V to 4.8V DC maximum) and VDDIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW4343W.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power up the regulators and take the respective circuit blocks out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO can be turned on and off based on the dynamic demands of the digital baseband.

The CYW4343W allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, LPLDO1 provides the CYW4343W with all required voltage, further reducing leakage currents.

Note: VBAT should be connected to the LDO_VDDBAT5V and SR_VDDBAT5V pins of the device.

Note: VDDIO should be connected to the SYS_VDDIO and WCC_VDDIO pins of the device.

2.2 CYW4343W PMU Features

The PMU supports the following:

- VBAT to 1.35Vout (170 mA nominal, 370 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (250 mA nominal, 450 mA maximum 800 mA peak maximum) LDO3P3
- 1.35V to 1.2Vout (100 mA nominal, 150 mA maximum) LNLDO
- 1.35V to 1.2Vout (80 mA nominal, 200 mA maximum) CLDO with bypass mode for deep sleep
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from extremely low power-consumption mode.
- PMU input supplies automatic sensing and fast switching to support A4WP operations.

Figure 3 and Figure 4 show the typical power topology of the CYW4343W.

Figure 3. Typical Power Topology (1 of 2)

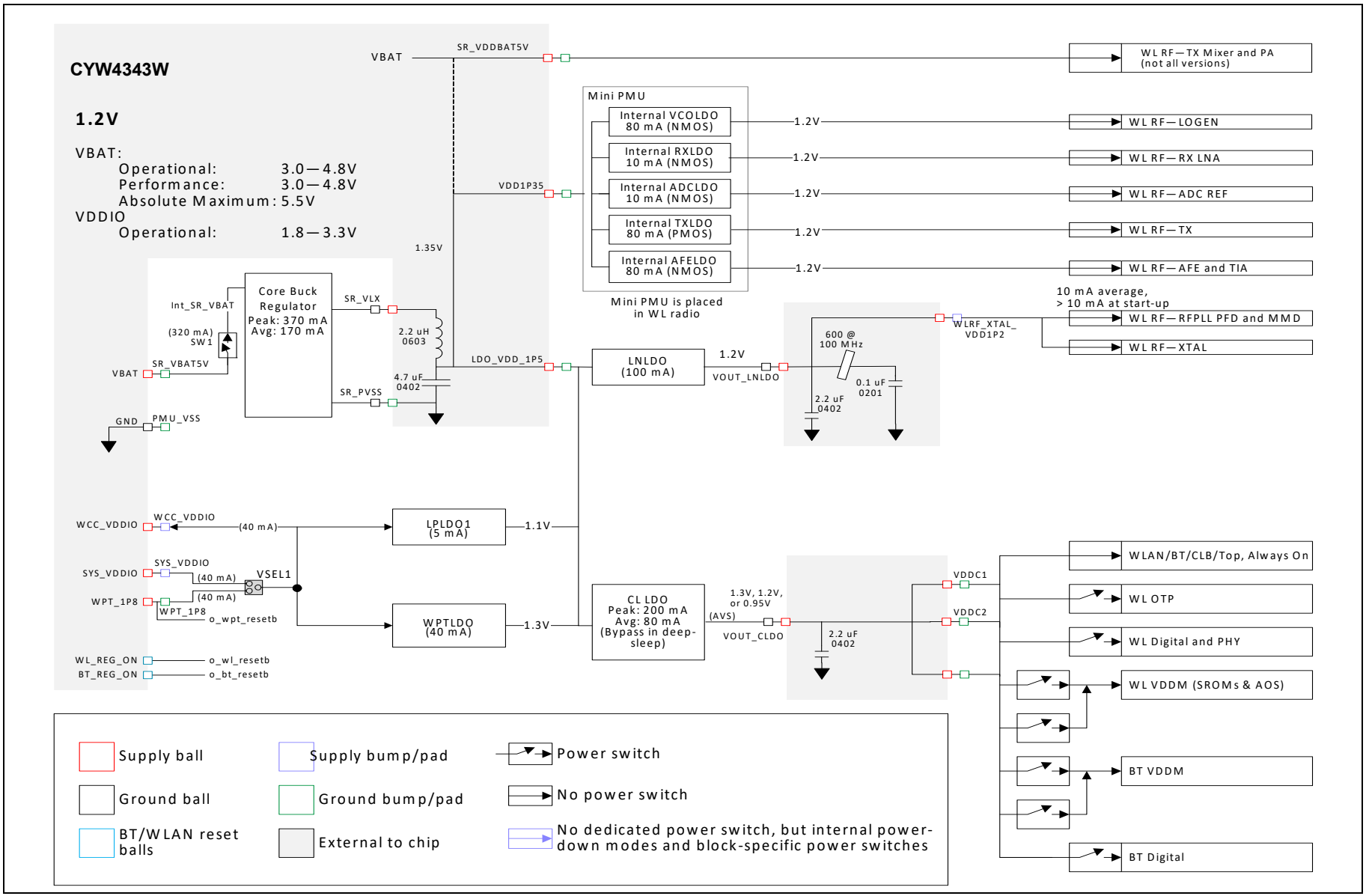
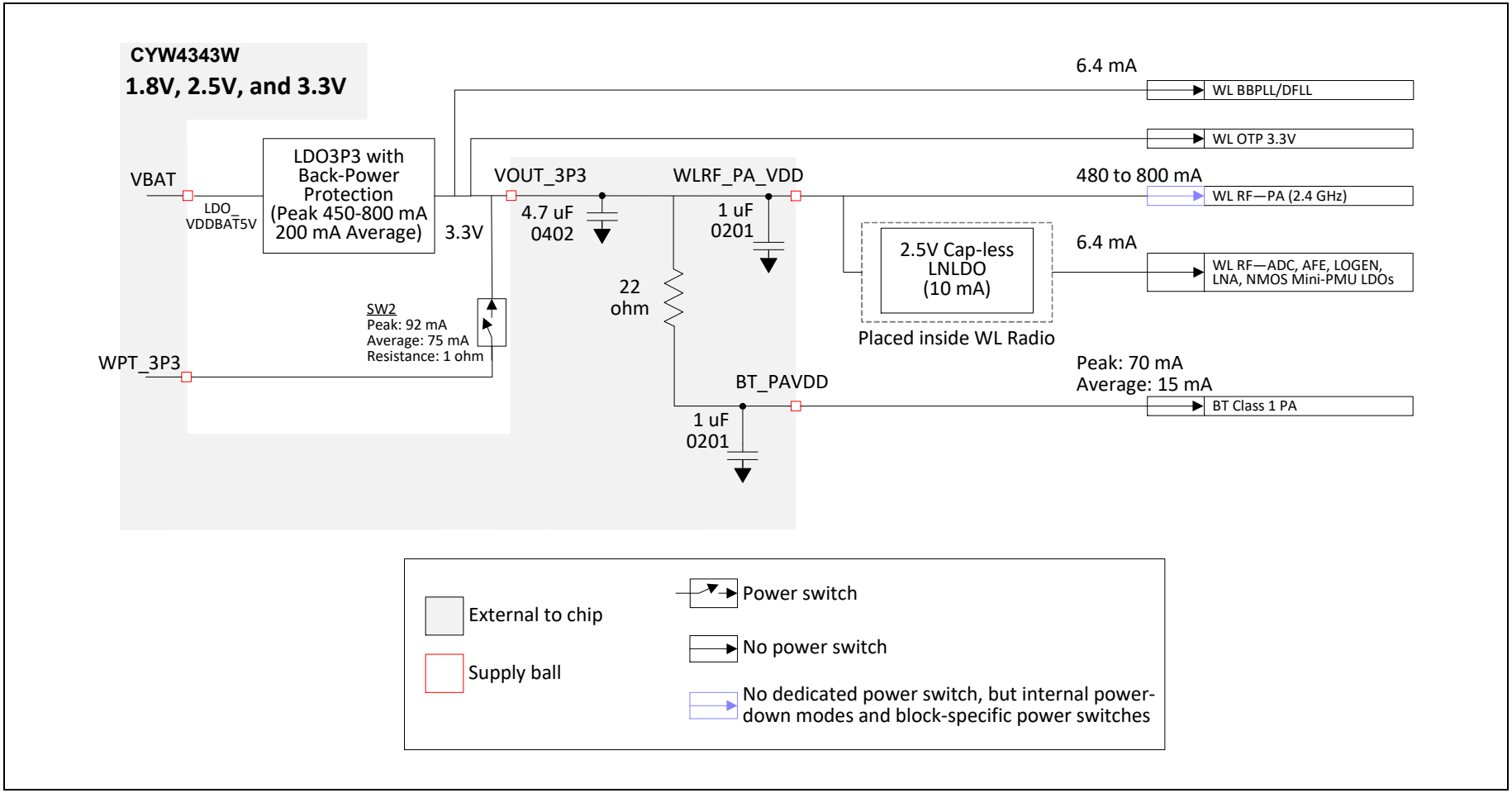


Figure 4. Typical Power Topology (2 of 2)



2.3 WLAN Power Management

The CYW4343W has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW4343W integrated RAM is a high volatile memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW4343W includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW4343W into various power management states appropriate to the operating environment and the activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at the 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW4343W WLAN power states are described as follows:

- Active mode—All WLAN blocks in the CYW4343W are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW4343W remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip, including analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved to retention memory in the always-on domain before the digital core is powered off. To avoid lengthy hardware reinitialization, the logic states in the digital core are restored to their pre-deep-sleep settings when a wake-up event is triggered by an external interrupt, a host resume through the SDIO bus, or by the PMU timers.
- Power-down mode—The CYW4343W is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is used to minimize system power consumption. It enables and disables various system resources based on a computation of required resources and a table that describes the relationship between resources and the time required to enable and disable them.

Resource requests can derive from several sources: clock requests from cores, the minimum resources defined in the *ResourceMin* register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of the following four states:

- enabled
- disabled
- transition_on
- transition_off

The timer value is 0 when the resource is enabled or disabled and nonzero during state transition. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can transition immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can transition immediately from enabled to disabled. The terms *enable sequence* and *disable sequence* refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW4343W provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW4343W is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW4343W to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the CYW4343W, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW4343W to be fully integrated in an embedded device and to take full advantage of the lowest power-savings modes.

When the CYW4343W is powered on from this state, it is the same as a normal power-up, and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW4343W has two signals (see Table 2) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Power-Up Sequence and Timing.

Table 2. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4343W regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW4343W regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

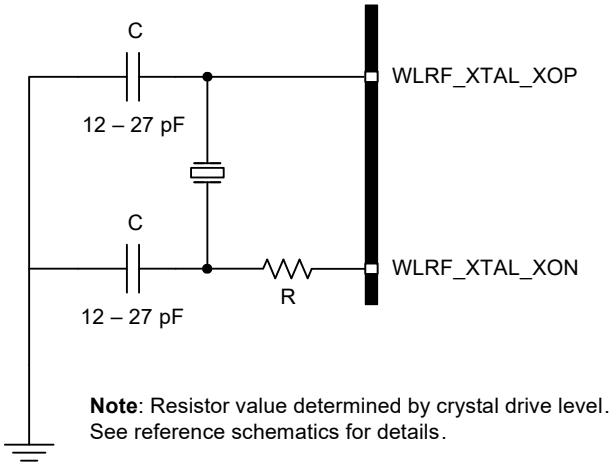
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW4343W can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 5. Consult the reference schematics for the latest configuration.

Figure 5. Recommended Oscillator Configuration



The CYW4343W uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing so that it can operate using numerous frequency references. The frequency reference can be an external source such as a TCXO or a crystal interfaced directly to the CYW4343W.

The default frequency reference setting is a 37.4 MHz crystal or TCXO. The signal requirements and characteristics for the crystal interface are shown in Table 3.

Note: Although the fractional-N synthesizer can support many reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

3.2 TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the phase noise requirements listed in Table 3.

If the TCXO is dedicated to driving the CYW4343W, it should be connected to the WLRF_XTAL_XOP pin through an external capacitor with value ranges from 200 pF to 1000 pF as shown in Figure 6.

Figure 6. Recommended Circuit to Use with an External Dedicated TCXO

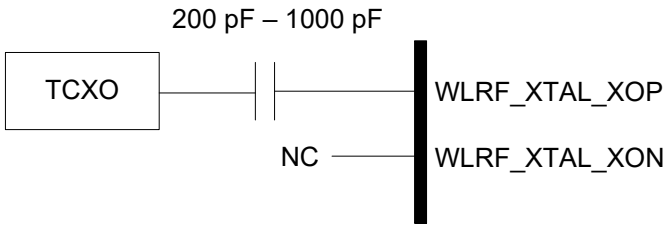


Table 3. Crystal Oscillator and External Clock Requirements and Performance

Parameter	Conditions/Notes	Crystal			External Frequency Reference			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	–	–	37.4[a]	–	–	–	–	MHz
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input Impedance (WLRF_XTAL_XOP)	Resistive	–	–	–	10k	100k	–	Ω
	Capacitive	–	–	–	–	–	7	pF
WLRF_XTAL_XOP input voltage	AC-coupled analog signal	–	–	–	400[b]	–	1260	mV_{p-p}
WLRF_XTAL_XOP input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WLRF_XTAL_XOP input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
Frequency tolerance Initial + over temperature	–	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[c, d, e] (IEEE 802.11 b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase Noise[c, d, e] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase Noise[c, d, e] (256-QAM)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–140	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–147	dBc/Hz

a. The frequency step size is approximately 80 Hz. The CYW4343W does not auto-detect the reference clock frequency; the frequency is specified in the software and/or NVRAM file.
b. To use 256-QAM, a 800 mV minimum voltage is required.
c. For a clock reference other than 37.4 MHz, 20 × log10(f/37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
d. Phase noise is assumed flat above 100 kHz.
e. The CYW4343W supports a 26 MHz reference clock sharing option. See the phase noise requirement in the table.

3.3 External 32.768 kHz Low-Power Oscillator

The CYW4343W uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 4.

Note: The CYW4343W will auto-detect the LPO clock. If it senses a clock on the EXT_SLEEP_CLK pin, it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

- To use the internal LPO: Tie EXT_SLEEP_CLK to ground. Do not leave this pin floating.
- To use an external LPO: Connect the external 32.768 kHz clock to EXT_SLEEP_CLK.

Table 4. External 32.768 kHz Sleep-Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square wave or sine wave	–
Input impedance[a]	>100	kΩ
	<5	pF
Clock jitter	<10,000	ppm

a. When power is applied or switched off.

4. WLAN System Interfaces

4.1 SDIO v2.0

The CYW4343W WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps) and 4-bit modes (100 Mbps), as well as high speed 4-bit mode (50 MHz clocks—200 Mbps). It has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

SDIO mode is enabled using the strapping option pins. See Table 22 for details.

Three functions are supported:

- Function 0 standard SDIO function. The maximum block size is 32 bytes.
- Function 1 backplane function to access the internal System-on-a-Chip (SoC) address space. The maximum block size is 64 bytes.
- Function 2 WLAN function for efficient WLAN packet transfer through DMA. The maximum block size is 512 bytes.

4.1.1 SDIO Pin Descriptions

Table 5. SDIO Pin Descriptions

SD 4-Bit Mode		SD 1-Bit Mode		gSPI Mode	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2	NC	Not used	NC	Not used
DATA3	Data line 3	NC	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

Figure 7. Signal Connections to SDIO Host (SD 4-Bit Mode)

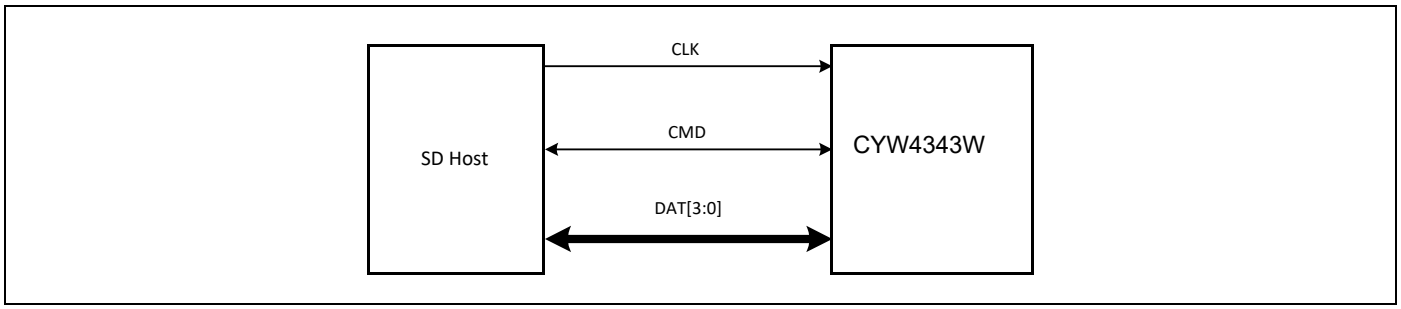
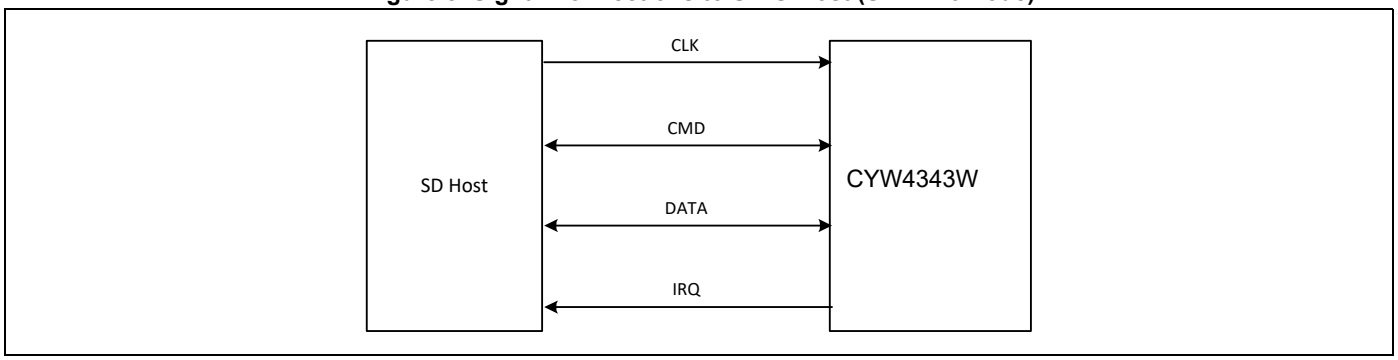


Figure 8. Signal Connections to SDIO Host (SD 1-Bit Mode)



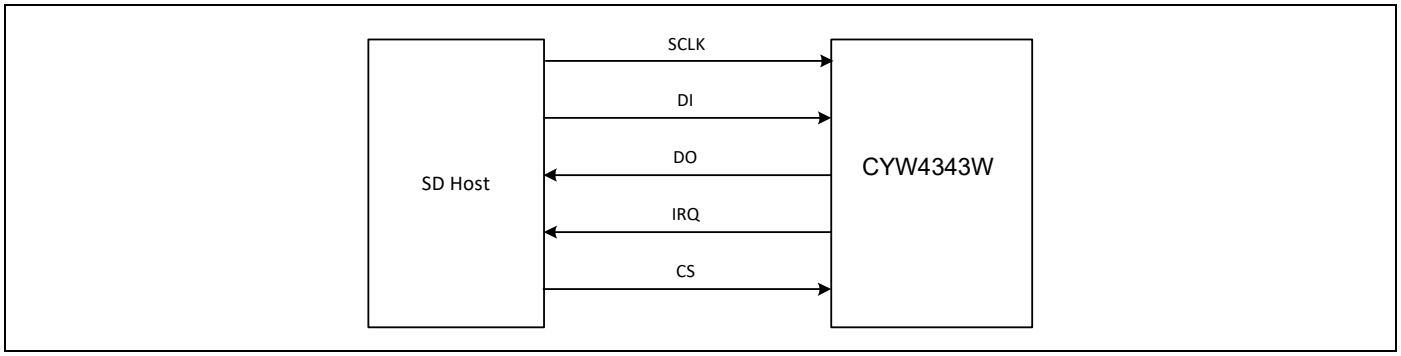
4.2 Generic SPI Mode

In addition to the full SDIO mode, the CYW4343W includes the option of using the simplified generic SPI (gSPI) interface/protocol. Characteristics of the gSPI mode include:

- Up to 50 MHz operation
- Fixed delays for responses and data from the device
- Alignment to host gSPI frames (16 or 32 bits)
- Up to 2 KB frame size per transfer
- Little-endian and big-endian configurations
- A configurable active edge for shifting
- Packet transfer through DMA for WLAN

gSPI mode is enabled using the strapping option pins. See Table 22 for details.

Figure 9. Signal Connections to SDIO Host (gSPI Mode)



4.3 SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianess is supported in both modes. Figure 10 and Figure 11 show the basic write and write/read commands.

Figure 10. gSPI Write Protocol

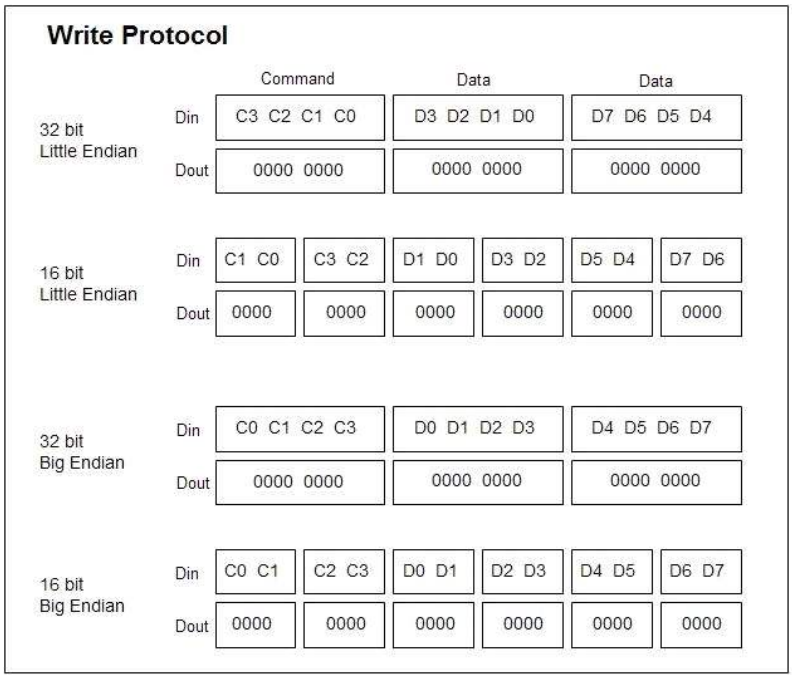
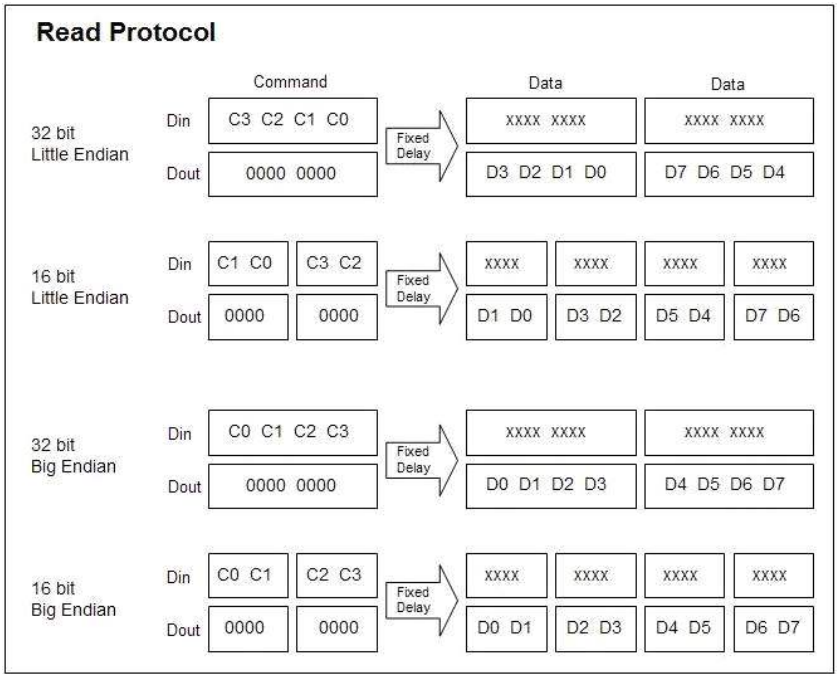


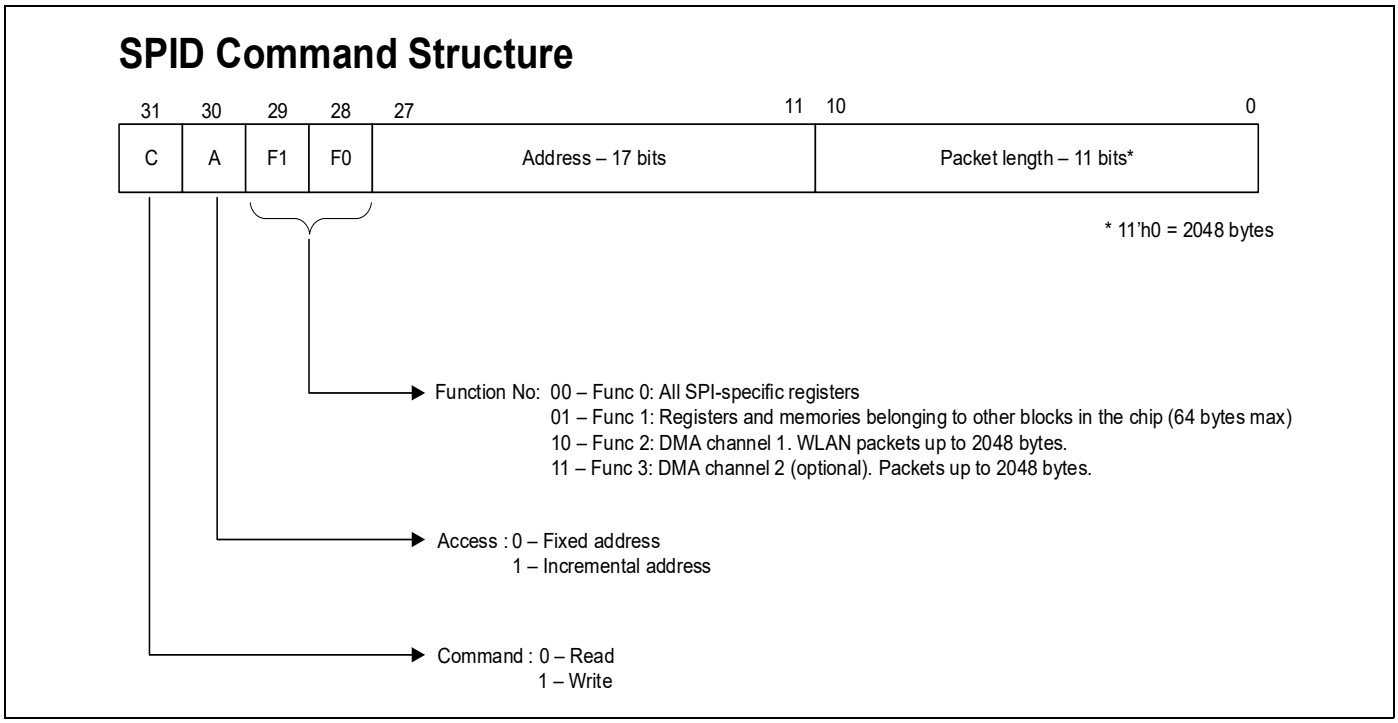
Figure 11. gSPI Read Protocol



4.3.1 Command Structure

The gSPI command structure is 32 bits. The bit positions and definitions are shown in Figure 12.

Figure 12. gSPI Command Structure



4.3.1.1 Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the gSPI clock. The device samples the data on the active edge.

4.3.1.2 Write/Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising-clock edge of the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

4.3.1.3 Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write/read command in the following respects: a) chip selects go high between the command/address and the data, and b) the time interval between the command/address is not fixed.

4.3.2 Status

The gSPI interface supports status notification to the host after a read/write transaction. This status notification provides information about packet errors, protocol errors, available packets in the RX queue, etc. The status information helps reduce the number of interrupts to the host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The gSPI bus timing for read/write transactions with and without status notification are as shown in Figure 13 below and Figure 14. See Table 6 for information on status-field details.

Figure 13. gSPI Signal Timing Without Status

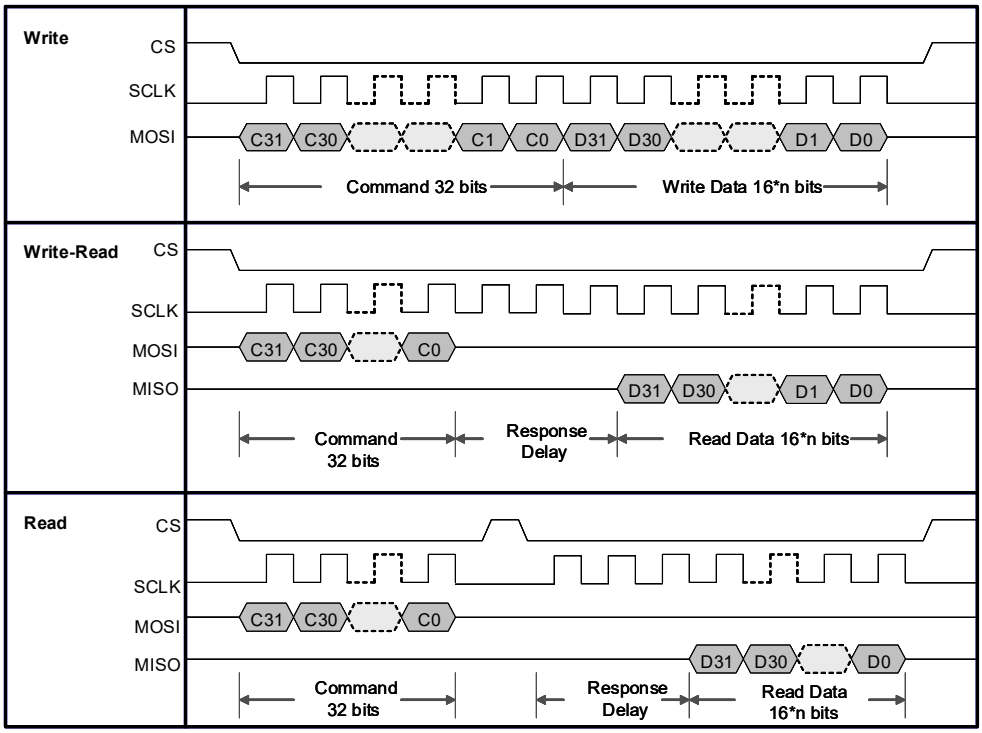


Figure 14. gSPI Signal Timing with Status (Response Delay = 0)

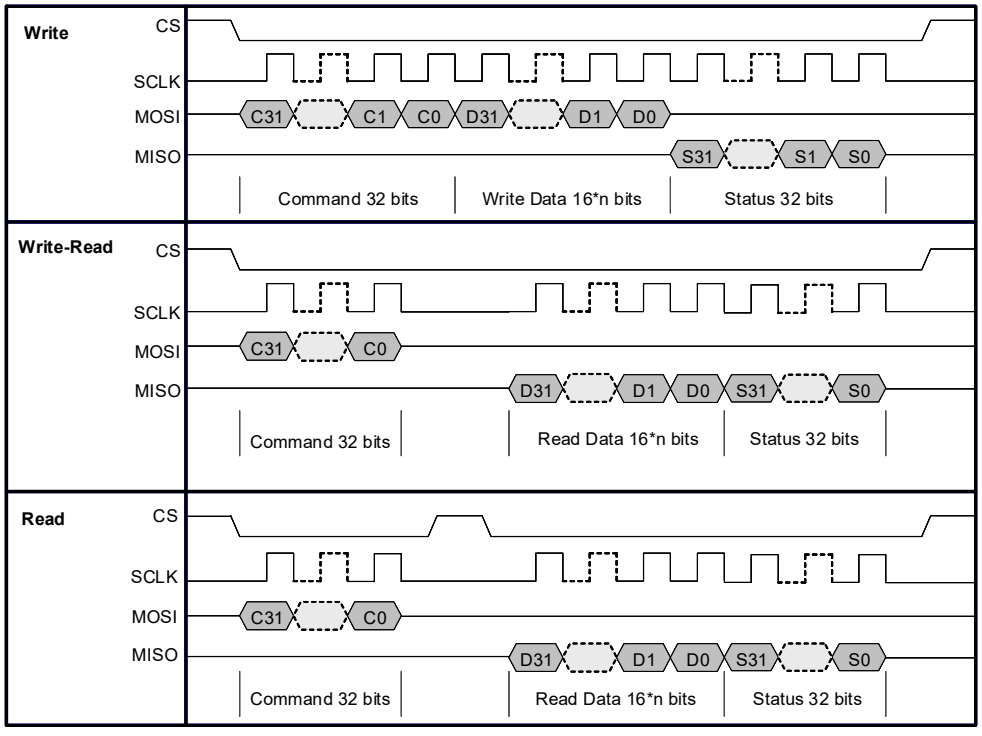


Table 6. gSPI Status Field Details

Bit	Name	Description
0	Data not available	The requested read data is not available.
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command.
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command.
3	F2 interrupt	F2 channel interrupt.
5	F2 RX ready	F2 FIFO is ready to receive data (FIFO empty).
7	Reserved	–
8	F2 packet available	Packet is available/ready in F2 TX FIFO.
9:19	F2 packet length	Length of packet available in F2 FIFO

4.4 gSPI Host-Device Handshake

To initiate communication through the gSPI after power-up, the host needs to bring up the WLAN chip by writing to the wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the CYW4343W is ready for data transfer. The device can signal an interrupt to the host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the host using the WLAN IRQ line whenever it has any information to pass to the host. On getting an interrupt, the host needs to read the interrupt and/or status register to determine the cause of the interrupt and then take necessary actions.

4.4.1 Boot-Up Sequence

After power-up, the gSPI host needs to wait 50 ms for the device to be out of reset. For this, the host needs to poll with a read command to F0 address 0x14. Address 0x14 contains a predefined bit pattern. As soon as the host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the host needs to set the wake-up WLAN bit (F0 reg 0x00 bit 7). Wake-up WLAN turns the PLL on; however, the PLL doesn't lock until the host programs the PLL registers to set the crystal frequency.

For the first time after power-up, the host needs to wait for the availability of the low-power clock inside the device. Once it is available, the host needs to write to a PMU register to set the crystal frequency. This will turn on the PLL. After the PLL is locked, the chipActive interrupt is issued to the host. This indicates device awake/ready status. See Table 7 for information on gSPI registers.

In Table 7, the following notation is used for register access:

- R: Readable from host and CPU
- W: Writable from host
- U: Writable from CPU

Table 7. gSPI Registers

Address	Register	Bit	Access	Default	Description
x0000	Word length	0	R/W/U	0	0: 16-bit word length 1: 32-bit word length
	Endianess	1	R/W/U	0	0: Little endian 1: Big endian
	High-speed mode	4	R/W/U	1	0: Normal mode. Sample on SPICLK rising edge, output on falling edge. 1: High-speed mode. Sample and output on rising edge of SPICLK (default).
	Interrupt polarity	5	R/W/U	1	0: Interrupt active polarity is low. 1: Interrupt active polarity is high (default).
	Wake-up	7	R/W	0	A write of 1 denotes a wake-up command from host to device. This will be followed by an F2 interrupt from the gSPI device to host, indicating device awake status.

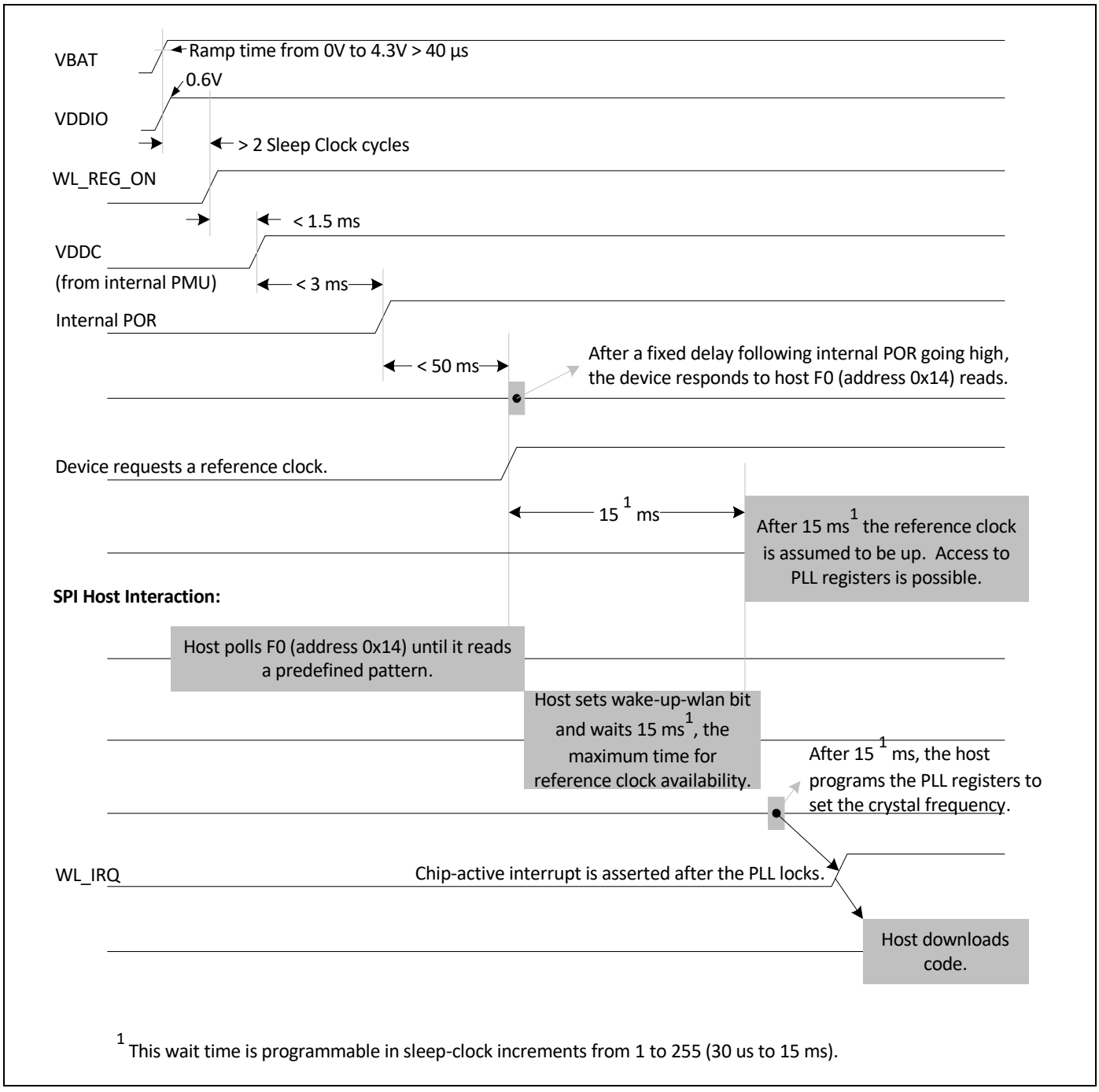
Table 7. gSPI Registers (Cont.)

Address	Register	Bit	Access	Default	Description
x0002	Status enable	0	R/W	1	0: No status sent to host after a read/write. 1: Status sent to host after a read/write.
	Interrupt with status	1	R/W	0	0: Do not interrupt if status is sent. 1: Interrupt host even if status is sent.
x0003	Reserved	–	–	–	–
x0004	Interrupt register	0	R/W	0	Requested data not available. Cleared by writing a 1 to this location.
		1	R	0	F2/F3 FIFO underflow from the last read.
		2	R	0	F2/F3 FIFO overflow from the last write.
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow from the last write.
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006, x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular interrupt is enabled if a corresponding bit is set.
x0008 to x000B	Status register	31:0	R	32'h0000	Same as status bit definitions
x000C, x000D	F1 info. register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 maximum packet size
x000E, x000F	F2 info. register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 maximum packet size
x0014 to x0017	Test-Read only register	31:0	R	32'hFEEDBEAD	This register contains a predefined pattern, which the host can read to determine if the gSPI interface is working properly.
x0018 to x001B	Test–R/W register	31:0	R/W/U	32'h00000000	This is a dummy register where the host can write some pattern and read it back to determine if the gSPI interface is working properly.
x001C to x001F	Response delay registers	7:0	R/W	0x1D = 4, other registers = 0	Individual response delays for F0, F1, F2, and F3. The value of the registers is the number of byte delays that are introduced before data is shifted out of the gSPI interface during host reads.

Figure 15 shows the WLAN boot-up sequence from power-up to firmware download, including the initial device power-on reset (POR) evoked by the WL_REG_ON signal. After initial power-up, the WL_REG_ON signal can be held low to disable the CYW4343W or pulsed low to induce a subsequent reset.

Note: The CYW4343W has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 3 ms after VDDC and VDDIO have both passed the 0.6V threshold.

Figure 15. WLAN Boot-Up Sequence



[1] This wait time is programmable in sleep-clock increments from 1 to 255 (30 us to 15 ms).

5. Wireless LAN MAC and PHY

5.1 MAC Features

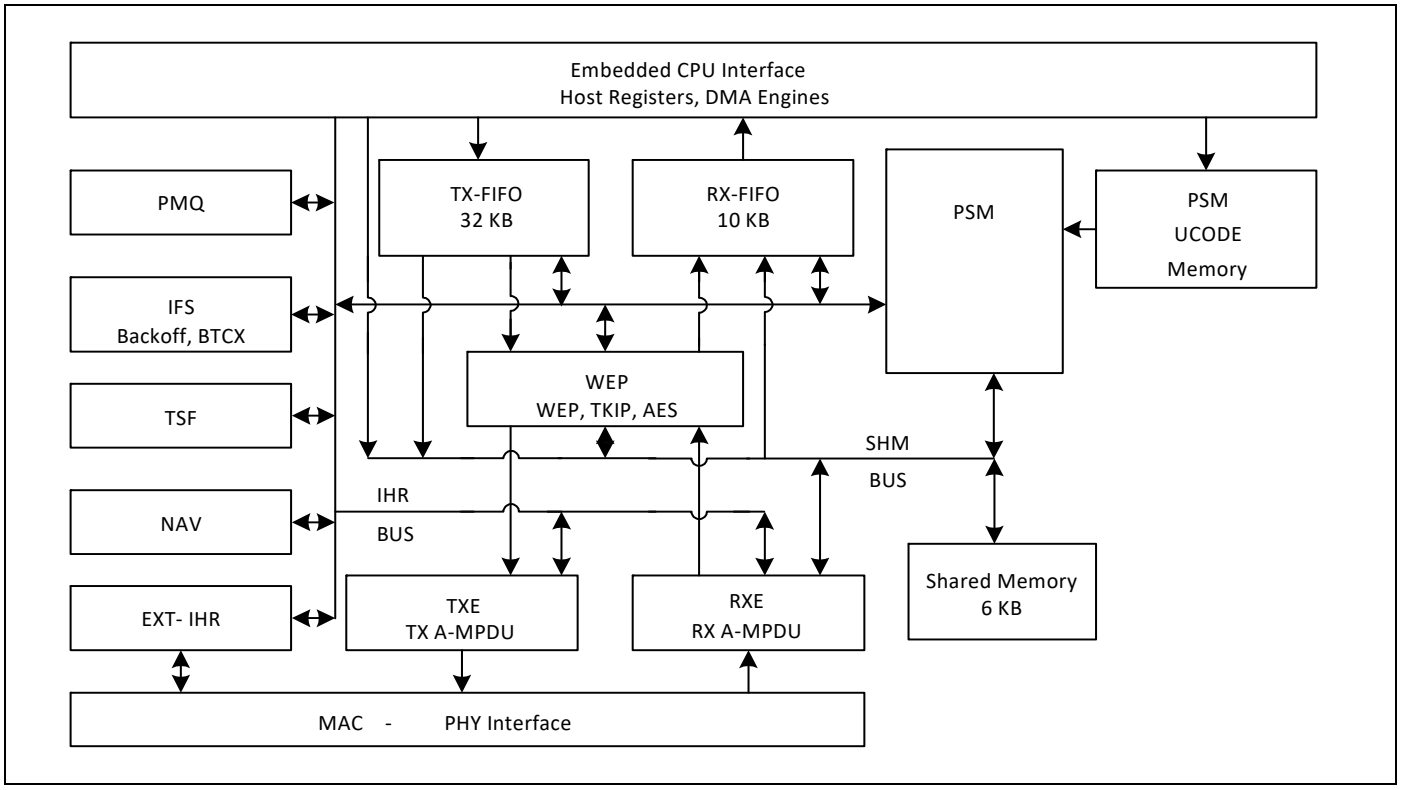
The CYW4343W WLAN MAC supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

- Transmission and reception of aggregated MPDUs (A-MPDU).
- Support for power management schemes, including WMM power-save, power-save multipoll (PSMP) and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware off-load for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management.
- Support for coexistence with Bluetooth and other external radios.
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support.

5.1.1 MAC Description

The CYW4343W WLAN MAC is designed to support high throughput operation with low-power consumption. It does so without compromising on Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power-saving modes that have been implemented allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 16.

Figure 16. WLAN MAC Architecture



The following sections provide an overview of the important modules in the MAC.

PSM

The programmable state machine (PSM) is a microcoded engine that provides most of the low-level control to the hardware to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow-control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are collocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, an instruction literal, or a program stack. For ALU operations, the operands are obtained from shared memory, scratch-pad memory, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad memory, or IHRs.

There are two basic branch instructions: conditional branches and ALU-based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs) or on the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as the MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, and WPA2 AES-CCMP.

Based on the frame type and association information, the PSM determines the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the transmit engine (TXE) to encrypt and compute the MIC on transmit frames and the receive engine (RXE) to decrypt and verify the MIC on receive frames. WAPI is also supported.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RX FIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RX FIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple back-off engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The back-off engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the back-off counters. When the back-off counters reach 0, the TXE gets notified so that it may commence frame transmission. In the event of multiple back-off counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power-saving mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires, the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration, ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is a programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

5.2 PHY Description

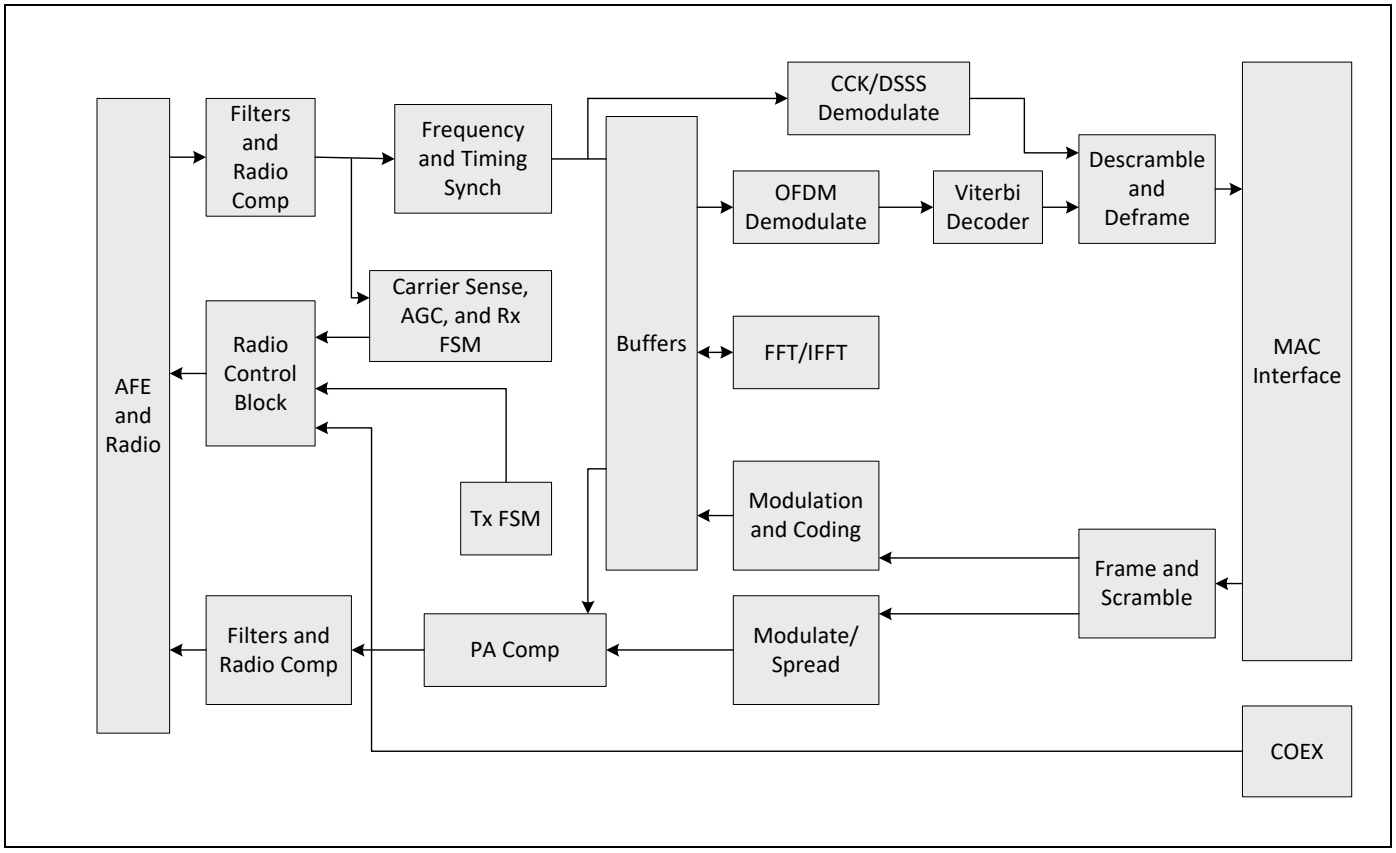
The CYW4343W WLAN digital PHY is designed to comply with IEEE 802.11b/g/n single stream to provide wireless LAN connectivity supporting data rates from 1 Mbps to 96 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to meet specification requirements in the presence of interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, FFT, and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, and channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/IEEE 802.11b hybrid networks with Bluetooth coexistence.

5.2.1 PHY Features

- Supports the IEEE 802.11b/g/n single-stream standards.
- Explicit IEEE 802.11n transmit beamforming.
- Supports optional Greenfield mode in TX and RX.
- Tx and Rx LDPC for improved range and power efficiency.
- Supports IEEE 802.11h/d for worldwide operation.
- Algorithms achieving low power, enhanced sensitivity, range, and reliability.
- Algorithms to maximize throughput performance in the presence of Bluetooth signals.
- Automatic gain control scheme for blocking and nonblocking application scenarios for cellular applications.
- Closed-loop transmit power control.
- Designed to meet FCC and other regulatory requirements.
- Support for 2.4 GHz Cypress TurboQAM data rates and 20 MHz channel bandwidth.

Figure 17. WLAN PHY Block Diagram



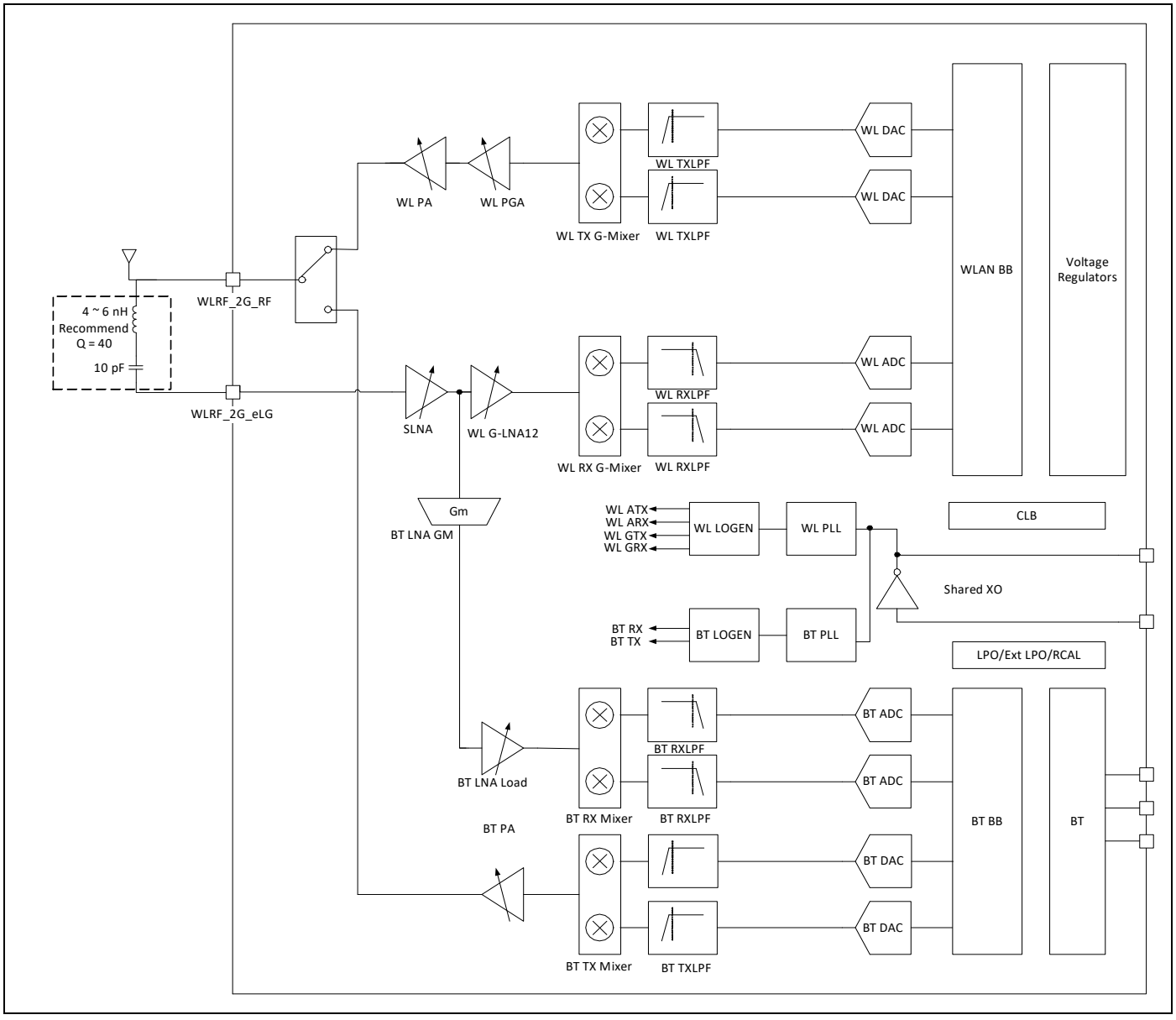
The PHY is capable of fully calibrating the RF front-end to extract the highest performance. On power-up, the PHY performs a full calibration suite to correct for IQ mismatch and local oscillator leakage. The PHY also performs periodic calibration to compensate for any temperature related drift, thus maintaining high-performance over time. A closed-loop transmit control algorithm maintains the output power at its required level and can control TX power on a per-packet basis.

6. WLAN Radio Subsystem

The CYW4343W includes an integrated WLAN RF transceiver that has been optimized for use in 2.4 GHz Wireless LAN systems. It is designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions. Improvements to the radio design include shared TX/RX baseband filters and high immunity to supply noise.

Figure 18 shows the radio functional block diagram.

Figure 18. Radio Functional Block Diagram



6.1 Receive Path

The CYW4343W has a wide dynamic range, direct conversion receiver. It employs high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band.

6.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band. A linear on-chip power amplifier is included, which is capable of delivering high output powers while meeting IEEE 802.11b/g/n specifications without the need for an external PA. This PA is supplied by an internal LDO that is directly supplied by VBAT, thereby eliminating the need for a separate PALDO. Closed-loop output power control is integrated.

6.3 Calibration

The CYW4343W features dynamic on-chip calibration, eliminating process variation across components. This enables the CYW4343W to be used in high-volume applications because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically during normal radio operation. Automatic calibration examples include baseband filter calibration for optimum transmit and receive performance and LOFT calibration for leakage reduction. In addition, I/Q calibration, R calibration, and VCO calibration are performed on-chip.

7. Bluetooth Subsystem Overview

The CYW4343W is a Bluetooth 4.1-compliant, baseband processor and 2.4 GHz transceiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth.

The CYW4343W is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high speed UART and PCM interface for audio. The CYW4343W incorporates all Bluetooth 4.1 features including secure simple pairing, sniff subrating, and encryption pause and resume.

The CYW4343W Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, NFC, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

7.1 Features

Major Bluetooth features of the CYW4343W include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.1 plus enhanced data rate (EDR) features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO)—voice connections
  - Fast connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.1 packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Beacon fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host Controller Power Management)
- Channel-quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

7.2 Bluetooth Radio

The CYW4343W has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

7.2.1 Transmit

The CYW4343W features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path has signal filters, an I/Q upconverter, an output power amplifier, and RF filters. The transmitter path also incorporates π/4–DQPSK for 2 Mbps and 8–DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth Class 1 or Class 2 operation.

7.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4–DQPSK, and 8–DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

7.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

7.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near-thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

7.2.5 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW4343W to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

7.2.6 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

7.2.7 Receiver Signal Strength Indicator

The radio portion of the CYW4343W provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

7.2.8 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW4343W uses an internal RF and IF loop filter.

7.2.9 Calibration

The CYW4343W radio transceiver features an automated calibration scheme that is self contained in the radio. No user interaction is required during normal operation or during manufacturing to optimize performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including filter gain and phase characteristics, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

8. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase the reliability and security of data before sending and receiving it over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

8.1 Bluetooth 4.1 Features

The BBC supports all Bluetooth 4.1 features, with the following benefits:

- Dual-mode classic Bluetooth and classic Low Energy (BT and BLE) operation.
- Low energy physical layer
- Low energy link layer
- Enhancements to HCI for low energy
- Low energy direct test mode
- 128 AES-CCM secure connection for both BT and BLE

Note: The CYW4343W is compatible with the Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

8.2 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer contains the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth link controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff
  - BLE Adv
  - BLE Scan/Initiation

8.3 Test Mode Support

The CYW4343W fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW4343W also supports enhanced testing features to simplify RF debugging and qualification as well as type-approval testing. These features include:

- Fixed frequency carrier-wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to an I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

8.4 Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the CYW4343W are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management

8.4.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

8.4.2 Host Controller Power Management

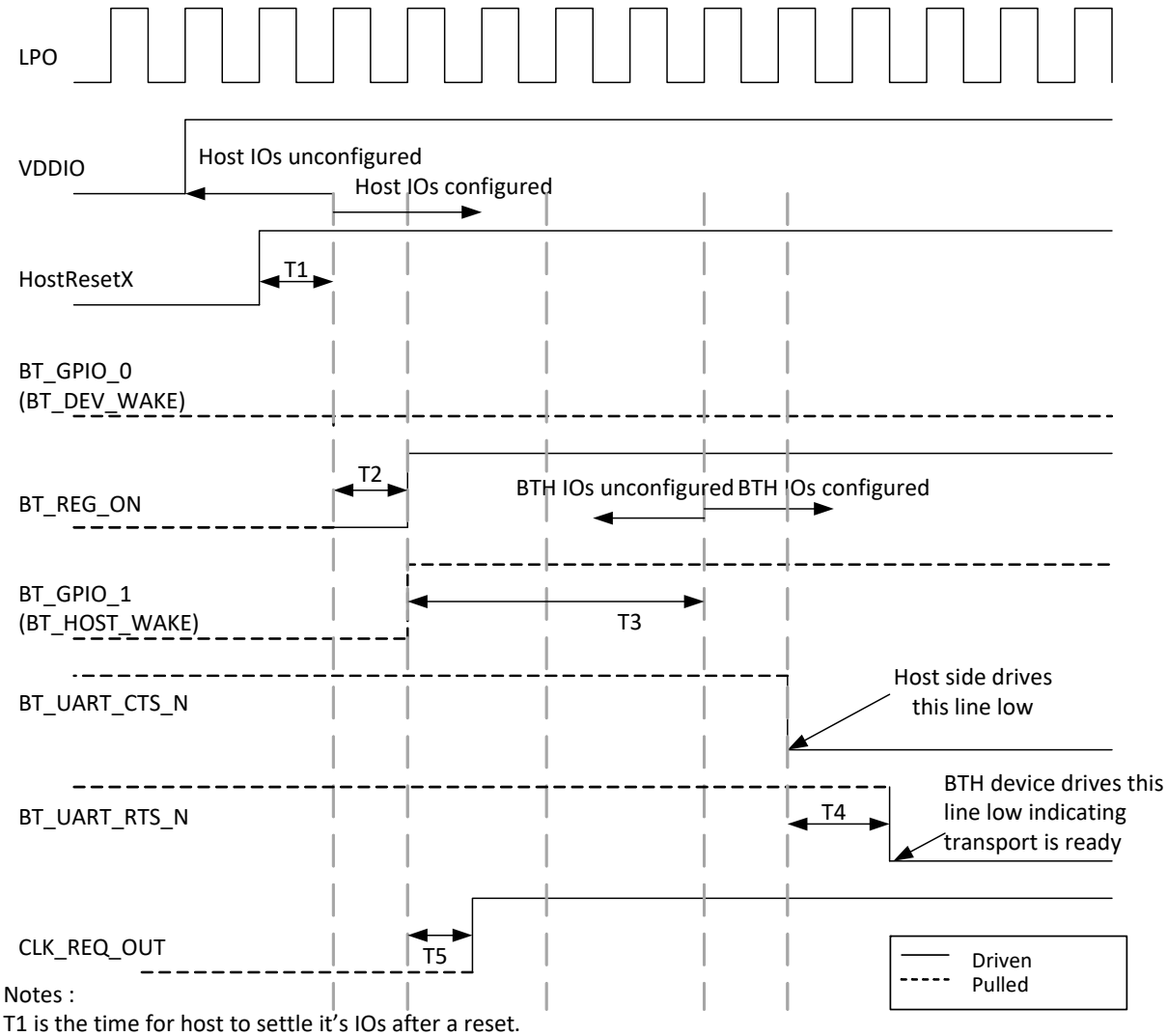
When running in UART mode, the CYW4343W can be configured so that dedicated signals are used for power management handshaking between the CYW4343W and the host. The basic power saving functions supported by those handshaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

Table 8 describes the power-control handshake signals used with the UART interface.

Table 8. Power Control Pin Description

Signal	Type	Description
BT_DEV_WAKE	I	Bluetooth device wake-up signal: Signal from the host to the CYW4343W indicating that the host requires attention. ■ Asserted: The Bluetooth device must wake up or remain awake. ■ Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	O	Host wake-up signal. Signal from the CYW4343W to the host indicating that the CYW4343W requires attention. ■ Asserted: Host device must wake up or remain awake. ■ Deasserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	O	The CYW4343W asserts CLK_REQ when Bluetooth or WLAN directs the host to turn on the reference clock. The CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the CYW4343W powers up or resets when VDDIO is present.
Note: Pad function Control Register is set to 0 for these pins.		

Figure 19. Startup Signaling Sequence



Notes :
T1 is the time for host to settle it's IOs after a reset.
T2 is the time for host to drive BT_REG_ON high after the Host IOs are configured.
T3 is the time for BTH (Bluetooth) device to settle its IOs after a reset and reference clock settling time has elapsed.
T4 is the time for BTH device to drive BT_UART_RTS_N low after the host drives BT_UART_CTS_N low. This assumes the BTH device has already completed initialization.
T5 is the time for BTH device to drive CLK_REQ_OUT high after BT_REG_ON goes high. Note this pin is used for designs that use an external reference clock source from the Host. This pin is irrelevant for Crystal reference clock based designs where the BTH device generates it's own reference clock from an external crystal connected to it's oscillator circuit.
Timing diagram assumes VBAT is present.

8.5 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff and hold. While in these modes, the CYW4343W runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the CYW4343W is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the CYW4343W to effectively be off while keeping the I/O pins powered, so they do not draw extra current from any other I/O-connected devices.

During the low-power shut-down state, provided VDDIO remains applied to the CYW4343W, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on digital signals in the system and enables the CYW4343W to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

Two CYW4343W input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the CYW4343W is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

8.5.1 Wideband Speech

The CYW4343W provides support for wideband speech (WBS) technology. The CYW4343W can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

8.6 Packet Loss Concealment

Packet Loss Concealment (PLC) improves the apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The CYW4343W uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 20 and Figure 21 show audio waveforms with and without Packet Loss Concealment. Cypress PLC/BEC algorithms also support wideband speech.

Figure 20. CVSD Decoder Output Waveform Without PLC

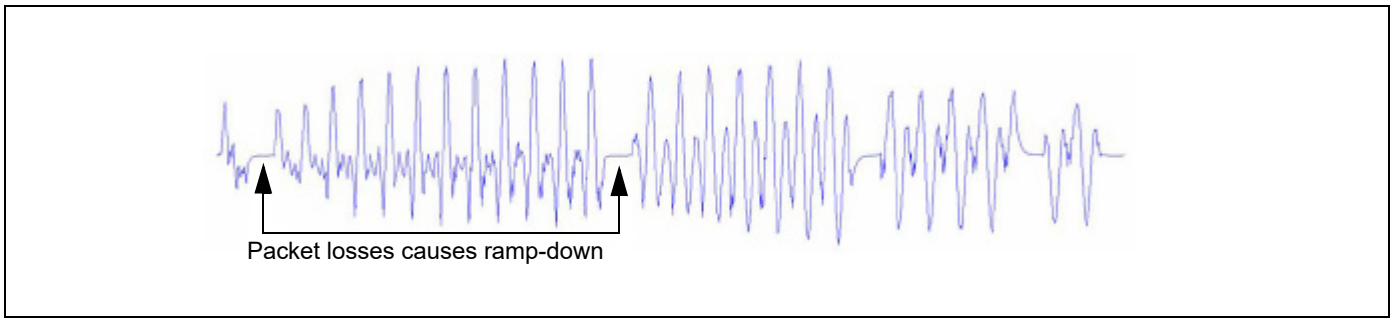
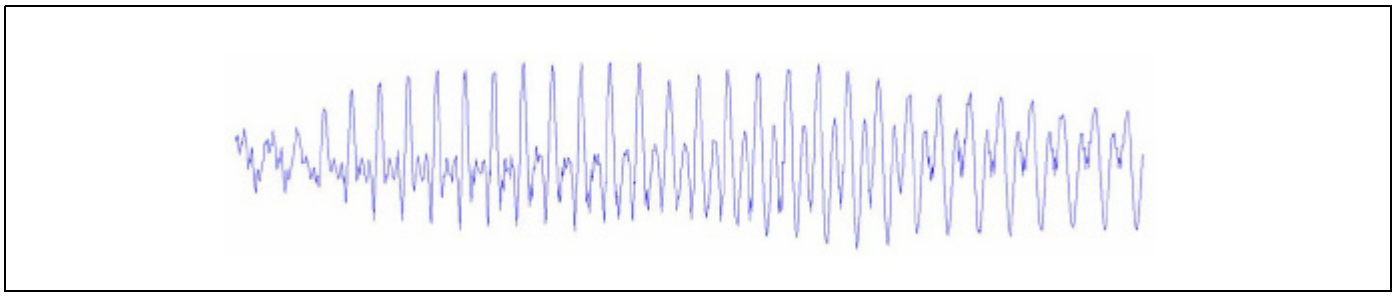


Figure 21. CVSD Decoder Output Waveform After Applying PLC



8.6.1 Codec Encoding

The CYW4343W can support SBC and mSBC encoding and decoding for wideband speech.

8.6.2 Multiple Simultaneous A2DP Audio Streams

The CYW4343W has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

8.7 Adaptive Frequency Hopping

The CYW4343W gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

8.8 Advanced Bluetooth/WLAN Coexistence

The CYW4343W includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The CYW4343W radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The CYW4343W integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The CYW4343W also supports Transmit Power Control (TPC) on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core’s channel information.

8.9 Fast Connection (Interlaced Page and Inquiry Scans)

The CYW4343W supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

9. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 576 KB of ROM for program storage and boot ROM, and 160 KB of RAM for data scratch-pad and patch RAM code. The internal ROM allows for flexibility during power-on reset (POR) to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or feature additions. These patches may be downloaded from the host to the CYW4343W through the UART transports.

9.1 RAM, ROM, and Patch Memory

The CYW4343W Bluetooth core has 160 KB of internal RAM which is mapped between general purpose scratch-pad memory and patch memory, and 576 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory is used for bug fixes and feature additions to ROM memory code.

9.2 Reset

The CYW4343W has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT POR circuit is out of reset after BT_REG_ON goes high. If BT_REG_ON is low, then the POR circuit is held in reset.

10. Bluetooth Peripheral Transport Unit

10.1 PCM Interface

The CYW4343W supports two independent PCM interfaces that share pins with the I^2S interfaces. The PCM interface on the CYW4343W can connect to linear PCM codec devices in master or slave mode. In master mode, the CYW4343W generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW4343W. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

10.1.1 Slot Mapping

The CYW4343W supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rates is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

10.1.2 Frame Synchronization

The CYW4343W supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

10.1.3 Data Formatting

The CYW4343W may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW4343W uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0's, 1's, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

10.1.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate. The CYW4343W also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 kbps rate) is transferred over the PCM bus.

10.1.5 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 22. PCM Timing Diagram (Short Frame Sync, Master Mode)

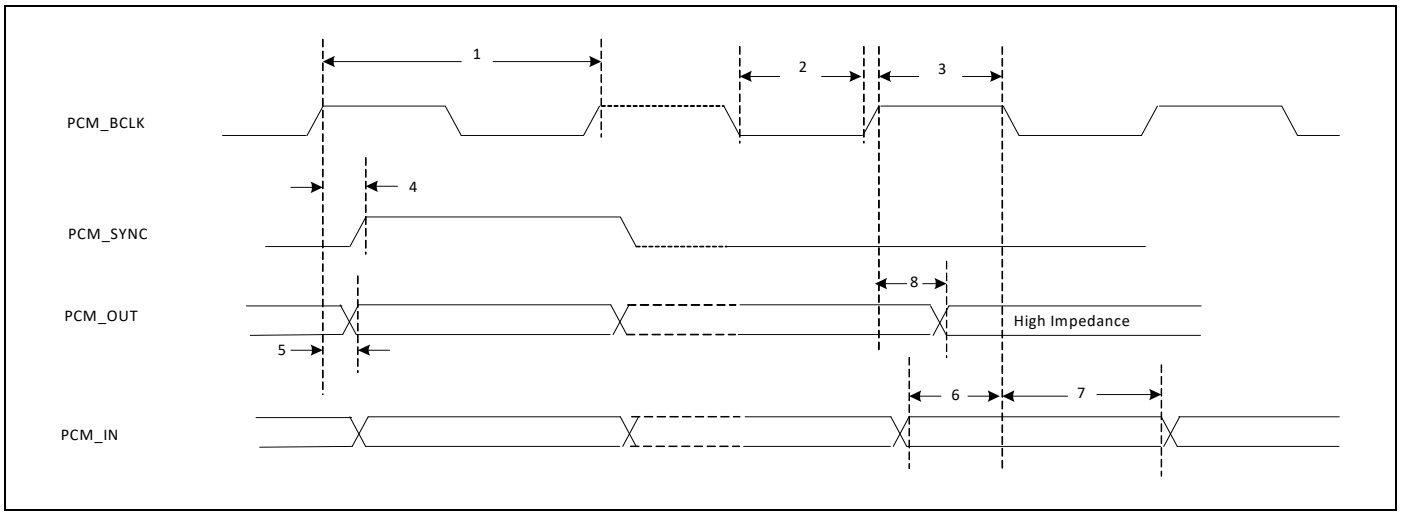


Table 9. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

Figure 23. PCM Timing Diagram (Short Frame Sync, Slave Mode)

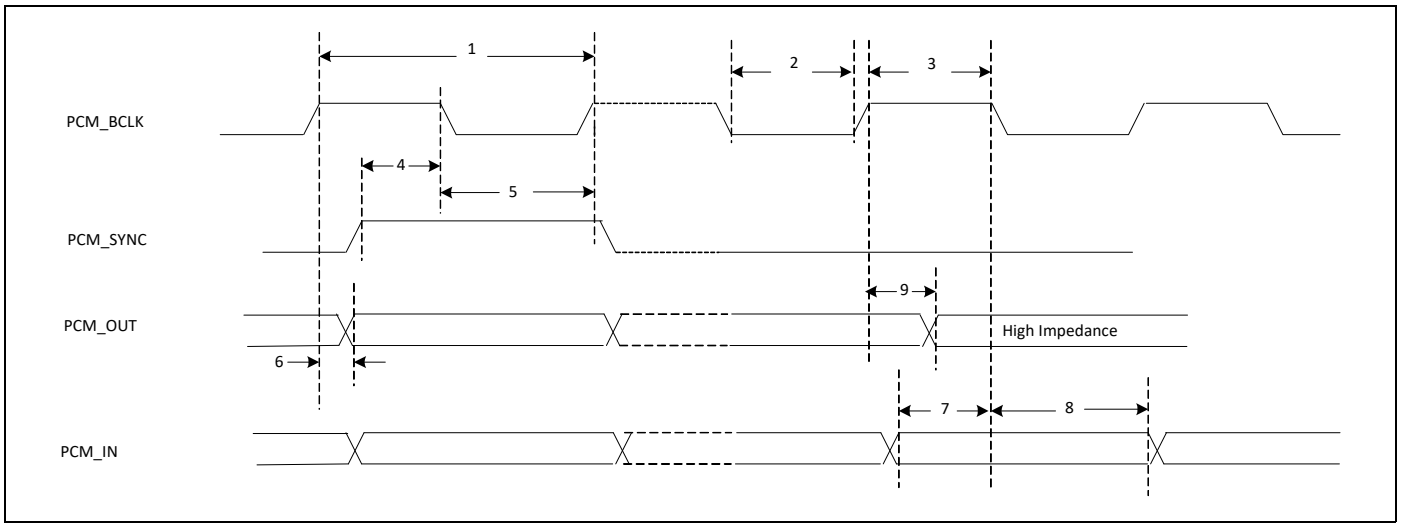


Table 10. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

Figure 24. PCM Timing Diagram (Long Frame Sync, Master Mode)

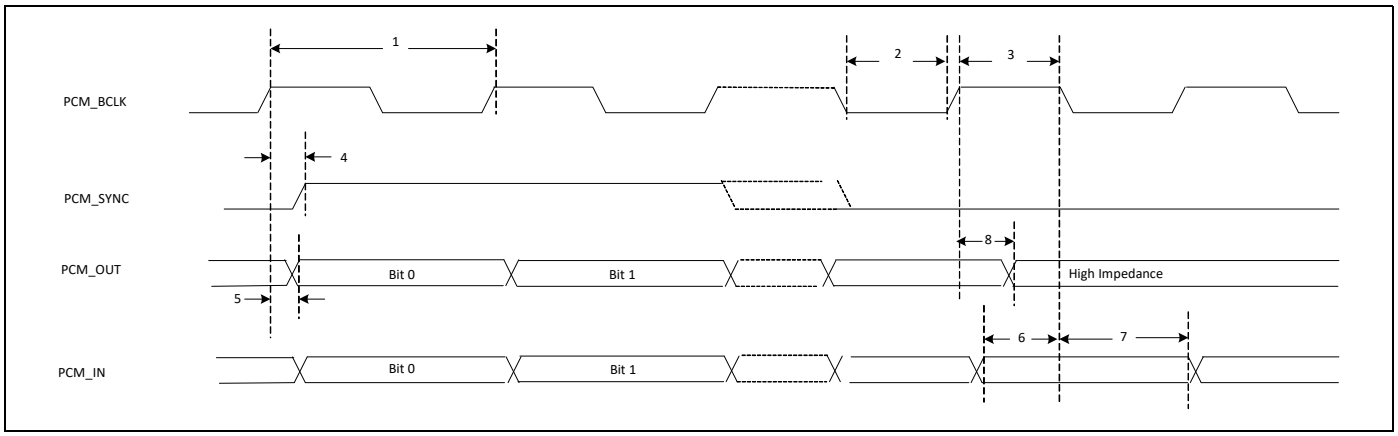


Table 11. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

Figure 25. PCM Timing Diagram (Long Frame Sync, Slave Mode)

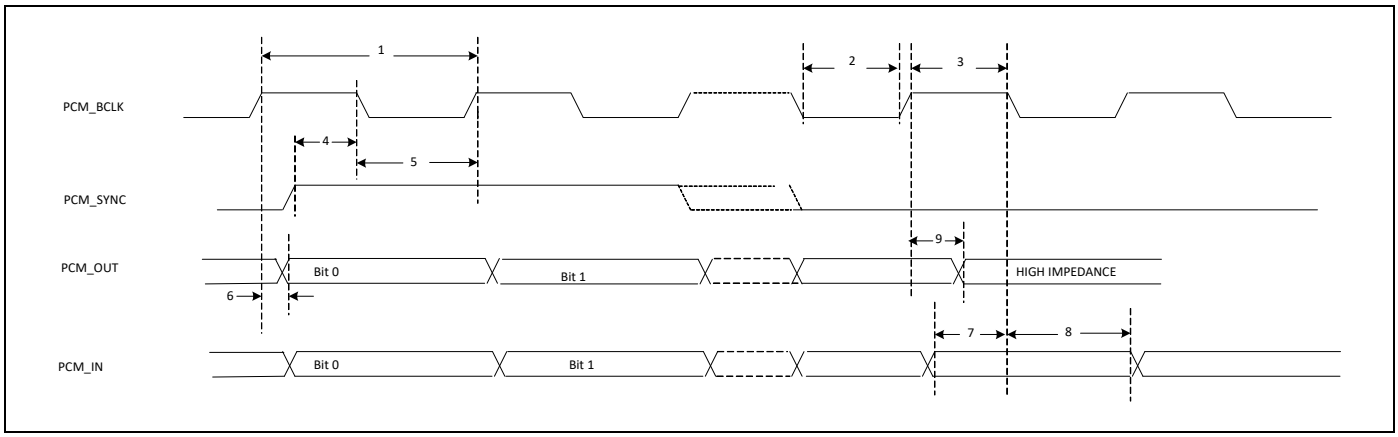


Table 12. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

10.2 UART Interface

The CYW4343W uses UART for Bluetooth HCI. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the Advanced High Performance Bus (AHB) interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4 and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport as described in the Bluetooth specification (*Three-wire UART Transport Layer*). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The CYW4343W UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform a wake-on activity function. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW4343W UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2% (see Table 13).

Table 13. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART timing is defined in Figure 26 and Table 14.

Figure 26. UART Timing

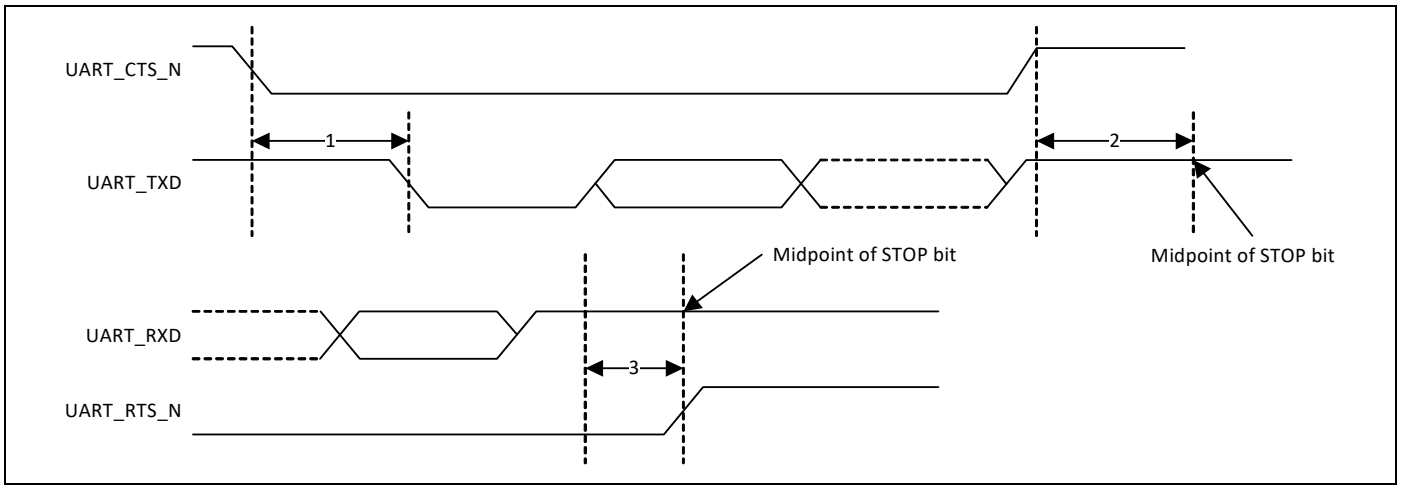


Table 14. UART Timing Specifications

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

10.3 I²S Interface

The CYW4343W supports an independent I²S digital audio port for high-fidelity Bluetooth audio. The I²S interface supports both master and slave modes. The I²S signals are:

- I²S Clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO is always an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit-clock cycle after the I²S WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW4343W are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using an N/M clock divider.

In slave mode, clock rates up to 3.072 MHz are supported.

10.3.1 I^2S Timing

Note: Timing values specified in Table 15 are relative to high and low threshold levels

Table 15. Timing for I^2S Transmitters and Receivers

	Transmitter				Receiver				Notes
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock period T	T_{tr}	–	–	–	T_r	–	–	–	1
Master mode: Clock generated by transmitter or receiver.									
High t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Low t_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Slave mode: Clock accepted by transmitter or receiver.									
High t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Low t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–	–	–	4
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	5
Hold time t_{htr}	0	–	–	–	–	–	–	–	4
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	6
Hold time t_{hr}	–	–	–	–	–	0	–	–	6

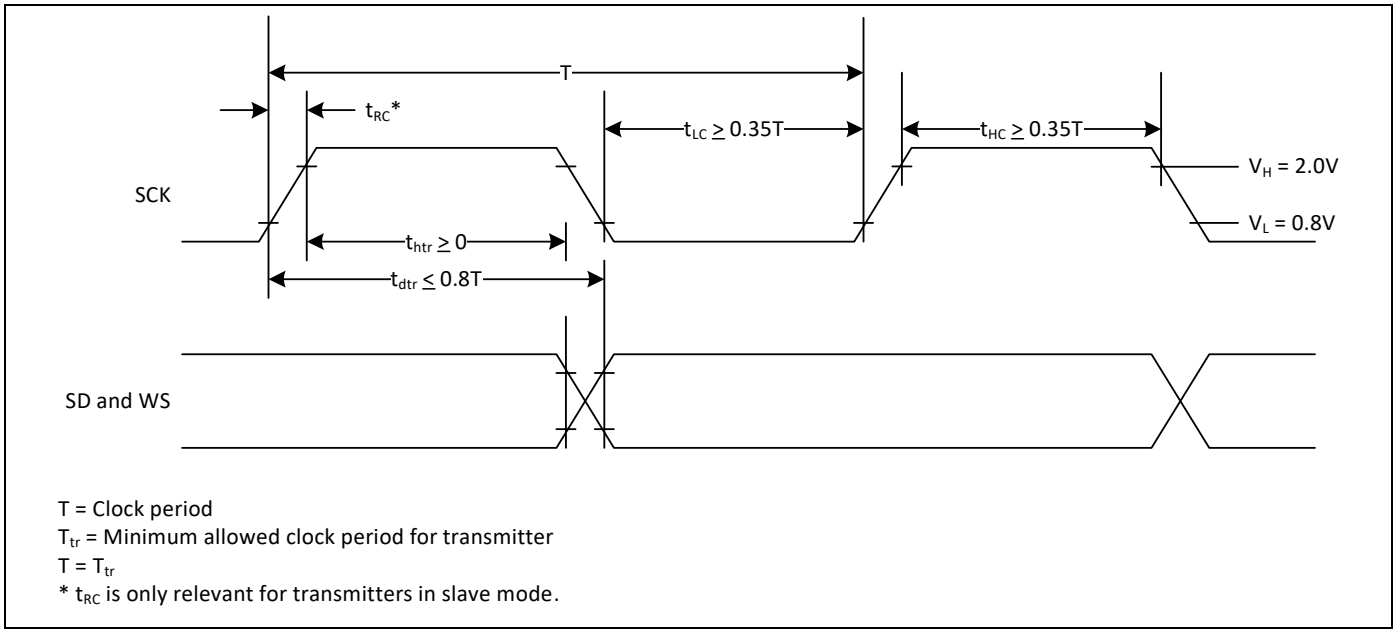
Note:

- The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
- At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
- In slave mode, the transmitter and receiver need a clock signal with minimum high and low periods so that they can detect the signal. As long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
- Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC}, which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, as long as the clock rise-time, t_{RC}, does not exceed t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
- To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.

The data setup and hold time must not be less than the specified receiver setup and hold time.

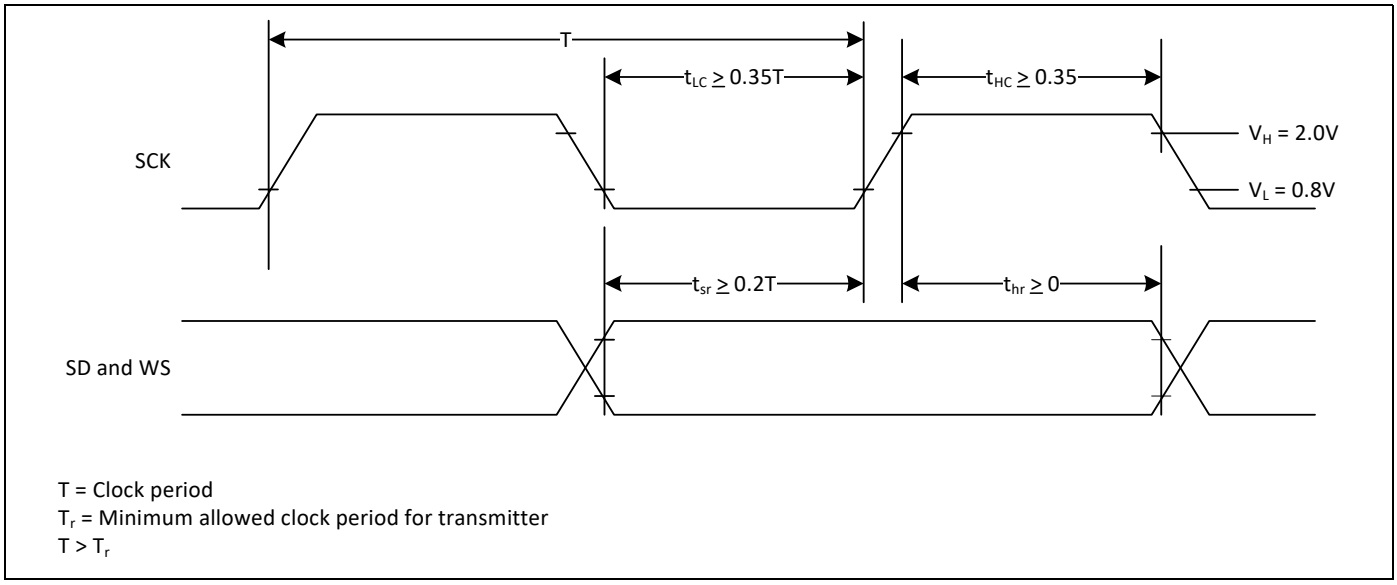
Note: The time periods specified in Figure 27 and Figure 28 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 27. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 28. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

11. CPU and Global Functions

11.1 WLAN CPU and Memory Subsystem

The CYW4343W includes an integrated ARM Cortex-M3 processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debugging. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for the Thumb-2 instruction set. ARM Cortex-M3 provides a 30% performance gain over ARM7TDMI.

At 0.19 µW/MHz, the Cortex-M3 is the most power efficient general purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for code and data access (ICode/DCode and system buses). ARM Cortex-M3 supports extensive debug features including real-time tracing of program execution.

On-chip memory for the CPU includes 512 KB SRAM and 640 KB ROM.

11.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 4096-bit One-Time Programmable (OTP) memory, which is read by system software after a device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address, can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP memory programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package. Documentation on the OTP development process is available on the Cypress customer support portal (www.cypress.com/support).

11.3 GPIO Interface

Five general purpose I/O (GPIO) pins are available on the CYW4343W that can be used to connect to various external devices.

GPIOs are tristated by default. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. They can also be programmed to have internal pull-up or pull-down resistors.

GPIO_0 is normally used as a WL_HOST_WAKE signal.

The CYW4343W supports 2-wire, 3-wire, and 4-wire coexistence configurations using GPIO_1 through GPIO_4. The signal functions of GPIO_1 through GPIO_4 are programmable to support the three coexistence configurations.

11.4 External Coexistence Interface

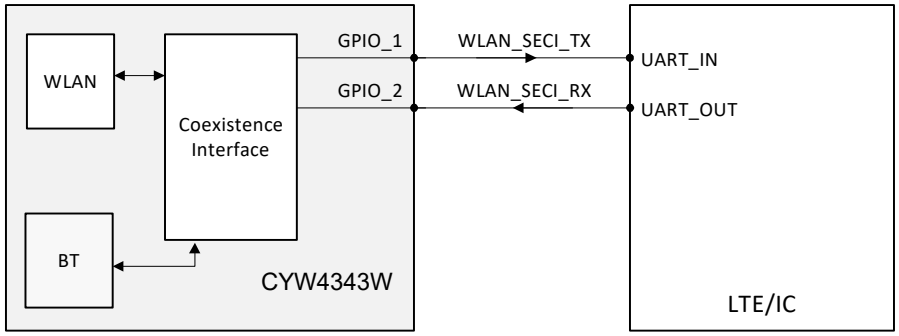
The CYW4343W supports 2-wire, 3-wire, and 4-wire coexistence interfaces to enable signaling between the device and an external colocated wireless device in order to manage wireless medium sharing for optimal performance. The external colocated device can be any of the following ICs: GPS, WiMAX, LTE, or UWB. An LTE IC is used in this section for illustration.

11.4.1 2-Wire Coexistence

Figure 29 shows a 2-wire LTE coexistence example. The following definitions apply to the GPIOs in the figure:

- GPIO_1: WLAN_SECI_TX output to an LTE IC.
- GPIO_2: WLAN_SECI_RX input from an LTE IC.

Figure 29. 2-Wire Coexistence Interface to an LTE IC



Notes:
- NOR ing to generate ISM_RX_PRIORITY for ERCX_TXCONF or BT_RX_PRIORITY is achieved by setting the GPIO mask registers appropriately.
- WLAN_SECI_OUT and WLAN_SECI_IN are multiplexed on the GPIOs.

See Figure 26 and Table 14 for UART timing.

11.4.2 3-Wire and 4-Wire Coexistence Interfaces

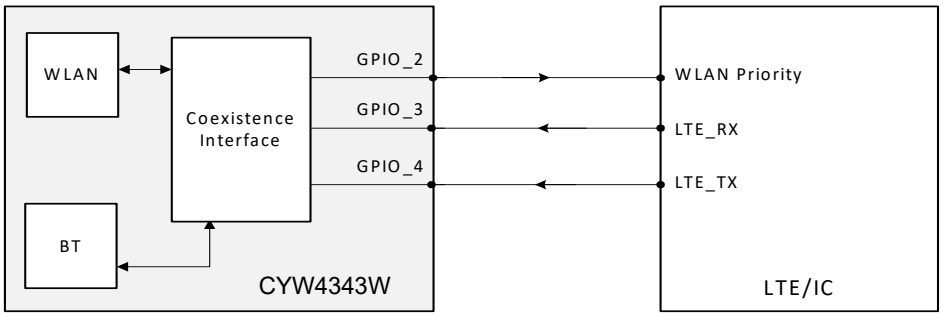
Figure 30 and Figure 31 show 3-wire and 4-wire LTE coexistence examples, respectively. The following definitions apply to the GPIOs in the figures:

- For the 3-wire coexistence interface:
- GPIO_2: WLAN priority output to an LTE IC.
- GPIO_3: LTE_RX input from an LTE IC.
- GPIO_4: LTE_TX input from an LTE IC.

For the 4-wire coexistence interface:

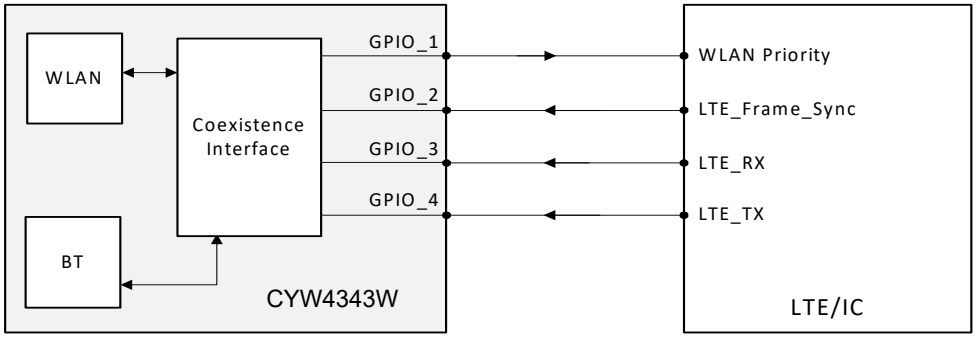
- GPIO_1: WLAN priority output to an LTE IC.
- GPIO_2: LTE frame sync input from an LTE IC. This GPIO applies only to the 4-wire coexistence interface.
- GPIO_3: LTE_RX input from an LTE IC.
- GPIO_4: LTE_TX input from an LTE IC.

Figure 30. 3-Wire Coexistence Interface to an LTE IC



Note: OR ing to generate WCN_PRIORITY for ERCX_TXCONF or BT_RX_PRIORITY is achieved by setting the GPIO mask registers appropriately.

Figure 31. 4-Wire Coexistence Interface to an LTE IC



Note: OR ing to generate WCN_PRIORITY for ERCX_TXCONF or BT_RX_PRIORITY is achieved by setting the GPIO mask registers appropriately.

11.5 JTAG Interface

The CYW4343W supports the IEEE 1149.1 JTAG boundary scan standard over SDIO for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Cypress to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

11.6 UART Interface

One UART interface can be enabled by software as an alternate function on the JTAG pins. UART_RX is available on the JTAG_TDI pin, and UART_TX is available on the JTAG_TDO pin.

The UART is primarily for debugging during development. By adding an external RS-232 transceiver, this UART enables the CYW4343W to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and it provides a FIFO size of 64 × 8 in each direction.

12. WLAN Software Architecture

12.1 Host Software Architecture

The host driver (DHD) provides a transparent connection between the host operating system and the CYW4343W media (for example, WLAN) by presenting a network driver interface to the host operating system and communicating with the CYW4343W over a SDIO interface-specific bus to:

- Forward transmit and receive frames between the host network stack and the CYW4343W device.
- Pass control requests from the host to the CYW4343W device, returning the CYW4343W device responses.

The driver communicates with the CYW4343W over the bus using a control channel and a data channel to pass control messages and data messages. The actual message format is based on the BDC protocol.

12.2 Device Software Architecture

The wireless device, protocol, and bus drivers are run on the embedded ARM processor using a Cypress defined operating system called HNDRTE, which transfers data over a propriety Cypress format over the SDIO interface between the host and device (BDC/LMAC). The data portion of the format consists of IEEE 802.11 frames wrapped in a Cypress encapsulation. The host architecture provides all missing functionality between a network device and the Cypress device interface. The host can also be customized to provide functionality between the Cypress device interface and a full network device interface.

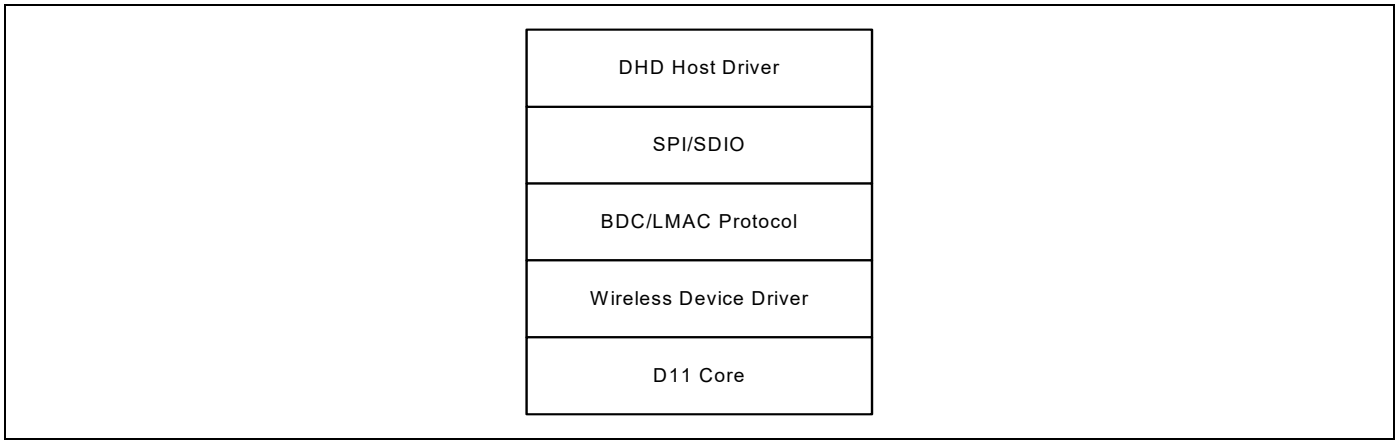
This transfer requires a message-oriented (framed) interconnect between the host and device. The SDIO bus is an addressed bus—each host-initiated bus operation contains an explicit device target address—and does not natively support a higher-level data frame concept. Cypress has implemented a hardware/software message encapsulation scheme that ignores the bus operation code address and prefixes each frame with a 4-byte length tag for framing. The device presents a packet-level interface over which data, control, and asynchronous event (from the device) packets are supported.

The data and control packets received from the bus are initially processed by the bus driver and then passed on to the protocol driver. If the packets are data packets, they are transferred to the wireless device driver (and out through its medium), and a data packet received from the device medium follows the same path in the reverse direction. If the packets are control packets, the protocol header is decoded by the protocol driver. If the packets are wireless IOCTL packets, the IOCTL API of the wireless driver is called to configure the wireless device. The microcode running in the D11 core processes all time-critical tasks.

12.3 Remote Downloader

When the CYW4343W powers up, the DHD initializes and downloads the firmware to run in the device.

Figure 32. WLAN Software Architecture



12.4 Wireless Configuration Utility

The device driver that supports the IEEE 802.11 family of wireless solutions provides an input/output control (IOCTL) interface for making advanced configuration settings. The IOCTL interface makes it possible to make settings that are normally not possible when using just the native operating system-specific IEEE 802.11 configuration mechanisms. The utility uses IOCTLs to query or set a number of different driver/chip operating properties.

13. Pinout and Signal Descriptions

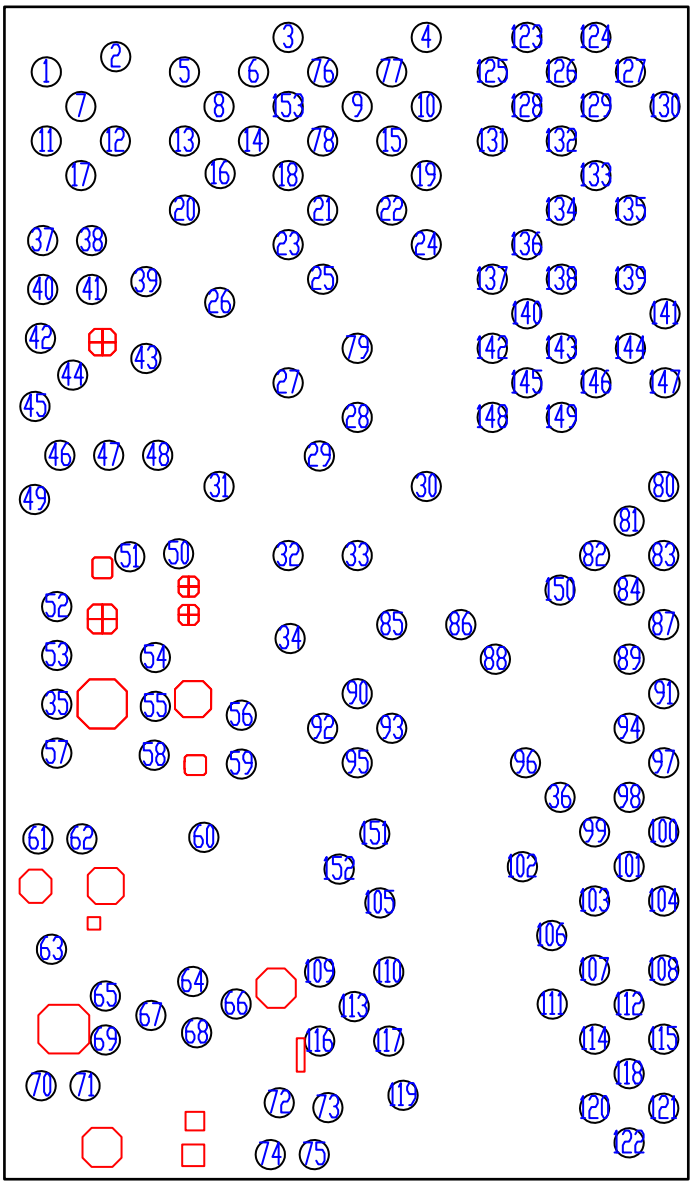
13.1 Ball Map

Figure 33 shows the 74-ball WLBGA ball map. Figure 34 shows the 153-bump WLCSP.

Figure 33. 74-Ball WLBGA Ball Map (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	
1	BT_UART_RXD	BT_DEV_WAKE	BT_HOST_WAKE		FM_RF_IN	BT_VCO_VDD	BT_IF_VDD	BT_PAVDD	WLRF_2G_eLG	WLRF_2G_RF		WLRF_PA_VDD	1
2	BT_UART_TXD	BT_UART_CTS_N	FM_OUT1	FM_OUT2	FM_RF_VDD	BTFM_PLL_VDD	BTFM_PLL_VSS	BT_IF_VSS	WLRF_LNA_GND	WLRF_GENERAL_GND	WLRF_PA_GND	WLRF_VDD_1P35	2
3	BT_I2S_WS	BT_I2S_DO	BT_UART_RTS_N	VDDC	FM_RF_VSS			BT_VCO_VSS	WLRF_GPIO		WLRF_VCO_GND	WLRF_XTAL_VDD1P2	3
4	BT_I2S_CLK	BT_PCM_OUT	BT_PCM_IN	VSSC		BT_GPIO_3	VDDC	WLRF_AFE_GND		GPIO_3	WLRF_XTAL_GND	WLRF_XTAL_XOP	4
5	BT_PCM_CLK	BT_PCM_SYNC	SYS_VDDIO	WPT_1P8	WPT_3P3	LPO_IN	BT_GPIO_4	BT_GPIO_5	VSSC	GPIO_4	GPIO_2	WLRF_XTAL_XON	5
6	SR_VLX	PMU_AVSS	VOUT_CLDO	VOUT_LNLDO	BT_REG_ON	WCC_VDDIO	WL_REG_ON	GPIO_1	GPIO_0	SDIO_DATA_0	SDIO_CMD	CLK_REQ	6
7	SR_PVSS	SR_VDDBAT5V	LDO_VDD1P5		VOUT_3P3	LDO_VDDBAT5V		SDIO_DATA_1	SDIO_DATA_3		SDIO_DATA_2	SDIO_CLK	7
	A	B	C	D	E	F	G	H	J	K	L	M	

Figure 34. 153-Bump WLCSP (Top View)



13.2 WLBGA Ball List in Ball Number Order with X-Y Coordinates

Table 16 provides ball numbers and names in ball number order. The table includes the X and Y coordinates for a top view with a (0,0) center.

Table 16. CYW4343W WLBGA Ball List — Ordered By Ball Number

Ball Number	Ball Name	X Coordinate	Y Coordinate
A1	BT_UART_RXD	–1200.006	2199.996
A2	BT_UART_TXD	–799.992	2199.996
A3	BT_I2S_WS or BT_PCM_SYNC	–399.996	2199.996
A4	BT_I2S_CLK or BT_PCM_CLK	0	2199.996
A5	BT_PCM_CLK or BT_I2S_CLK	399.996	2199.996
A6	SR_VLX	799.992	2199.978
A7	SR_PVSS	1199.988	2199.978
B1	BT_DEV_WAKE	–1200.006	1800
B2	BT_UART_CTS_N	–799.992	1800
B3	BT_I2S_DO or BT_PCM_OUT	–399.996	1800
B4	BT_PCM_OUT or BT_I2S_DO	0	1800
B5	BT_PCM_SYNC or BT_I2S_WS	399.996	1800
B6	PMU_AVSS	799.992	1799.982
B7	SR_VBAT5V	1199.988	1799.982
C1	BT_HOST_WAKE	–1200.006	1399.995
C2	FM_OUT1	–799.992	1399.986
C3	BT_UART_RTS_N	–399.996	1399.995
C4	BT_PCM_IN or BT_I2S_DI	0	1399.995
C5	SYS_VDDIO	399.996	1399.986
C6	VOUT_CLDO	799.992	1399.986
C7	LDO_VDD15V	1199.988	1399.986
D2	FM_OUT2	–799.992	999.99
D3	VDDC	–399.996	999.999
D4	VSSC	0	999.999
D5	WPT_1P8	399.996	999.99
D6	VOUT_LNLDO	799.992	999.99
E1	FM_RF_IN	–1199.988	599.994
E2	FM_RF_VDD	–799.992	599.994
E3	FM_RF_VSS	–399.996	599.994
E5	WPT_3P3	399.996	599.994
E6	BT_REG_ON	799.992	599.994
E7	VOUT_3P3	1199.988	599.994
F1	BT_VCO_VDD	–1199.988	199.998
F2	BTFM_PLL_VDD	–799.992	199.998
F4	BT_GPIO_3	0	199.998
F5	LPO_IN	399.996	199.998

Table 16. CYW4343W WLBGA Ball List — Ordered By Ball Number (Cont.)

Ball Number	Ball Name	X Coordinate	Y Coordinate
F6	WCC_VDDIO	800.001	199.998
F7	LDO_VBAT5V	1199.988	199.998
G1	BT_IF_VDD	–1199.988	–199.998
G2	BTFM_PLL_VSS	–799.992	–199.998
G4	VDDC	0	–199.998
G5	BT_GPIO_4	399.996	–199.998
G6	WL_REG_ON	800.001	–199.998
H1	BT_PAVDD	–1199.988	–599.994
H2	BT_IF_VSS	–799.992	–599.994
H3	BT_VCO_VSS	–399.996	–599.994
H4	WLRF_AFE_GND	0	–599.994
H5	BT_GPIO_5	399.996	–599.994
H6	GPIO_1	800.001	–599.994
H7	SDIO_DATA_1	1200.006	–599.994
J1	WLRF_2G_eLG	–1199.988	–999.99
J2	WLRF_LNA_GND	–799.992	–999.99
J3	WLRF_GPIO	–399.996	–999.99
J5	VSSC	399.996	–999.999
J6	GPIO_0	800.001	–999.999
J7	SDIO_DATA_3	1200.006	–999.999
K1	WLRF_2G_RF	–1199.988	–1399.986
K2	WLRF_GENERAL_GND	–799.992	–1399.986
K4	GPIO_3	0	–1399.995
K5	GPIO_4	399.996	–1399.995
K6	SDIO_DATA_0	800.001	–1399.995
L2	WLRF_PA_GND	–799.992	–1799.982
L3	WLRF_VCO_GND	–399.996	–1799.982
L4	WLRF_XTAL_GND	0	–1799.982
L5	GPIO_2	399.996	–1799.991
L6	SDIO_CMD	800.001	–1799.991
L7	SDIO_DATA_2	1200.006	–1799.991
M1	WLRF_PA_VDD	–1199.988	–2199.978
M2	WLRF_VDD_1P35	–799.992	–2199.978
M3	WLRF_XTAL_VDD1P2	–399.996	–2199.978
M4	WLRF_XTAL_XOP	0	–2199.978
M5	WLRF_XTAL_XON	399.996	–2199.978
M6	CLK_REQ	800.001	–2199.996
M7	SDIO_CLK	1200.006	–2199.996

13.3 WLCSP Bump List in Bump Order with X-Y Coordinates

Table 17. CYW4343W WLCSP Bump List — Ordered By Bump Number

Bump Number	Bump Name	Bump View (0,0 Center of Die)		Top View (0,0 Center of Die)	
		X Coordinate	Y Coordinate	X Coordinate	Y Coordinate
1	BT_UART_RXD	1228.248	2133.594	–1228.248	2133.594
2	BT_VDDC_ISO_2	944.082	2195.919	–944.082	2195.919
3	BT_PCM_CLK or BT_I2S_CLK	238.266	2275.020	–238.266	2275.020
4	BT_TM1	–327.438	2275.020	327.438	2275.020
5	BT_GPIO_3	662.544	2133.594	–662.544	2133.594
6	BT_DEV_WAKE	379.692	2133.594	–379.692	2133.594
7	BT_UART_RTS_N	1086.822	1992.168	–1086.822	1992.168
8	BT_GPIO_4	521.118	1992.168	–521.118	1992.168
9	BT_VDDC_ISO_1	–44.586	1992.168	44.586	1992.168
10	BT_GPIO_5	–327.438	1992.168	327.438	1992.168
11	BT_HOST_WAKE	1228.248	1850.742	–1228.248	1850.742
12	BT_UART_TXD	945.396	1850.742	–945.396	1850.742
13	BT_GPIO_2	662.544	1850.742	–662.544	1850.742
14	BT_VDDC	379.692	1850.742	–379.692	1850.742
15	BT_I2S_CLK or BT_PCM_CLK	–186.012	1850.742	186.012	1850.742
16	BT_VDDC	516.501	1717.578	–516.501	1717.578
17	BT_PCM_SYNC or BT_I2S_WS	1086.822	1709.316	–1086.822	1709.316
18	BT_I2S_WS or BT_PCM_SYNC	238.266	1709.316	–238.266	1709.316
19	BT_PCM_OUT or BT_I2S_DO	–327.438	1709.316	327.438	1709.316
20	BT_PCM_IN or BT_I2S_DI	662.544	1567.890	–662.544	1567.890
21	VSSC	96.840	1567.890	–96.840	1567.890
22	BT_UART_CTS_N	–186.012	1567.890	186.012	1567.890
23	BT_I2S_DI or BT_PCM_IN	238.266	1426.464	–238.266	1426.464
24	BT_I2S_DO or BT_PCM_OUT	–327.438	1426.464	327.438	1426.464
25	VSSC	96.840	1285.038	–96.840	1285.038
26	BT_VDDC	518.391	1189.863	–518.391	1189.863
27	VSSC	238.266	860.760	–238.266	860.760
28	BT_VDDC	–44.586	719.334	44.586	719.334
29	VSSC	110.286	561.303	–110.286	561.303
30	VSSC	–327.438	436.482	327.438	436.482
31	BT_VDDC	521.118	436.473	–521.118	436.473
32	VSSC	238.266	153.630	–238.266	153.630
33	VSSC	–44.586	153.630	44.586	153.630
34	BT_VDDC	229.986	–185.976	–229.986	–185.976
35	BT_PAVSS	1185.471	–455.270	–1185.471	–455.270
36	VSSC	–875.142	–836.352	875.142	–836.352

Table 17. CYW4343W WLCSP Bump List — Ordered By Bump Number (Cont.)

Bump Number	Bump Name	Bump View (0,0 Center of Die)		Top View (0,0 Center of Die)	
		X Coordinate	Y Coordinate	X Coordinate	Y Coordinate
37	FM_DAC_VOUT1	1243.031	1443.096	–1243.031	1443.096
38	FM_DAC_AVSS	1043.033	1443.096	–1043.033	1443.096
39	FM_PLLAVSS	820.485	1275.098	–820.485	1275.098
40	FM_DAC_VOUT2	1243.031	1243.098	–1243.031	1243.098
41	FM_DAC_AVDD	1043.033	1243.098	–1043.033	1243.098
42	FM_VCOVSS	1252.220	1043.100	–1252.220	1043.100
43	FM_PLLDVDD1P2	820.485	960.593	–820.485	960.593
44	FM_VCOVDD1P2	1120.383	892.373	–1120.383	892.373
45	FM_RFVDD1P2	1274.787	764.213	–1274.787	764.213
46	FM_RFVSS	1172.988	563.990	–1172.988	563.990
47	FM_IFVSS	972.990	563.990	–972.990	563.990
48	FM_IFDVDD1P2	772.304	563.990	–772.304	563.990
49	FM_RFINMAIN	1276.551	383.225	–1276.551	383.225
50	BT_DVSS	686.628	160.911	–686.628	160.911
51	BT_IFVDD1P2	886.626	148.775	–886.626	148.775
52	BT_AGPIO	1185.471	–55.274	–1185.471	–55.274
53	BT_PAVDD2P5	1185.462	–255.272	–1185.462	–255.272
54	BT_LNAVDD1P2	781.893	–263.768	–781.893	–263.768
55	BT_LNAVSS	781.893	–463.766	–781.893	–463.766
56	BT_PLLVSS	429.885	–499.995	–429.885	–499.995
57	BT_VCOVDD1P2	1185.471	–655.268	–1185.471	–655.268
58	BT_VCOVSS	786.393	–663.764	–786.393	–663.764
59	BT_PLLVDD1P2	429.885	–699.993	–429.885	–699.993
60	WRF_AFE_GND	583.250	–999.990	–583.250	–999.990
61	WRF_RFIN_ELG_2G	1262.642	–1006.290	–1262.642	–1006.290
62	WRF_RX2G_GND	1082.642	–1006.290	–1082.642	–1006.290
63	WRF_RFIO_2G	1206.990	–1458.198	–1206.990	–1458.198
64	WRF_GENERAL_GND	628.713	–1590.210	–628.713	–1590.210
65	WRF_PA_GND3P3	986.531	–1649.615	–986.531	–1649.615
66	WRF_VCO_GND	451.188	–1682.370	–451.188	–1682.370
67	WRF_GPAIO_OUT	799.992	–1729.224	–799.992	–1729.224
68	WRF_PMU_VDD1P35	612.878	–1800.135	–612.878	–1800.135
69	WRF_PA_GND3P3	986.531	–1829.615	–986.531	–1829.615
70	WRF_PA_VDD3P3	1249.686	–2016.945	–1249.686	–2016.945
71	WRF_PA_VDD3P3	1069.686	–2016.945	–1069.686	–2016.945
72	WRF_XTAL_GND1P2	274.613	–2086.677	–274.613	–2086.677
73	WRF_XTAL_VDD1P2	75.519	–2106.621	–75.519	–2106.621
74	WRF_XTAL_XOP	311.126	–2298.978	–311.126	–2298.978

Table 17. CYW4343W WLCSP Bump List — Ordered By Bump Number (Cont.)

Bump Number	Bump Name	Bump View (0,0 Center of Die)		Top View (0,0 Center of Die)	
		X Coordinate	Y Coordinate	X Coordinate	Y Coordinate
75	WRF_XTAL_XON	131.126	–2298.978	–131.126	–2298.978
76	LPO_IN	96.840	2133.594	–96.840	2133.594
77	WCC_VDDIO	–186.012	2133.594	186.012	2133.594
78	VSSC	96.813	1850.742	–96.813	1850.742
79	WCC_VDDIO	–44.586	1002.186	44.586	1002.186
80	GPIO_12	–1299.420	436.482	1299.420	436.482
81	GPIO_11	–1157.994	295.056	1157.994	295.056
82	GPIO_9	–1016.568	153.630	1016.568	153.630
83	GPIO_10	–1299.420	153.630	1299.420	153.630
84	GPIO_8	–1157.994	12.204	1157.994	12.204
85	VSSC	–186.012	–129.222	186.012	–129.222
86	VDDC	–468.864	–129.222	468.864	–129.222
87	GPIO_7	–1299.420	–129.222	1299.420	–129.222
88	VSSC	–610.290	–270.648	610.290	–270.648
89	GPIO_6	–1157.994	–270.648	1157.994	–270.648
90	VSSC	–44.586	–412.074	44.586	–412.074
91	GPIO_4	–1299.420	–412.074	1299.420	–412.074
92	VSSC	96.840	–553.500	–96.840	–553.500
93	VDDC	–186.012	–553.500	186.012	–553.500
94	GPIO_5	–1157.994	–553.500	1157.994	–553.500
95	VDDC	–44.586	–694.926	44.586	–694.926
96	WL_VDDP_ISO	–733.716	–694.926	733.716	–694.926
97	GPIO_2	–1299.420	–694.926	1299.420	–694.926
98	GPIO_3	–1157.994	–836.352	1157.994	–836.352
99	WCC_VDDIO	–1016.568	–977.778	1016.568	–977.778
100	GPIO_0	–1299.420	–977.778	1299.420	–977.778
101	GPIO_1	–1157.994	–1119.204	1157.994	–1119.204
102	VSSC	–720.954	–1120.266	720.954	–1120.266
103	WCC_VDDIO	–1016.568	–1260.630	1016.568	–1260.630
104	SDIO_CMD	–1299.420	–1260.630	1299.420	–1260.630
105	GPIO_14	–137.700	–1268.568	137.700	–1268.568
106	VSSC	–841.113	–1402.056	841.113	–1402.056
107	VDDC	–1016.568	–1543.482	1016.568	–1543.482
108	SDIO_CLK	–1299.420	–1543.482	1299.420	–1543.482
109	GPIO_15	109.152	–1551.420	–109.152	–1551.420
110	PACKAGEOPTION_0	–173.700	–1551.420	173.700	–1551.420
111	VSSC	–843.237	–1682.775	843.237	–1682.775
112	SDIO_DATA_0	–1157.994	–1684.908	1157.994	–1684.908

Table 17. CYW4343W WLCSP Bump List — Ordered By Bump Number (Cont.)

Bump Number	Bump Name	Bump View (0,0 Center of Die)		Top View (0,0 Center of Die)	
		X Coordinate	Y Coordinate	X Coordinate	Y Coordinate
113	PACKAGEOPTION_1	–32.274	–1692.846	32.274	–1692.846
114	VDDC	–1016.568	–1826.334	1016.568	–1826.334
115	SDIO_DATA_1	–1299.420	–1826.334	1299.420	–1826.334
116	PACKAGEOPTION_2	109.152	–1834.272	–109.152	–1834.272
117	JTAG_SEL	–173.700	–1834.272	173.700	–1834.272
118	SDIO_DATA_2	–1157.994	–1967.760	1157.994	–1967.760
119	GPIO_13	–232.227	–2056.131	232.227	–2056.131
120	WCC_VDDIO	–1016.568	–2109.186	1016.568	–2109.186
121	VSSC	–1299.420	–2109.186	1299.420	–2109.186
122	SDIO_DATA_3	–1157.994	–2250.612	1157.994	–2250.612
123	SR_PVSS	–739.130	2274.984	739.130	2274.984
124	SR_PVSS	–1021.973	2274.984	1021.973	2274.984
125	VSSC	–597.708	2133.563	597.708	2133.563
126	SR_VLX	–880.551	2133.563	880.551	2133.563
127	SR_VLX	–1163.394	2133.563	1163.394	2133.563
128	SR_VLX	–739.130	1992.141	739.130	1992.141
129	SR_VDDBAT5V	–1021.973	1992.141	1021.973	1992.141
130	SR_VDDBAT5V	–1304.816	1992.141	1304.816	1992.141
131	PMU_AVSS	–597.708	1850.720	597.708	1850.720
132	SR_VDDBAT5V	–880.551	1850.720	880.551	1850.720
133	LDO_VDD1P5	–1021.973	1709.298	1021.973	1709.298
134	VOUT_CLDO	–880.551	1567.877	880.551	1567.877
135	LDO_VDD1P5	–1163.394	1567.877	1163.394	1567.877
136	VOUT_CLDO	–739.130	1426.455	739.130	1426.455
137	WCC_VDDIO	–597.708	1285.034	597.708	1285.034
138	VOUT_LNLDO	–880.551	1285.034	880.551	1285.034
139	VOUT_3P3	–1163.394	1285.034	1163.394	1285.034
140	SYS_VDDIO	–739.130	1143.612	739.130	1143.612
141	LDO_VDDBAT5V	–1304.816	1143.612	1304.816	1143.612
142	VSSC	–597.708	1002.191	597.708	1002.191
143	VOUT_3P3_SENSE	–880.551	1002.191	880.551	1002.191
144	VOUT_3P3	–1163.394	1002.191	1163.394	1002.191
145	WPT_1P8	–739.130	860.769	739.130	860.769
146	WPT_3P3	–1021.973	860.769	1021.973	860.769
147	LDO_VDDBAT5V	–1304.816	860.769	1304.816	860.769
148	WL_REG_ON	–597.708	719.348	597.708	719.348
149	BT_REG_ON	–880.551	719.348	880.551	719.348
150	WL_VDDM_ISO	–875.142	12.204	875.142	12.204

Table 17. CYW4343W WLCSP Bump List — Ordered By Bump Number (Cont.)

Bump Number	Bump Name	Bump View (0,0 Center of Die)		Top View (0,0 Center of Die)	
		X Coordinate	Y Coordinate	X Coordinate	Y Coordinate
151	PLL_VSSC	–116.586	–985.716	116.586	-985.716
152	PLL_VDDC	29.286	–1130.076	–29.286	–1130.076
153	CLK_REQ	238.266	1992.168	–238.266	1992.168

13.4 WLBGA Ball List Ordered By Ball Name

Table 18 provides the ball numbers and names in ball name order.

Table 18. CYW4343W WLBGA Ball List — Ordered By Ball Name

Ball Name	Ball Number
BT_DEV_WAKE	B1
BT_GPIO_3	F4
BT_GPIO_4	G5
BT_GPIO_5	H5
BT_HOST_WAKE	C1
BT_I2S_CLK or BT_PCM_CLK	A4
BT_I2S_DO or BT_PCM_OUT	B3
BT_I2S_WS or BT_PCM_SYNC	A3
BT_IF_VDD	G1
BT_IF_VSS	H2
BT_PAVDD	H1
BT_PCM_CLK or BT_I2S_CLK	A5
BT_PCM_IN or BT_I2S_DI	C4
BT_PCM_OUT or BT_I2S_DO	B4
BT_PCM_SYNC or BT_I2S_WS	B5
BT_REG_ON	E6
BT_UART_CTS_N	B2
BT_UART_RTS_N	C3
BT_UART_RXD	A1
BT_UART_TXD	A2
BT_VCO_VDD	F1
BT_VCO_VSS	H3
BTFM_PLL_VDD	F2
BTFM_PLL_VSS	G2
CLK_REQ	M6
FM_OUT1	C2
FM_OUT2	D2
FM_RF_IN	E1
FM_RF_VDD	E2
FM_RF_VSS	E3
GPIO_0	J6
GPIO_1	H6
GPIO_2	L5
GPIO_3	K4
GPIO_4	K5
LDO_VDD1P5	C7
LDO_VDDBAT5V	F7
LPO_IN	F5
PMU_AVSS	B6
SDIO_CLK	M7
SDIO_CMD	L6
SDIO_DATA_0	K6
SDIO_DATA_1	H7
SDIO_DATA_2	L7
SDIO_DATA_3	J7
SR_PVSS	A7
SR_VDDBAT5V	B7
SR_VLX	A6
SYS_VDDIO	C5
VDDC	D3
VDDC	G4
VOUT_3P3	E7
VOUT_CLDO	C6
VOUT_LNLDO	D6
VSSC	D4
VSSC	J5
WCC_VDDIO	F6
WL_REG_ON	G6
WLRF_2G_eLG	J1
WLRF_2G_RF	K1
WLRF_AFE_GND	H4
WLRF_GENERAL_GND	K2
WLRF_GPIO	J3
WLRF_LNA_GND	J2
WLRF_PA_GND	L2
WLRF_PA_VDD	M1
WLRF_VCO_GND	L3
WLRF_VDD_1P35	M2
WLRF_XTAL_GND	L4
WLRF_XTAL_VDD1P2	M3
WLRF_XTAL_XON	M5
WLRF_XTAL_XOP	M4
WPT_1P8	D5
WPT_3P3	E5

13.5 WLCSP Bump List Ordered By Name

Table 19 provides the bump numbers and names in bump name order.

Table 19. CYW4343W WLCSP Bump List — Ordered By Bump Name

Bump Name	Bump Number(s)
BT_AGPIO	52
BT_DEV_WAKE	6
BT_DVSS	50
BT_GPIO_2	13
BT_GPIO_3	5
BT_GPIO_4	8
BT_GPIO_5	10
BT_HOST_WAKE	11
BT_I2S_CLK or BT_PCM_CLK	15
BT_I2S_DI or BT_PCM_IN	23
BT_I2S_DO or BT_PCM_OUT	24
BT_I2S_WS or BT_PCM_SYNC	18
BT_IFVDD1P2	51
BT_LNAVDD1P2	54
BT_LNAVSS	55
BT_PAVDD2P5	53
BT_PAVSS	35
BT_PCM_CLK or BT_I2S_CLK	3
BT_PCM_IN or BT_I2S_DI	20
BT_PCM_OUT or BT_I2S_DO	19
BT_PCM_SYNC or BT_I2S_WS	17
BT_PLLVDD1P2	59
BT_PLLVSS	56
BT_REG_ON	149
BT_TM1	4
BT_UART_CTS_N	22
BT_UART_RTS_N	7
BT_UART_RXD	1
BT_UART_TXD	12
BT_VCOVDD1P2	57
BT_VCOVSS	58
BT_VDDC	14, 16, 26, 28, 31, 34
BT_VDDC_ISO_1	9
BT_VDDC_ISO_2	2
CLK_REQ	153
FM_DAC_AVDD	41
FM_DAC_AVSS	38
FM_DAC_VOUT1	37
FM_DAC_VOUT2	40
FM_IFDVDD1P2	48
FM_IFVSS	47
FM_PLLAVSS	39
FM_PLLDVDD1P2	43
FM_RFINMAIN	49
FM_RFVDD1P2	45
FM_RFVSS	46
FM_VCOVDD1P2	44
FM_VCOVSS	42
GPIO_0	100
GPIO_1	101
GPIO_2	97
GPIO_3	98
GPIO_4	91
GPIO_5	94
GPIO_6	89
GPIO_7	87
GPIO_8	84
GPIO_9	82
GPIO_10	83
GPIO_11	81
GPIO_12	80
GPIO_13	119
GPIO_14	105
GPIO_15	109
JTAG_SEL	117
LDO_VDD1P5	133, 135
LDO_VDDBAT5V	141, 147
LPO_IN	76
PACKAGEOPTION_0	110
PACKAGEOPTION_1	113
PACKAGEOPTION_2	116
PLL_VDDC	152
PLL_VSSC	151
PMU_AVSS	131
SDIO_CLK	108
SDIO_CMD	104
SDIO_DATA_0	112
SDIO_DATA_1	115

Bump Name	Bump Number(s)
SDIO_DATA_2	118
SDIO_DATA_3	122
SR_PVSS	123, 124
SR_VDDBAT5V	129, 130, 132
SR_VLX	126, 127, 128
SYS_VDDIO	140
VDDC	86, 93, 95, 107, 114
VOUT_3P3	139, 144
VOUT_3P3_SENSE	143
VOUT_CLDO	134, 136
VOUT_LNLDO	138
VSSC	21, 25, 27, 29, 30, 32, 33, 36, 78, 85, 88, 90, 92, 102, 106, 111, 121, 125, 142
WCC_VDDIO	77, 79, 99, 103, 120, 137
WL_REG_ON	148
WL_VDDM_ISO	150
WL_VDDP_ISO	96
WPT_1P8	145
WPT_3P3	146
WRF_AFE_GND	60
WRF_GENERAL_GND	64
WRF_GPAIO_OUT	67
WRF_PA_GND3P3	65, 69, 70, 71
WRF_PMU_VDD1P35	68
WRF_RFIN_ELG_2G	61
WRF_RFIO_2G	63
WRF_RX2G_GND	62
WRF_VCO_GND	66
WRF_XTAL_GND1P2	72
WRF_XTAL_VDD1P2	73
WRF_XTAL_XON	75
WRF_XTAL_XOP	74

13.6 Signal Descriptions

Table 20 provides the WLBGA package signal descriptions.

Table 20. WLBGA Signal Descriptions

Signal Name	WLBGA Ball	Type	Description
RF Signal Interface			
WLRF_2G_RF	K1	O	2.4 GHz BT and WLAN RF output port
SDIO Bus Interface			
SDIO_CLK	M7	I	SDIO clock input
SDIO_CMD	L6	I/O	SDIO command line
SDIO_DATA_0	K6	I/O	SDIO data line 0
SDIO_DATA_1	H7	I/O	SDIO data line 1.
SDIO_DATA_2	L7	I/O	SDIO data line 2. Also used as a strapping option (see Table 24).
SDIO_DATA_3	J7	I/O	SDIO data line 3
Note: Per Section 6 of the SDIO specification, 10 to 100 kΩ pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO host pull-ups.			
WLAN GPIO Interface			
WLRF_GPIO	J3	I/O	Test pin. Not connected in normal operation.
Clocks			
WLRF_XTAL_XON	M5	O	XTAL oscillator output
WLRF_XTAL_XOP	M4	I	XTAL oscillator input
CLK_REQ	M6	O	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required. Shared by BT, and WLAN.
LPO_IN	F5	I	External sleep clock input (32.768 kHz). If an external 32.768 kHz clock cannot be provided, pull this pin low. However, BLE will be always on and cannot go to deep sleep.
FM Receiver			
FM_OUT1	C2	O	FM analog output 1
FM_OUT2	D2	O	FM analog output 2
FM_RF_IN	E1	I	FM radio antenna port
FM_RF_VDD	E2	I	FM power supply
Bluetooth PCM			
BT_PCM_CLK or BT_I2S_CLK	A5	I/O	PCM or I^2S clock; can be master (output) or slave (input)
BT_PCM_IN or BT_I2S_DI	C4	I	PCM or I^2S data input sensing
BT_PCM_OUT or BT_I2S_DO	B4	O	PCM or I^2S data output
BT_PCM_SYNC or BT_I2S_WS	B5	I/O	PCM SYNC or I2S_WS; can be master (output) or slave (input)
Bluetooth GPIO			
BT_GPIO_3	F4	I/O	WPT_INTb to wireless charging PMU.
BT_GPIO_4	G5	I/O	BSC_SDA to/from wireless charging PMU.
BT_GPIO_5	H5	I/O	BSC_SCL from wireless charging PMU.

Table 20. WLBGA Signal Descriptions (Cont.)

Signal Name	WLBGA Ball	Type	Description
Bluetooth UART and Wake			
BT_UART_CTS_N	B2	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
BT_UART_RTS_N	C3	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
BT_UART_RXD	A1	I	UART serial input. Serial data input for the HCI UART interface.
BT_UART_TXD	A2	O	UART serial output. Serial data output for the HCI UART interface.
BT_DEV_WAKE	B1	I/O	DEV_WAKE or general-purpose I/O signal.
BT_HOST_WAKE	C1	I/O	HOST_WAKE or general-purpose I/O signal.
Note: By default, the Bluetooth BT WAKE signals provide GPIO/WAKE functionality, and the UART pins provide UART functionality. Through software configuration, the PCM interface can also be routed over the BT_WAKE/UART signals as follows: ■ PCM_CLK on the UART_RTS_N pin ■ PCM_OUT on the UART_CTS_N pin ■ PCM_SYNC on the BT_HOST_WAKE pin ■ PCM_IN on the BT_DEV_WAKE pin In this case, the BT HCI transport included sleep signaling will operate using UART_RXD and UART_TXD; that is, using a 3-Wire UART Transport.			
Bluetooth/FM I^2S			
BT_I2S_CLK or BT_PCM_CLK	A4	I/O	I^2S or PCM clock; can be master (output) or slave (input)
BT_I2S_DO or BT_PCM_OUT	B3	I/O	I^2S or PCM data output
BT_I2S_WS or BT_PCM_SYNC	A3	I/O	I^2S WS or PCM sync; can be master (output) or slave (input)
Miscellaneous			
WL_REG_ON	G6	I	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	E6	I	Used by PMU to power up or power down the internal regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
WPT_3P3	E5	N/A	Not used. Do not connect to this pin.
WPT_1P8	D5	N/A	Not used. Do not connect to this pin.
GPIO_0	J6	I/O	Programmable GPIO pins. This pin becomes an output pin when it is used as WLAN_HOST_WAKE/out-of-band signal.
GPIO_1	H6	I/O	Programmable GPIO pins
GPIO_2	L5	I/O	Programmable GPIO pins
GPIO_3	K4	I/O	Programmable GPIO pins
GPIO_4	K5	I/O	Programmable GPIO pins
WLRF_2G_eLG	J1	I	Connect to an external inductor. See the reference schematic for details.

Table 20. WLBGA Signal Descriptions (Cont.)

Signal Name	WLBGA Ball	Type	Description
Integrated Voltage Regulators			
SR_VDDBAT5V	B7	I	SR VBAT input power supply
SR_VLX	A6	O	CBUCK switching regulator output. See Table 39 for details of the inductor and capacitor required on this output.
LDO_VDDBAT5V	F7	I	LDO VBAT
LDO_VDD1P5	C7	I	LNLDO input
VOUT_LNLDO	D6	O	Output of low-noise LNLDO
VOUT_CLDO	C6	O	Output of core LDO
Bluetooth Power Supplies			
BT_PAVDD	H1	I	Bluetooth PA power supply
BT_IF_VDD	G1	I	Bluetooth IF block power supply
BTFM_PLL_VDD	F2	I	Bluetooth RF PLL power supply
BT_VCO_VDD	F1	I	Bluetooth RF power supply
Power Supplies			
WLRF_XTAL_VDD1P2	M3	I	XTAL oscillator supply
WLRF_PA_VDD	M1	I	Power amplifier supply
WCC_VDDIO	F6	I	VDDIO input supply. Connect to VDDIO.
SYS_VDDIO	C5	I	VDDIO input supply. Connect to VDDIO.
WLRF_VDD_1P35	M2	I	LNLDO input supply
VDDC	D3, G4	I	Core supply for WLAN and BT.
VOUT_3P3	E7	O	3.3V output supply. See the reference schematic for details.
Ground			
BT_IF_VSS	H2	I	1.2V Bluetooth IF block ground
BTFM_PLL_VSS	G2	I	Bluetooth/FM RF PLL ground
BT_VCO_VSS	H3	I	1.2V Bluetooth RF ground
FM_RF_VSS	E3	I	FM RF ground
PMU_AVSS	B6	I	Quiet ground
SR_PVSS	A7	I	Switcher-power ground
VSSC	D4, J5	I	Core ground for WLAN and BT
WLRF_AFE_GND	H4	I	AFE ground
WLRF_LNA_GND	J2	I	2.4 GHz internal LNA ground
WLRF_GENERAL_GND	K2	I	Miscellaneous RF ground
WLRF_PA_GND	L2	I	2.4 GHz PA ground
WLRF_VCO_GND	L3	I	VCO/LO generator ground
WLRF_XTAL_GND	L4	I	XTAL ground

Table 21 provides the WLCSP package signal descriptions.

Table 21. WLCSP Signal Descriptions

Signal Name	WLCSP Bump	Type	Description or Instruction
RF Signal Interface			
WRF_RFIN_ELG_2G	61	I	Connect to an external inductor. See the reference schematic for details.
WRF_RFIO_2G	63	I/O	2.4 GHz BT and WLAN RF input/output port
SDIO Bus Interface			
SDIO_CLK	108	I	SDIO clock input
SDIO_CMD	104	I/O	SDIO command line
SDIO_DATA_0	112	I/O	SDIO data line 0
SDIO_DATA_1	115	I/O	SDIO data line 1.
SDIO_DATA_2	118	I/O	SDIO data line 2. Also used as a strapping option (see Table 24).
SDIO_DATA_3	122	I/O	SDIO data line 3
Note: Per Section 6 of the SDIO specification, 10 to 100 kΩ pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO host pull-ups.			
WLAN GPIO Interface			
WRF_GPAIO_OUT	67	O	Test pin. Not connected in normal operation.
Clocks			
WRF_XTAL_XON	75	O	XTAL oscillator output
WRF_XTAL_XOP	74	I	XTAL oscillator input
CLK_REQ	153	O	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required. Shared by BT, and WLAN.
LPO_IN	76	I	External sleep clock input (32.768 kHz). If an external 32.768 kHz clock cannot be provided, pull this pin low. However, BLE will be always on and cannot go to deep sleep.
FM			
FM_DAC_VOUT1	37	O	FM DAC output 1
FM_DAC_VOUT2	40	O	FM DAC output 2
FM_RFINMAIN	49	I	FM RF input
Bluetooth PCM			
BT_PCM_CLK or BT_I2S_CLK	3	I/O	PCM or I^2S clock; can be master (output) or slave (input)
BT_PCM_IN or BT_I2S_DI	20	I	PCM or I^2S data input sensing
BT_PCM_OUT or BT_I2S_DO	19	O	PCM or I^2S data output
BT_PCMM_SYNC or BT_I2S_WS	17	I/O	PCM SYNC or I2S WS; can be master (output) or slave (input)
Bluetooth GPIO			
BT_AGPIO	52	I/O	Bluetooth analog GPIO
BT_GPIO_2	13	I/O	Bluetooth general purpose I/O
BT_GPIO_3	5	I/O	WPT_INTb to wireless charging PMU.
BT_GPIO_4	8	I/O	BSC_SDA to/from wireless charging PMU.

Table 21. WLCSP Signal Descriptions (Cont.)

Signal Name	WLCSP Bump	Type	Description or Instruction
BT_GPIO_5	10	I/O	BSC_SCL from wireless charging PMU
BT_TM1	4	I/O	ARM JTAG mode
Bluetooth UART and Wake			
BT_UART_CTS_N	22	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
BT_UART_RTS_N	7	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
BT_UART_RXD	1	I	UART serial input. Serial data input for the HCI UART interface.
BT_UART_TXD	12	O	UART serial output. Serial data output for the HCI UART interface.
BT_DEV_WAKE	6	I/O	DEV_WAKE or general-purpose I/O signal
BT_HOST_WAKE	11	I/O	HOST_WAKE or general-purpose I/O signal
Note: By default, the Bluetooth BT WAKE signals provide GPIO/WAKE functionality, and the UART pins provide UART functionality. Through software configuration, the PCM interface can also be routed over the BT_WAKE/UART signals as follows: ■ PCM_CLK on the UART_RTS_N pin ■ PCM_OUT on the UART_CTS_N pin ■ PCM_SYNC on the BT_HOST_WAKE pin ■ PCM_IN on the BT_DEV_WAKE pin In this case, the BT HCI transport included sleep signaling will operate using UART_RXD and UART_TXD; that is, using a 3-Wire UART Transport.			
Bluetooth/FM I^2S			
BT_I2S_CLK or BT_PCM_CLK	15	I/O	I^2S or PCM clock; can be master (output) or slave (input)
BT_I2S_DI or BT_PCM_IN	23	I	I^2S or PCM data input
BT_I2S_DO or BT_PCM_OUT	24	O	I^2S or PCM data output
BT_I2S_WS or BT_PCM_SYNC	18	I/O	I^2S WS or PCM SYNC; can be master (output) or slave (input)
Miscellaneous			
WL_REG_ON	148	I	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	149	I	Used by PMU to power up or power down the internal regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
WPT_3P3	146	N/A	Not used. Do not connect to this pin.
WPT_1P8	145	N/A	Not used. Do not connect to this pin.
GPIO_0	100	I/O	Programmable GPIO pin. This pin becomes an output pin when it is used as WLAN_HOST_WAKE/out-of-band signal.
GPIO_1	101	I/O	Programmable GPIO pin
GPIO_2	97	I/O	Programmable GPIO pin

Table 21. WLCSP Signal Descriptions (Cont.)

Signal Name	WLCSP Bump	Type	Description or Instruction
GPIO_3	98	I/O	Programmable GPIO pin
GPIO_4	91	I/O	Programmable GPIO pin
GPIO_5	94	I/O	Programmable GPIO pin
GPIO_6	89	I/O	Programmable GPIO pin
GPIO_7	87	I/O	Programmable GPIO pin
GPIO_8	84	I/O	Programmable GPIO pin
GPIO_9	82	I/O	Programmable GPIO pin
GPIO_10	83	I/O	Programmable GPIO pin
GPIO_11	81	I/O	Programmable GPIO pin
GPIO_12	80	I/O	Programmable GPIO pin
GPIO_13	119	I/O	Programmable GPIO pin
GPIO_14	105	I/O	Programmable GPIO pin
GPIO_15	109	I/O	Programmable GPIO pin
PACKAGEOPTION_0	110	I	VDDIO
PACKAGEOPTION_1	113	I	Ground
PACKAGEOPTION_2	116	I	Ground
JTAG_SEL	117	I	JTAG select. Connect to ground.
Integrated Voltage Regulators			
SR_VDDBAT5V	129, 130, 132	I	SR VBAT input power supply
SR_VLX	126, 127, 128	O	CBUCK switching regulator output. See Table 39 for details of the inductor and capacitor required on this output.
LDO_VDDBAT5V	141, 147	I	LDO VBAT
LDO_VDD1P5	133, 135	I	LNLDO input
VOUT_LNLDO	138	O	Output of low-noise LDO (LNLDO)
VOUT_CLDO	134, 136	O	Output of core LDO
Bluetooth Power Supplies			
BT_IFVDD1P2	51	PWR	Bluetooth IF-block power supply
BT_LNAVDD1P2	54	PWR	Bluetooth RF LNA power supply
BT_PAVDD2P5	53	PWR	Bluetooth RF PA power supply
BT_PLLVDD1P2	59	PWR	Bluetooth RF PLL power supply
BT_VCOVDD1P2	57	PWR	Bluetooth RF power supply
BT_VDDC	14, 16, 26, 28, 31, 34	PWR	Bluetooth core power supply
BT_VDDC_ISO_1	9	PWR	Bluetooth core power supply
BT_VDDC_ISO_2	2	PWR	Bluetooth core power supply
Power Supplies			
FM_DAC_AVDD	41	PWR	FM DAC power supply
FM_IFDVDD1P2	48	PWR	FM IF power supply
FM_PLLDVDD1P2	43	PWR	FM PLL power supply
FM_RFVDD1P2	45	PWR	FM RF power supply
FM_VCOVDD1P2	44	PWR	FM VCO power supply

Table 21. WLCSP Signal Descriptions (Cont.)

Signal Name	WLCSP Bump	Type	Description or Instruction
PLL_VDDC	152	PWR	Core PLL power supply
SYS_VDDIO	140	I	VDDIO input supply. Connect to VDDIO.
VDDC	86, 93, 95, 107, 114	I	Core supply for WLAN and BT
VOUT_3P3	139, 144	O	3.3V output supply. See the reference schematic for details.
VOUT_3P3_SENSE	143	O	Voltage sense pin for LDO 3.3V output
WCC_VDDIO	77, 79, 99, 103, 120, 137	I	VDDIO input supply. Connect to VDDIO.
WL_VDDM_ISO	150	–	Test pin. Not connected in normal operation.
WL_VDDP_ISO	96	–	Test pin. Not connected in normal operation.
WRF_XTAL_VDD1P2	73	I	XTAL oscillator supply
WRF_PA_VDD3P3	70, 71	I	Power amplifier supply
WRF_PMU_VDD1P35	68	I	LNLDO input supply

Table 21. WLCSP Signal Descriptions (Cont.)

Signal Name	WLCSP Bump	Type	Description or Instruction
Ground			
BT_DVSS	50	GND	Bluetooth digital ground
BT_LNAVSS	55	GND	Bluetooth LNA ground
BT_PAVSS	35	GND	Bluetooth PA ground
BT_PLLVSS	56	GND	Bluetooth PLL ground
BT_VCOVSS	58	GND	Bluetooth VCO ground
FM_DAC_AVSS	38	GND	FM DAC analog ground
FM_IFVSS	47	GND	FM IF-block ground
FM_PLLAVSS	39	GND	FM PLL analog ground
FM_RFVSS	46	GND	FM RF ground
FM_VCOVSS	42	GND	FM VCO ground
PLL_VSSC	151	GND	PLL core ground
PMU_AVSS	131	I	Quiet ground
SR_PVSS	123, 124	I	Switcher-power ground
VSSC	21, 25, 27, 29, 30, 32, 33, 36, 78, 85, 88, 90, 92, 102, 106, 111, 121, 125, 142	I	Core ground for WLAN and BT
WRF_AFE_GND	60	I	AFE ground
WRF_RX2G_GND	62	I	2.4 GHz internal LNA ground
WRF_GENERAL_GND	64	I	Miscellaneous RF ground
WRF_PA_GND3P3	65, 69	I	2.4 GHz PA ground
WRF_VCO_GND	66	I	VCO/LO generator ground
WRF_XTAL_GND1P2	72	I	XTAL ground

13.7 WLAN GPIO Signals and Strapping Options

The pins listed in Table 22 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to ground using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 22. GPIO Functions and Strapping Options

Pin Name	WLBGA Pin #	Default	Function	Description
SDIO_DATA_2	L7	1	WLAN host interface select	This pin selects the WLAN host interface mode. The default is SDIO. For gSPI, pull this pin low.

13.8 Chip Debug Options

The chip can be accessed for debugging via the JTAG interface, multiplexed on the SDIO_DATA_0 through SDIO_DATA_3 (and SDIO_CLK) I/O or the Bluetooth PCM I/O depending on the bootstrap state of GPIO_1 and GPIO_2.

Table 23 shows the debug options of the device.

Table 23. Chip Debug Options

JTAG_SEL	GPIO_2	GPIO_1	Function	SDIO I/O Pad Function	BT PCM I/O Pad Function
0	0	0	Normal mode	SDIO	BT PCM
0	0	1	JTAG over SDIO	JTAG	BT PCM
0	1	0	JTAG over BT PCM	SDIO	JTAG
0	1	1	SWD over GPIO_1/GPIO_2	SDIO	BT PCM

13.9 I/O States

The following notations are used in Table 24:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 24. I/O States[a]

Name	I/O	Keeper[b]	Active Mode	Low Power State/Sleep (All Power Present)	Power-Down[c] WL_REG_ON = 0 BT_REG_ON = 0	Out-of-Reset; (WL_REG_ON = 1; BT_REG_ON = Do Not Care)	(WL_REG_ON = 1 BT_REG_ON = 0) VDDIOs Present	Out-of-Reset; (WL_REG_ON = 0 BT_REG_ON = 1) VDDIOs Present	Power Rail
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (200k)	Input; PD (200k)	–	–
BT_REG_ON	I	N	Input; PD (pull down can be disabled)	Input; PD (pull down can be disabled)	Input; PD (of 200K)	Input; PD (200k)	Input; PD (200k)	Input; PD (200k)	–
CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active high	PD	Open drain, active high.	Open drain, active high.	Open drain, active high.	WCC_VDDIO
BT_HOST_ WAKE	I/O	Y	I/O; PU, PD, NoPull (programmable)	I/O; PU, PD, NoPull (programmable)	High-Z, NoPull	–	Input, PD	Output, Drive low	WCC_VDDIO
BT_DEV_WAK E	I/O	Y	I/O; PU, PD, NoPull (programmable)	Input; PU, PD, NoPull (programmable)	High-Z, NoPull	–	Input, PD	Input, PD	WCC_VDDIO
BT_UART_CTS	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	–	Input; PU	Input, NoPull	WCC_VDDIO
BT_UART_RTS	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	–	Input; PU	Output, NoPull	WCC_VDDIO
BT_UART_RX D	I	Y	Input; PU	Input; NoPull	High-Z, NoPull	–	Input; PU	Input, NoPull	WCC_VDDIO
BT_UART_TXD	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	–	Input; PU	Output, NoPull	WCC_VDDIO
SDIO_DATA_0	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_DATA_1	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_DATA_2	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_DATA_3	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO

Table 24. I/O States[a] (Cont.)

Name	I/O	Keeper[b]	Active Mode	Low Power State/Sleep (All Power Present)	Power-Down[c] WL_REG_ON = 0 BT_REG_ON = 0	Out-of-Reset; (WL_REG_ON = 1; BT_REG_ON = Do Not Care)	(WL_REG_ON = 1 BT_REG_ON = 0) VDDIOs Present	Out-of-Reset; (WL_REG_ON = 0 BT_REG_ON = 1) VDDIOs Present	Power Rail
SDIO_CMD	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PU	SDIO MODE -> NoPull	Input; PU	WCC_VDDIO
SDIO_CLK	I	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	Input	WCC_VDDIO
BT_PCM_CLK	I/O	Y	Input; NoPull[d]	Input; NoPull[d]	High-Z, NoPull	–	Input, PD	Input, PD	WCC_VDDIO
BT_PCM_IN	I/O	Y	Input; NoPull[d]	Input; NoPull[d]	High-Z, NoPull	–	Input, PD	Input, PD	WCC_VDDIO
BT_PCM_OUT	I/O	Y	Input; NoPull[d]	Input; NoPull[d]	High-Z, NoPull	–	Input, PD	Input, PD	WCC_VDDIO
BT_PCM_SYNC	I/O	Y	Input; NoPull[d]	Input; NoPull[d]	High-Z, NoPull	–	Input, PD	Input, PD	WCC_VDDIO
BT_I2S_WS	I/O	Y	Input; NoPull[e]	Input; NoPull[e]	High-Z, NoPull	–	Input, PD	Input, PD	WCC_VDDIO
BT_I2S_CLK	I/O	Y	Input; NoPull[e]	Input; NoPull[e]	High-Z, NoPull	–	Input, PD	Output, Drive low	WCC_VDDIO
BT_I2S_DO	I/O	Y	Input; NoPull[e]	Input; NoPull[e]	High-Z, NoPull	–	Input, PD	Input, PD	WCC_VDDIO
JTAG_SEL	I	Y	PD	PD	High-Z, NoPull	Input, PD	PD	Input, PD	WCC_VDDIO
GPIO_0	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, SDIO OOB Int, NoPull	Active mode	Input, NoPull	WCC_VDDIO
GPIO_1	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, PD	Active mode	Input, Strap, PD	WCC_VDDIO
GPIO_2	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, GCI GPIO[7], NoPull	Active mode	Input, Strap, NoPull	WCC_VDDIO
GPIO_3	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, GCI GPIO[0], PU	Active mode	Input, PU	WCC_VDDIO
GPIO_4	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, GCI GPIO[1], PU	Active mode	Input, PU	WCC_VDDIO
GPIO_5	I/O	N	TBD	Active mode	High-Z, NoPull[f]	Input, GCI GPIO[2], PU	Active mode	Input, PU	WCC_VDDIO
GPIO_6	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, GCI GPIO[3], NoPull	Active mode	Input, NoPull	WCC_VDDIO
GPIO_7	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Output, WLAN UART RTS#, NoPull	Active mode	Output, NoPull, Low	WCC_VDDIO
GPIO_8	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, WLAN UART CTS#, NoPull	Active mode	Input, NoPull	WCC_VDDIO
GPIO_9	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, WLAN UART RX, NoPull	Active mode	Input, NoPull	WCC_VDDIO

Table 24. I/O States[a] (Cont.)

Name	I/O	Keeper[b]	Active Mode	Low Power State/Sleep (All Power Present)	Power-Down[c] WL_REG_ON = 0 BT_REG_ON = 0	Out-of-Reset; (WL_REG_ON = 1; BT_REG_ON = Do Not Care)	(WL_REG_ON = 1 BT_REG_ON = 0) VDDIOs Present	Out-of-Reset; (WL_REG_ON = 0 BT_REG_ON = 1) VDDIOs Present	Power Rail
GPIO_10	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Output, WLAN UART TX, NoPull	Active mode	Output, NoPull, Low	WCC_VDDIO
GPIO_11	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, Low, NoPull	Active mode	Input, NoPull	WCC_VDDIO
GPIO_12	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, GCI GPIO[6], NoPull	Active mode	Input, NoPull	WCC_VDDIO
GPIO_13	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, GCI GPIO[7], NoPull	Active mode	Input, NoPull	WCC_VDDIO
GPIO_14	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, PD	Active mode	Input, PD	WCC_VDDIO
GPIO_15	I/O	Y	TBD	Active mode	High-Z, NoPull[f]	Input, PD	Active mode	Input, PD	WCC_VDDIO

a. PU = pulled up, PD = pulled down.
b. N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in the power-down state. If there is no keeper, and it is an input and there is NoPull, then the pad should be driven to prevent leakage due to floating pad, for example, SDIO_CLK.
c. In the Power-down state (xx_REG_ON = 0): High-Z; NoPull => The pad is disabled because power is not supplied.
d. Depending on whether the PCM interface is enabled and the configuration is master or slave mode, it can be either an output or input.
e. Depending on whether the I^2S interface is enabled and the configuration is master or slave mode, it can be either an output or input.
f. The GPIO pull states for the active and low-power states are hardware defaults. They can all be subsequently programmed as a pull-up or pull-down.

14. DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

14.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 25 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Excluding VBAT, operation at the absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 25. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	VBAT	–0.5 to +6.0[a]	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
Maximum undershoot voltage for I/O[b]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[b]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C

a. Continuous operation at 6.0V is supported.
b. Duration not to exceed 25% of the duty cycle.

14.2 Environmental Ratings

The environmental ratings are shown in Table 26.

Table 26. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient temperature (T_A)	–30 to +70°C [a]	°C	Operation
Storage temperature	–40 to +125°C	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed, but specifications require derating at extreme temperatures (see the specification tables for details).

14.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 27. ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human Body Model Contact Discharge per JEDEC EID/JESD22-A114	1000	V
Machine Model (MM)	ESD_HAND_MM	Machine Model Contact	30	V
CDM	ESD_HAND_CDM	Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101	300	V

14.4 Recommended Operating Conditions and DC Characteristics

Functional operation is not guaranteed outside the limits shown in Table 28, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 28. Recommended Operating Conditions and DC Characteristics

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0[a]	–	4.8[b]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
SDIO Interface I/O Pins					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					

Table 28. Recommended Operating Conditions and DC Characteristics (Cont.)

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[c]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

a. The CYW4343W is functional across this range of voltages. However, optimal RF performance specified in the data sheet is guaranteed only for 3.2V < VBAT < 4.8V.
b. The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration over the lifetime of the device are allowed.
c. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

15. WLAN RF Specifications

The CYW4343W includes an integrated direct conversion radio that supports the 2.4 GHz band. This section describes the RF characteristics of the 2.4 GHz radio.

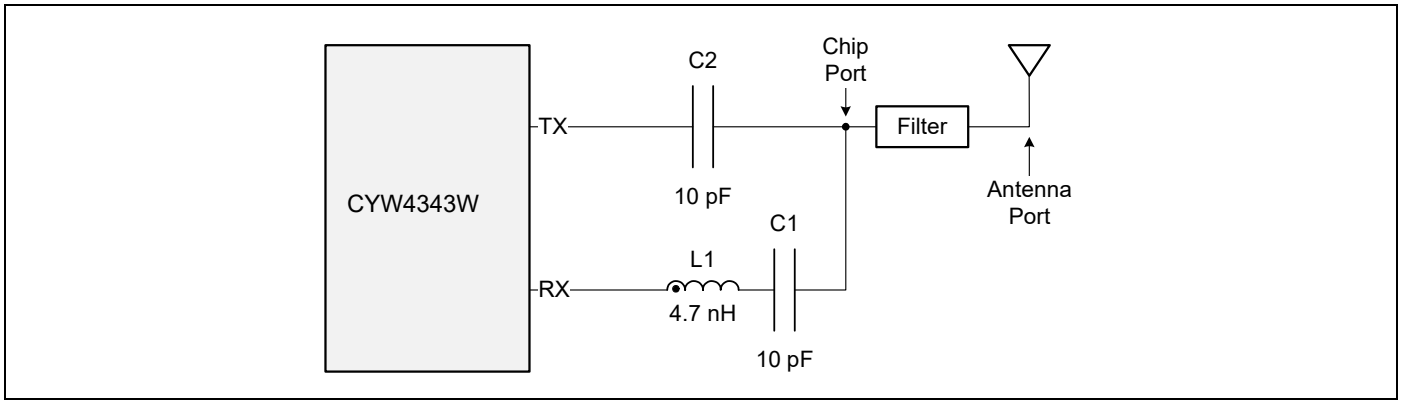
Note: Values in this data sheet are design goals and may change based on device characterization results.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 26 and Table 28. Functional operation outside these limits is not guaranteed.

Typical values apply for the following conditions:

- VBAT = 3.6V.
- Ambient temperature +25°C.

Figure 35. RF Port Location



Note: All specifications apply at the chip port unless otherwise specified.

15.1 2.4 GHz Band General RF Specifications

Table 29. 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs

15.2 WLAN 2.4 GHz Receiver Performance Specifications

Note: Unless otherwise specified, the specifications in Table 30 are measured at the chip port (for the location of the chip port, see Figure 35).

Table 30. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity (8% PER for 1024 octet PSDU) [a]	1 Mbps DSSS	–97.5	–99.5	–	dBm
	2 Mbps DSSS	–93.5	–95.5	–	dBm
	5.5 Mbps DSSS	–91.5	–93.5	–	dBm
	11 Mbps DSSS	–88.5	–90.5	–	dBm
RX sensitivity (10% PER for 1000 octet PSDU) at WLAN RF port [a]	6 Mbps OFDM	–91.5	–93.5	–	dBm
	9 Mbps OFDM	–90.5	–92.5	–	dBm
	12 Mbps OFDM	–87.5	–89.5	–	dBm
	18 Mbps OFDM	–85.5	–87.5	–	dBm
	24 Mbps OFDM	–82.5	–84.5	–	dBm
	36 Mbps OFDM	–80.5	–82.5	–	dBm
	48 Mbps OFDM	–76.5	–78.5	–	dBm
	54 Mbps OFDM	–75.5	–77.5	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU). Defined for default parameters: Mixed mode, 800 ns GI.	20 MHz channel spacing for all MCS rates (Mixed mode)				
	256-QAM, R = 5/6	–67.5	–69.5	–	dBm
	256-QAM, R = 3/4	–69.5	–71.5	–	dBm
	MCS7	–71.5	–73.5	–	dBm
	MCS6	–73.5	–75.5	–	dBm
	MCS5	–74.5	–76.5	–	dBm
	MCS4	–79.5	–81.5	–	dBm
	MCS3	–82.5	–84.5	–	dBm
	MCS2	–84.5	–86.5	–	dBm
	MCS1	–86.5	–88.5	–	dBm
	MCS0	–90.5	–92.5	–	dBm

Table 30. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Blocking level for 3 dB RX sensitivity degradation (without external filtering).[b]	704–716 MHz	LTE	–	–13	–	dBm
	777–787 MHz	LTE	–	–13	–	dBm
	776–794 MHz	CDMA2000	–	–13.5	–	dBm
	815–830 MHz	LTE	–	–12.5	–	dBm
	816–824 MHz	CDMA2000	–	–13.5	–	dBm
	816–849 MHz	LTE	–	–11.5	–	dBm
	824–849 MHz	WCDMA	–	–11.5	–	dBm
	824–849 MHz	CDMA2000	–	–12.5	–	dBm
	824–849 MHz	LTE	–	–11.5	–	dBm
	824–849 MHz	GSM850	–	–8	–	dBm
	830–845 MHz	LTE	–	–11.5	–	dBm
	832–862 MHz	LTE	–	–11.5	–	dBm
	880–915 MHz	WCDMA	–	–10	–	dBm
	880–915 MHz	LTE	–	–12	–	dBm
	880–915 MHz	E-GSM	–	–9	–	dBm
	1710–1755 MHz	WCDMA	–	–13	–	dBm
	1710–1755 MHz	LTE	–	–14.5	–	dBm
	1710–1755 MHz	CDMA2000	–	–14.5	–	dBm
	1710–1785 MHz	WCDMA	–	–13	–	dBm
	1710–1785 MHz	LTE	–	–14.5	–	dBm
	1710–1785 MHz	GSM1800	–	–12.5	–	dBm
	1850–1910 MHz	GSM1900	–	–11.5	–	dBm
	1850–1910 MHz	CDMA2000	–	–16	–	dBm
	1850–1910 MHz	WCDMA	–	–13.5	–	dBm
	1850–1910 MHz	LTE	–	–16	–	dBm
	1850–1915 MHz	LTE	–	–17	–	dBm
	1920–1980 MHz	WCDMA	–	–17.5	–	dBm
	1920–1980 MHz	CDMA2000	–	–19.5	–	dBm
	1920–1980 MHz	LTE	–	–19.5	–	dBm
	2300–2400 MHz	LTE	–	–44	–	dBm
	2500–2570 MHz	LTE	–	–43	–	dBm
	2570–2620 MHz	LTE	–	–34	–	dBm
	5G	WLAN	–	>–4	–	dBm
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–6	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–12	–	–	dBm
	@ 6–54 Mbps (10% PER, 1000 octets)		–15.5	–	–	dBm

Table 30. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection-DSSS. (Difference between interfering and desired signal [25 MHz apart] at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes.)	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM. (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1000[c] octet PSDU with desired signal level as specified in Condition/Notes.)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
RCPI accuracy[d]	Range –98 dBm to –75 dBm		–3	–	3	dB
	Range above –75 dBm		–5	–	5	dB
Return loss	Zo = 50Ω across the dynamic range.		10	–	–	dB

a. Optimal RF performance, as specified in this data sheet, is guaranteed only for temperatures between –10°C and 55°C.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. For 65 Mbps, the size is 4096.
d. The minimum and maximum values shown have a 95% confidence level.

15.3 WLAN 2.4 GHz Transmitter Performance Specifications

Note: Unless otherwise specified, the specifications in Table 30 are measured at the chip port (for the location of the chip port, see Figure 35).

Table 31. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		–	–	–	MHz
Transmitted power in cellular and WLAN 5G bands (at 21 dBm, 90% duty cycle, 1 Mbps CCK).[a]	776–794 MHz	CDMA2000	–	–167.5	–	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	–	–163.5	–	dBm/Hz
	1450–1495 MHz	DAB	–	–154.5	–	dBm/Hz
	1570–1580 MHz	GPS	–	–152.5	–	dBm/Hz
	1592–1610 MHz	GLONASS	–	–149.5	–	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	–	–145.5	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–143.5	–	dBm/Hz
	1850–1910 MHz	GSM1900	–	–140.5	–	dBm/Hz
	1910–1930 MHz	TDSCDMA, LTE	–	–138.5	–	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne, WCDMA	–	–139	–	dBm/Hz
	2010–2075 MHz	TDSCDMA	–	–127.5	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–124.5	–	dBm/Hz
	2305–2370 MHz	LTE Band 40	–	–104.5	–	dBm/Hz
	2370–2400 MHz	LTE Band 40	–	–81.5	–	dBm/Hz
	2496–2530 MHz	LTE Band 41	–	–94.5	–	dBm/Hz
	2530–2560 MHz	LTE Band 41	–	–120.5	–	dBm/Hz
	2570–2690 MHz	LTE Band 41	–	–121.5	–	dBm/Hz
	5000–5900 MHz	WLAN 5G	–	–109.5	–	–
Harmonic level (at 21 dBm with 90% duty cycle, 1 Mbps CCK)	4.8–5.0 GHz	2nd harmonic	–	–26.5	–	dBm/ MHz
	7.2–7.5 GHz	3rd harmonic	–	–23.5	–	dBm/ MHz
	9.6–10 GHz	4th harmonic	–	–32.5	–	dBm/ MHz
TX power at the chip port for the highest power level setting at 25°C, VBA = 3.6V, and spectral mask and EVM compliance[b, c]	–	**EVM Does Not Exceed**				
	IEEE 802.11b (DSSS/CCK)	–9 dB	21	–	–	dBm
	OFDM, BPSK	–8 dB	20.5	–	–	dBm
	OFDM, QPSK	–13 dB	20.5	–	–	dBm
	OFDM, 16-QAM	–19 dB	20.5	–	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	18	–	–	dBm
	OFDM, 64-QAM (R = 5/6)	–27 dB	17.5	–	–	dBm
	OFDM, 256-QAM (R = 5/6)	–32 dB	15	–	–	dBm
TX power control dynamic range	–		9	–	–	dB

Table 31. WLAN 2.4 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Closed loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies across 5 to 21 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Zo = 50		4	6	–	dB
Load pull variation for output power, EVM, and Adjacent Channel Power Ratio (ACPR)	VSWR = 2:1.	EVM degradation	–	3.5	–	dB
		Output power variation	–	±2	–	dB
		ACPR-compliant power level	–	15	–	dBm
	VSWR = 3:1.	EVM degradation	–	4	–	dB
		Output power variation	–	±3	–	dB
		ACPR-compliant power level	–	15	–	dBm

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.
b. TX power for channel 1 and channel 11 is specified separately by nonvolatile memory parameters to ensure band-edge compliance.
c. Optimal RF performance, as specified in this data sheet, is guaranteed only for temperatures between –10°C and 55°C.

15.4 General Spurious Emissions Specifications

Table 32. General Spurious Emissions Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–99	–96	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–44	–41	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–68	–65	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–88	–85	dBm
RX/standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–99	–96	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–54	–51	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–88	–85	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–88	–85	dBm
Note: The specifications in this table apply at the chip port.						

16. Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 26 and Table 28. Typical values apply for the following conditions:

- VBAT = 3.6V.
- Ambient temperature +25°C.

Note: All Bluetooth specifications apply at the chip port. For the location of the chip port, see Figure 35.

Table 33. Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the chip output port unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–94	–	dBm
	π/4–DQPSK, 0.01% BER, 2 Mbps	–	–96	–	dBm
	8–DPSK, 0.01% BER, 3 Mbps	–	–90	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
Interference Performance[a]					
C/I co-channel	GFSK, 0.1% BER	–	–	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0.0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20	dB
C/I co-channel	π/4–DQPSK, 0.1% BER	–	–	13	dB
C/I 1 MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–	0.0	dB
C/I 2 MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3 MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–	–40	dB
C/I image channel	π/4–DQPSK, 0.1% BER	–	–	–7	dB
C/I 1 MHz adjacent to image channel	π/4–DQPSK, 0.1% BER	–	–	–20	dB
C/I co-channel	8–DPSK, 0.1% BER	–	–	21	dB
C/I 1 MHz adjacent channel	8–DPSK, 0.1% BER	–	–	5.0	dB
C/I 2 MHz adjacent channel	8–DPSK, 0.1% BER	–	–	–25	dB
C/I ≥ 3 MHz adjacent channel	8–DPSK, 0.1% BER	–	–	–33	dB
C/I Image channel	8–DPSK, 0.1% BER	–	–	0.0	dB
C/I 1 MHz adjacent to image channel	8–DPSK, 0.1% BER	–	–	–13	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm

Table 33. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Out-of-Band Blocking Performance, Modulated Interferer (LTE)					
GFSK (1 Mbps)					
2310 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2330 MHz	LTE band40 TDD 20M BW	–	–19	–	dBm
2350 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2370 MHz	LTE band40 TDD 20M BW	–	–24	–	dBm
2510 MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
2530 MHz	LTE band7 FDD 20M BW	–	–21	–	dBm
2550 MHz	LTE band7 FDD 20M BW	–	–21	–	dBm
2570 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
π/4 DPSK (2 Mbps)					
2310 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2330 MHz	LTE band40 TDD 20M BW	–	–19	–	dBm
2350 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2370 MHz	LTE band40 TDD 20M BW	–	–24	–	dBm
2510 MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
2530 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
2550 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
2570 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
8DPSK (3 Mbps)					
2310 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2330 MHz	LTE band40 TDD 20M BW	–	–19	–	dBm
2350 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2370 MHz	LTE band40 TDD 20M BW	–	–24	–	dBm
2510 MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
2530 MHz	LTE band7 FDD 20M BW	–	–21	–	dBm
2550 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
2570 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer (Non-LTE)					
GFSK (1 Mbps)[a]					
698–716 MHz	WCDMA	–	–12	–	dBm
776–849 MHz	WCDMA	–	–12	–	dBm
824–849 MHz	GSM850	–	–12	–	dBm
824–849 MHz	WCDMA	–		–	dBm
880–915 MHz	E-GSM	–	–11	–	dBm
880–915 MHz	WCDMA	–		–	dBm
1710–1785 MHz	GSM1800	–		–	dBm
1710–1785 MHz	WCDMA	–		–	dBm

Table 33. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
1850–1910 MHz	GSM1900	–		–	dBm
1850–1910 MHz	WCDMA	–	–17	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18	–	dBm
1920–1980 MHz	WCDMA	–	–18	–	dBm
2010–2025 MHz	TD–SCDMA	–	–18	–	dBm
2500–2570 MHz	WCDMA	–	–21	–	dBm
π/4 DPSK (2 Mbps)[a]					
698–716 MHz	WCDMA	–	–8	–	dBm
776–794 MHz	WCDMA	–	–8	–	dBm
824–849 MHz	GSM850	–	–9	–	dBm
824–849 MHz	WCDMA	–	–9	–	dBm
880–915 MHz	E-GSM	–	–8	–	dBm
880–915 MHz	WCDMA	–	–8	–	dBm
1710–1785 MHz	GSM1800	–	–14	–	dBm
1710–1785 MHz	WCDMA	–	–14	–	dBm
1850–1910 MHz	GSM1900	–	–15	–	dBm
1850–1910 MHz	WCDMA	–	–14	–	dBm
1880–1920 MHz	TD-SCDMA	–	–16	–	dBm
1920–1980 MHz	WCDMA	–	–15	–	dBm
2010–2025 MHz	TD-SCDMA	–	–17	–	dBm
2500–2570 MHz	WCDMA	–	–21	–	dBm
8DPSK (3 Mbps)[a]					
698–716 MHz	WCDMA	–	–11	–	dBm
776–794 MHz	WCDMA	–	–11	–	dBm
824–849 MHz	GSM850	–	–11	–	dBm
824–849 MHz	WCDMA	–	–12	–	dBm
880–915 MHz	E-GSM	–	–11	–	dBm
880–915 MHz	WCDMA	–	–11	–	dBm
1710–1785 MHz	GSM1800	–	–16	–	dBm
1710–1785 MHz	WCDMA	–	–15	–	dBm
1850–1910 MHz	GSM1900	–	–17	–	dBm
1850–1910 MHz	WCDMA	–	–17	–	dBm
1880–1920 MHz	TD-SCDMA	–	–17	–	dBm
1920–1980 MHz	WCDMA	–	–17	–	dBm
2010–2025 MHz	TD-SCDMA	–	–18	–	dBm
2500–2570 MHz	WCDMA	–	–21	–	dBm
RX LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm

Table 33. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Spurious Emissions					
30 MHz–1 GHz		–	–95	–62	dBm
1–12.75 GHz		–	–70	–47	dBm
869–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

a. The Bluetooth reference level for the required signal at the Bluetooth chip port is 3 dB higher than the typical sensitivity level.

Table 34. LTE Specifications for Spurious Emissions

Parameter	Conditions	Typical	Unit
2500–2570 MHz	Band 7	–147	dBm/Hz
2300–2400 MHz	Band 40	–147	dBm/Hz
2570–2620 MHz	Band 38	–147	dBm/Hz
2545–2575 MHz	XGP Band	–147	dBm/Hz

Table 35. Bluetooth Transmitter RF Specifications[a]

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		–	12.0	–	dBm
QPSK TX power at Bluetooth		–	8.0	–	dBm
8PSK TX power at Bluetooth		–	8.0	–	dBm
Power control step	–	2	4	8	dB
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31	–20.0	dBm
|M – N| ≥ 2.5 MHz[b]		–	–43	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [c,d]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [d,e,f]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm
Out-of-Band Noise Floor[g]					
65–108 MHz	FM RX	–	–147	–	dBm/Hz
776–794 MHz	CDMA2000	–	–146	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–146	–	dBm/Hz
925–960 MHz	E-GSM	–	–146	–	dBm/Hz
1570–1580 MHz	GPS	–	–146	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–144	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–143	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–137	–	dBm/Hz

a. Unless otherwise specified, the specifications in this table apply at the chip output port, and output power specifications are with the temperature correction algorithm and TSSI enabled.
b. Typically measured at an offset of ±3 MHz.
c. The maximum value represents the value required for Bluetooth qualification as defined in the v4.1 specification.
d. The spurious emissions during Idle mode are the same as specified in Table 35.
e. Specified at the Bluetooth antenna port.
f. Meets this specification using a front-end band-pass filter.
g. Transmitted power in cellular and FM bands at the Bluetooth antenna port. See Figure 35 for location of the port.

Table 36. LTE Specifications for Out-of-Band Noise Floor

Parameter	Conditions	Typical	Unit
2500–2570 MHz	Band 7	–130	dBm/Hz
2300–2400 MHz	Band 40	–130	dBm/Hz
2570–2620 MHz	Band 38	–130	dBm/Hz
2545–2575 MHz	XGP Band	–130	dBm/Hz

Table 37. Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±8	±25	kHz
DH3 packet	–	±8	±40	kHz
DH5 packet	–	±8	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	155	175	kHz
10101010 sequence in payload[b]	115	140	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 38. BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402	–	2480	MHz
RX sense[a]	GFSK, 0.1% BER, 1 Mbps	–	–97	–	dBm
TX power[b]	–	–	8.5	–	dBm
Mod Char: delta f1 average	–	225	255	275	kHz
Mod Char: delta f2 max[c]	–	99.9	–	–	%
Mod Char: ratio	–	0.8	0.95	–	%

a. The Bluetooth tester is set so that Dirty TX is on.
b. BLE TX power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc.). The output is capped at 12 dBm. The BLE TX power at the antenna port cannot exceed the 10 dBm specification limit.
c. At least 99.9% of all delta F2 max. frequency values recorded over 10 packets must be greater than 185 kHz.

17. Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on device characterization results. Functional operation is not guaranteed outside of the specification limits provided in this section.

17.1 Core Buck Switching Regulator

Table 39. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	2.4	3.6	4.8[a]	V
PWM mode switching frequency	CCM, load > 100 mA VBAT = 3.6V.	–	4	–	MHz
PWM output current	–	–	–	370	mA
Output current limit	–	–	1400	–	mA
Output voltage range	Programmable, 30 mV steps. Default = 1.35V.	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static load, max. ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, C_{out} > 1.9 µF, ESL<200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak efficiency at 200 mA load, inductor DCR = 200 mΩ, VBAT = 3.6V, VOUT = 1.35V	–	85	–	%
PFM mode efficiency	10 mA load current, inductor DCR = 200 mΩ, VBAT = 3.6V, VOUT = 1.35V	–	77	–	%
Start-up time from power down	VDDIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	400	500	µs
External inductor	0603 size, 2.2 µH ±20%, DCR = 0.2Ω ± 25%	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, 4.7 µF ±20%, 10V	2.0[b]	4.7	10[c]	µF
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ±4.7 µF ±20%, 10V	0.67[b]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

a. The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
c. Total capacitance includes those connected at the far end of the active load.

17.2 3.3V LDO (LDO3P3)

Table 40. LDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = V_o + 0.2V = 3.5V dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8[a]	V
Output current	–	0.001	–	450	mA
Nominal output voltage, V_o	Default = 3.3V.	–	3.3	–	V
Dropout voltage	At max. load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	66	85	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, max. load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 3.3V, C_o = 4.7 µF, Max. load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	160	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V	1.0[b]	4.7	5.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with band gap) Ceramic, X5R, 0402, (ESR: 30m-200 mΩ), ± 10%, 10V. Not needed if sharing VBAT capacitor 4.7 µF with SR_VDDBATP5V.	–	4.7	–	µF

a. The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

17.3 CLDO

Table 41. CLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.2	–	200	mA
Output voltage, V_o	Programmable in 10 mV steps. Default = 1.2.V	0.95	1.2	1.26	V
Dropout voltage	At max. load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	13	–	µA
	200 mA load	–	1.24	–	mA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load regulation	Load from 1 mA to 300 mA	–	0.02	0.05	mV/mA
Leakage current	Power down	–	5	20	µA
	Bypass mode	–	1	3	µA
PSRR	@1 kHz, Vin ≥ 1.35V, C_o = 4.7 µF	20	–	–	dB
Start-up time of PMU	VDDIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO turn-on time	LDO turn-on time when rest of the chip is up.	–	140	180	µs
External output capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	1.1[a]	2.2	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

17.4 LNLDO

Table 42. LNLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. $V_{IN} = V_O + 0.15V = 1.35V$ (where $V_O = 1.2V$) dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	10	12	µA
	Max. load	–	970	990	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, 200 mA load	–	–	5	mV/V
Load regulation	Load from 1 mA to 200 mA: $V_{in} \geq (V_o + 0.12V)$	–	0.025	0.045	mV/mA
Leakage current	Power-down, junction temp. = 85°C	–	5	20	µA
Output noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60 35	–nV/$\sqrt{Hz}$
PSRR	@1 kHz, $V_{in} \geq (V_o + 0.15V)$, C_o = 4.7 µF	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	140	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[a]	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

18. System Power Consumption

Note: The values in this data sheet are design goals and are subject to change based on device characterization.Unless otherwise stated, these values apply for the conditions specified in Table 28.

18.1 WLAN Current Consumption

Table 43 shows typical currents consumed by the CYW4343W's WLAN section. All values shown are with the Bluetooth core in Reset mode with Bluetooth off.

18.1.1 2.4 GHz Mode

Table 43. 2.4 GHz Mode WLAN Power Consumption

Mode	Rate	VBAT = 3.6V, VDDIO = 1.8V, TA 25°C	
		VBAT (mA)	Vio (µA)
Sleep Modes			
Leakage (OFF)	N/A	0.0035	0.08
Sleep (idle, unassociated) [a]	N/A	0.0058	80
Sleep (idle, associated, inter-beacons) [b]	Rate 1	0.0058	80
IEEE Power Save PM1 DTIM1 (Avg.) [c]	Rate 1	1.05	74
IEEE Power Save PM1 DTIM3 (Avg.) [d]	Rate 1	0.35	86
IEEE Power Save PM2 DTIM1 (Avg.) [c]	Rate 1	1.05	74
IEEE Power Save PM2 DTIM3 (Avg.) [d]	Rate 1	0.35	86
Active Modes			
Rx Listen Mode [e]	N/A	37	12
Rx Active (at –50dBm RSSI) [f]	Rate 1	39	12
	Rate 11	40	12
	Rate 54	40	12
	Rate MCS7	41	12
Tx [f]	Rate 1 @ 20 dBm	320	15
	Rate 11 @ 18 dBm	290	15
	Rate 54 @ 15 dBm	260	15
	Rate MCS7 @ 15 dBm	260	15

a. Device is initialized in Sleep mode, but not associated.
b. Device is associated, and then enters Power Save mode (idle between beacons).
c. Beacon interval = 100 ms; beacon duration = 1 ms @ 1 Mbps (Integrated Sleep + wakeup + beacon).
d. Beacon interval = 300 ms; beacon duration = 1 ms @ 1 Mbps (Integrated Sleep + wakeup + beacon).
e. Carrier sense (CCA) when no carrier present.
f. Tx output power is measured on the chip-out side; duty cycle =100%. Tx Active mode is measured in Packet Engine mode (pseudo-random data)

18.2 Bluetooth Current Consumption

The Bluetooth current consumption measurements are shown in Table 44.

Note:

- The WLAN core is in reset (WLAN_REG_ON = low) for all measurements provided in Table 44.
- The BT current consumption numbers are measured based on GFSK TX output power = 10 dBm.

Table 44. Bluetooth BLE Current Consumption

Operating Mode	VBAT (VBAT = 3.6V) Typical	VDDIO (VDDIO = 1.8V) Typical	Units
Sleep	6	150	µA
Standard 1.28s Inquiry Scan	193	162	µA
500 ms Sniff Master	305	172	µA
DM1/DH1 Master	23.3	–	mA
DM3/DH3 Master	28.4	–	mA
DM5/DH5 Master	29.1	–	mA
3DH5/3DH5 Master	25.1	–	mA
SCO HV3 Master	11.8	–	mA
BLE Scan[a]	187	164	µA
BLE Adv. – Unconnectable 1.00 sec	93	163	µA
BLE Connected 1 sec	71	163	µA

a. No devices present. A 1.28 second interval with a scan window of 11.25 ms.

19. Interface Timing and AC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 26 and Table 28. Functional operation outside of these limits is not guaranteed.

19.1 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 36 and Table 45.

Figure 36. SDIO Bus Timing (Default Mode)

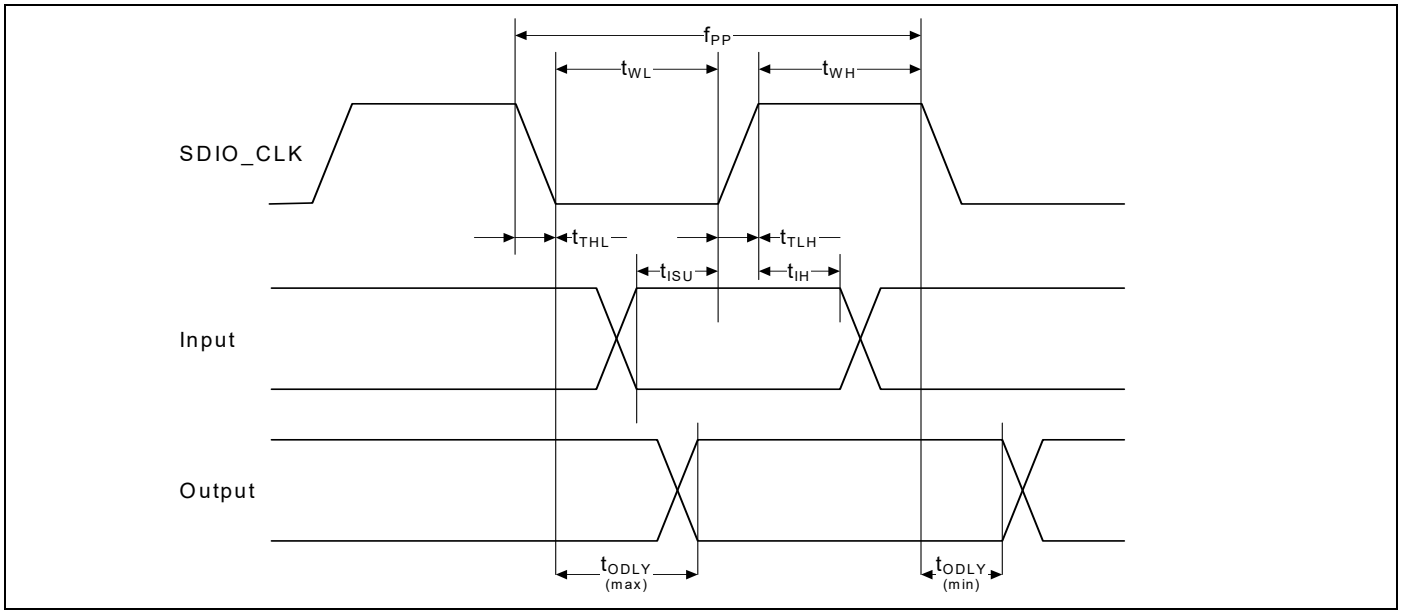


Table 45. SDIO Bus Timing [a] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency—Data Transfer mode	fPP	0	–	25	MHz
Frequency—Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock fall time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time—Data Transfer mode	tODLY	0	–	14	ns
Output delay time—Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40 pF load on command and data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

19.2 SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 37 and Table 46.

Figure 37. SDIO Bus Timing (High-Speed Mode)

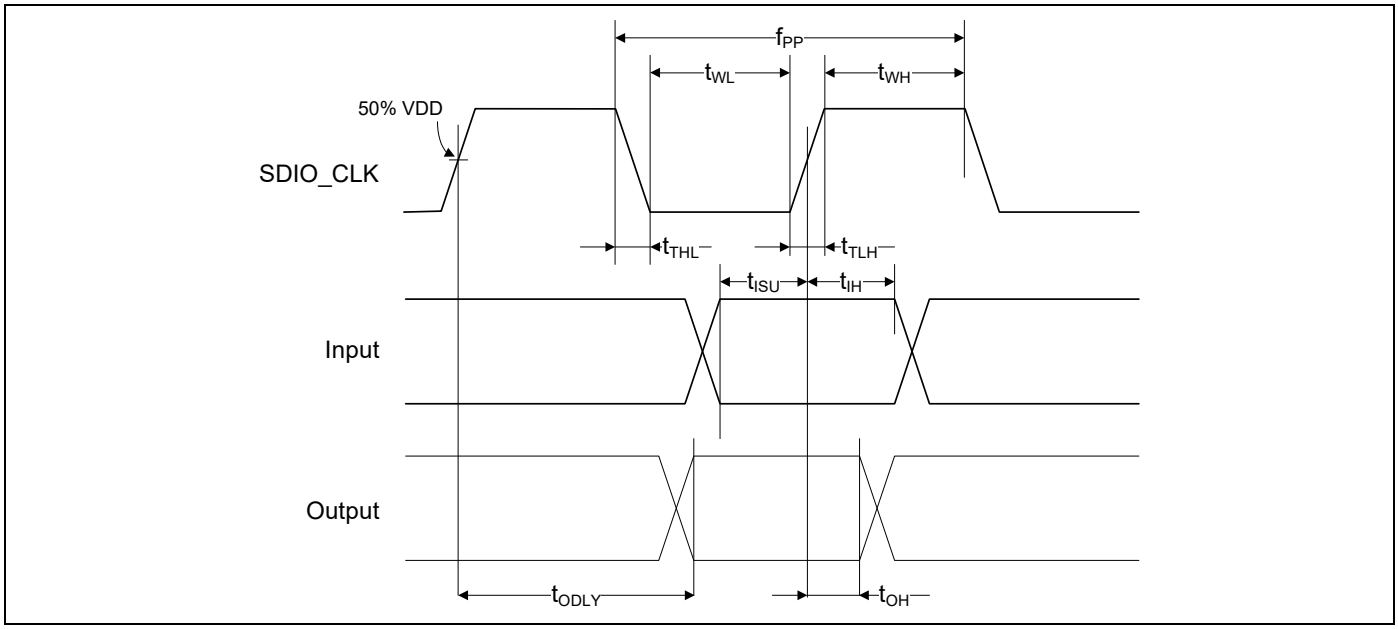


Table 46. SDIO Bus Timing [a] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock fall time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	–	–	ns
Input hold time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on command and data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

19.3 JTAG Timing

Table 47. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

20. Power-Up Sequence and Timing

20.1 Sequencing of Reset and Regulator Control Signals

The CYW4343W has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 38 through Figure 41). The timing values indicated are minimum required values; longer delays are also acceptable.

Note:

- The WL_REG_ON and BT_REG_ON signals are OR'ed in the CYW4343W. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the CYW4343W regulators.
- The CYW4343W has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold (see Table 28). Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.
- VBAT and VDDIO should not rise faster than 40 µs. VBAT should be up before or at the same time as VDDIO. VDDIO should not be present first or be held high before VBAT is high.

20.1.1 Description of Control Signals

- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4343W regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW4343W regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note: For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

20.1.2 Control Signal Timing Diagrams

Figure 38. WLAN = ON, Bluetooth = ON

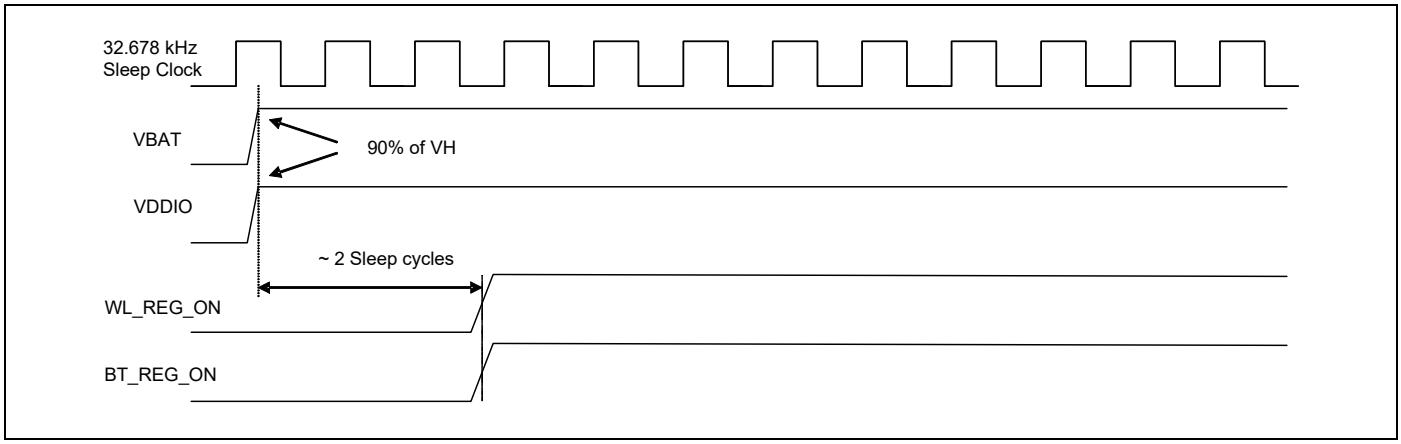


Figure 39. WLAN = OFF, Bluetooth = OFF

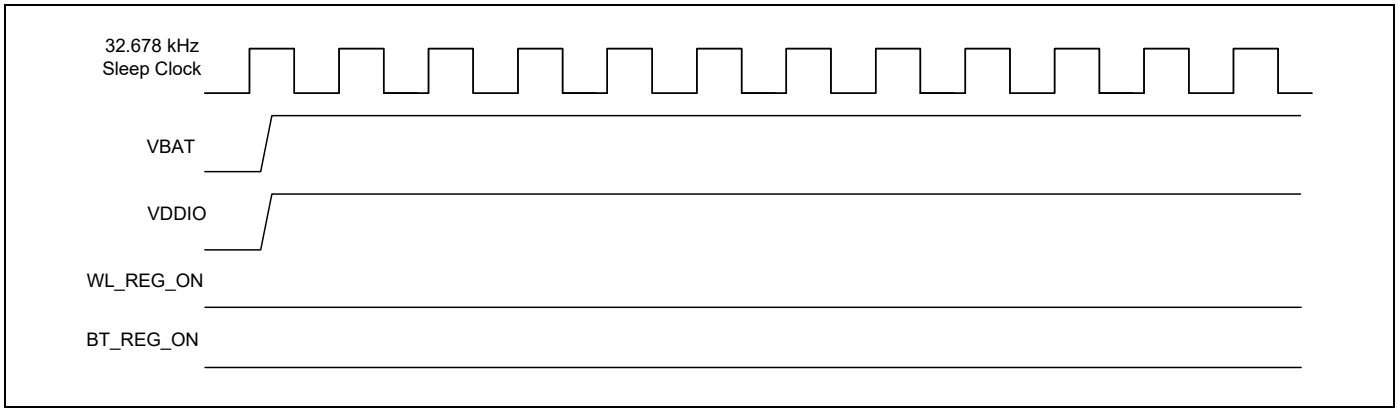


Figure 40. WLAN = ON, Bluetooth = OFF

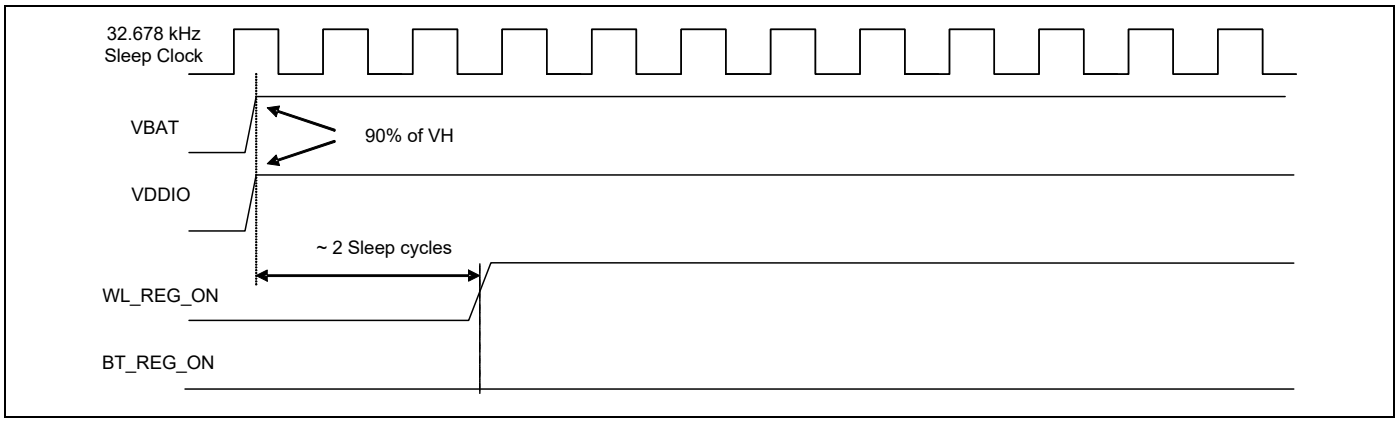
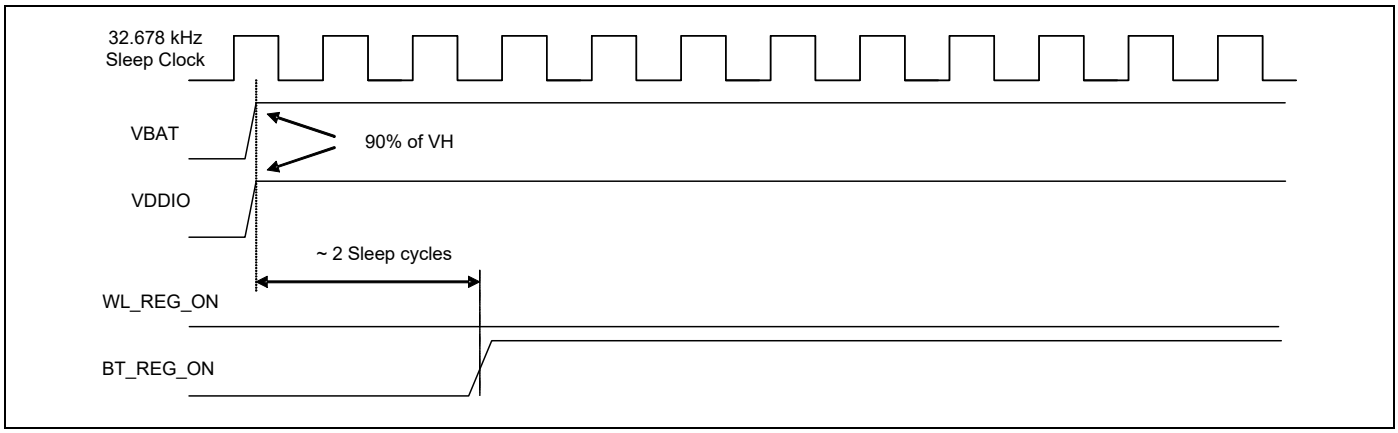


Figure 41. WLAN = OFF, Bluetooth = ON



21. Package Information

21.1 Package Thermal Characteristics

Table 48. Package Thermal Characteristics[a]

Characteristic	Value in Still Air
θ_{JA} (°C/W)	53.11
θ_{JB} (°C/W)	13.14
θ_{JC} (°C/W)	6.36
Ψ_{JT} (°C/W)	0.04
Ψ_{JB} (°C/W)	14.21
Maximum Junction Temperature T_j (°C)[b]	125
Maximum Power Dissipation (W)	1.2

a. No heat sink, TA = 70°C. This is an estimate based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm x 114.3 mm x 1.6 mm) and P = 1.2W continuous dissipation.
b. Absolute junction temperature limits maintained through active thermal monitoring and dynamic TX duty cycle limiting.

21.1.1 Junction Temperature Estimation and PSI Versus Theta$_{jc}$

Package thermal characterization parameter PSI-JT (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

$$T_J = T_T + P \times \Psi_{JT}$$

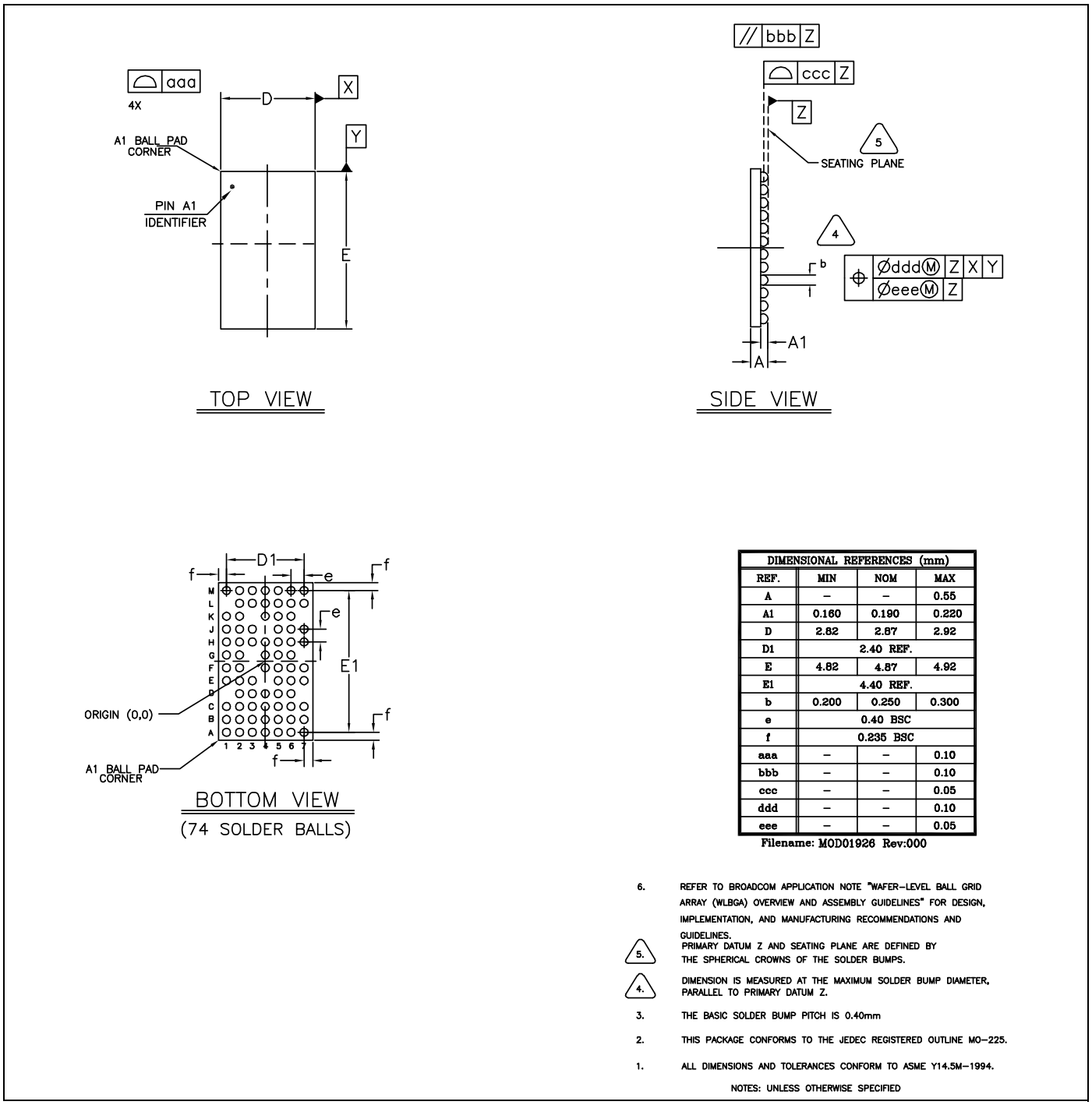
Where:

- T_J = junction temperature at steady-state condition, °C
- T_T = package case top center temperature at steady-state condition, °C
- P = device power dissipation, Watts
- Ψ_{JT} = package thermal characteristics (no airflow), °C/W

22. Mechanical Information

Figure 42 shows the mechanical drawing for the CYW4343W WLBGA package.

Figure 42. 74-Ball WLBGA Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.55
A1	0.160	0.190	0.220
D	2.82	2.87	2.92
D1		2.40 REF.	
E	4.82	4.87	4.92
E1		4.40 REF.	
b	0.200	0.250	0.300
e		0.40 BSC	
f		0.235 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

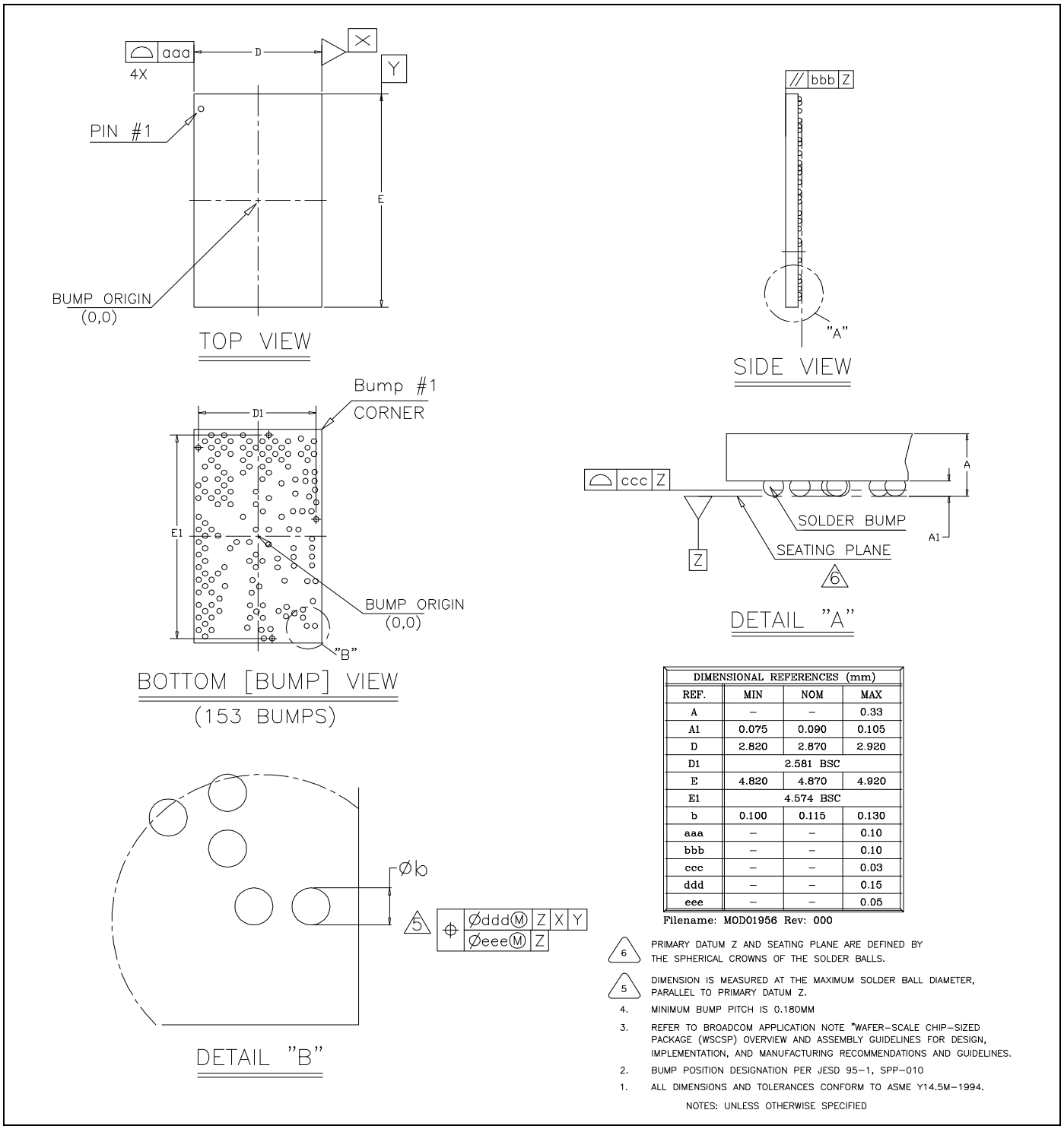
Filename: MOD01926 Rev:000

6. REFER TO BROADCOM APPLICATION NOTE "WAFER-LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.
3. THE BASIC SOLDER BUMP PITCH IS 0.40mm
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 43 shows the mechanical drawing for the CYW4343W WLCSP package. Figure 44 shows the WLCSP keep-out areas.

Figure 43. 153-Bump WLCSP Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.33
A1	0.075	0.090	0.105
D	2.820	2.870	2.920
D1		2.581 BSC	
E	4.820	4.870	4.920
E1		4.574 BSC	
b	0.100	0.115	0.130
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.03
ddd	–	–	0.15
eee	–	–	0.05

Filename: MOD01956 Rev: 000

6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
4. MINIMUM BUMP PITCH IS 0.180MM
3. REFER TO BROADCOM APPLICATION NOTE "WAFER-SCALE CHIP-SIZED PACKAGE (WSCSP) OVERVIEW AND ASSEMBLY GUIDELINES FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.
2. BUMP POSITION DESIGNATION PER JESD 95-1, SPP-010
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Note: No top-layer metal is allowed in the keep-out areas

Note: A DXF file containing WLBGA keep-outs can be imported into a layout program. Contact your Cypress FAE for more information.

Figure 44. WLCSP Package Keep-Out Areas—Top View with the Bumps Facing Down

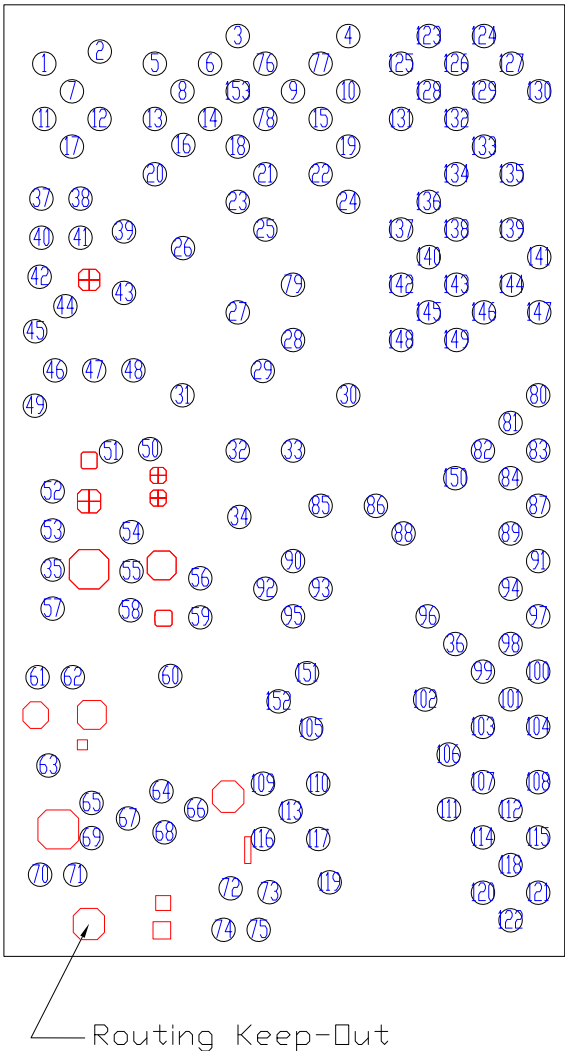
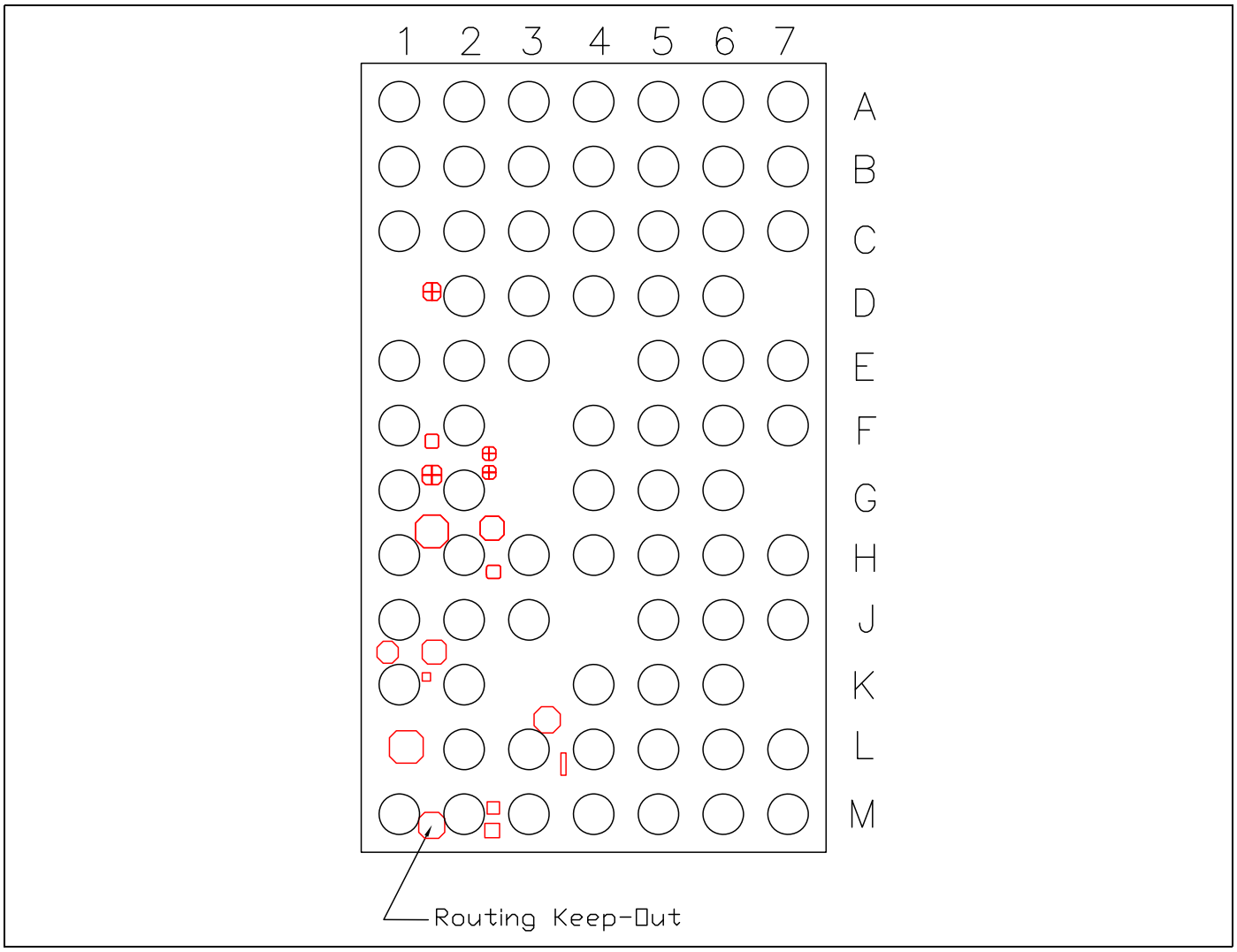


Figure 45. WLBGA Package Keep-Out Areas—Top View with the Bumps Facing Down



23. Ordering Information

Table 49. Part Ordering Information

Part Number [a]	Package	Description	Operating Ambient Temperature
CYW4343WKUBG	74-ball WLBGA halogen-free package (4.87 mm x 2.87 mm, 0.40 pitch)	2.4 GHz single-band WLAN IEEE 802.11n + BT 4.1	–30°C to +70°C
CYW4343WKWBG	153-bump WLCSP	2.4 GHz single-band WLAN IEEE 802.11n + BT 4.1	–30°C to +70°C

a. Add “T” to the end of the part number to specify “Tape and Reel.”

24. Additional Information

24.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

24.2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Document History Page

Document Title: CYW4343W Single-Chip 802.11 b/g/n MAC/Baseband/Radio with Bluetooth 4.1 Document Number: 002-14797			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	-	03/10/2014	4343W-DS100-R Initial release
*A	-	04/18/2014	4343W-DS101-R Refer to the earlier release for detailed revision history.
*B	-	06/09/2014	4343W-DS102-R Refer to the earlier release for detailed revision history
*C	-	09/05/2014	4343W-DS103-R Refer to the earlier release for detailed revision history
*D	-	10/03/2014	4343W-DS104-R Refer to the earlier release for detailed revision history
*E	-	01/12/2015	4343W-DS105-R Refer to the earlier release for detailed revision history
*F	-	07/01/2015	4343W-DS106-R Updated: Table 24, “I/O States”. Table 27, “ESD Specifications”. Table 30, “WLAN 2.4 GHz Receiver Performance Specifications”. Table 31, “WLAN 2.4 GHz Transmitter Performance Specifications”. Table 43, “2.4 GHz Mode WLAN Power Consumption”. Table 49, “Part Ordering Information”
*G	-	08/24/15	4343W-DS107-R Updated: Figure3: “Typical Power Topology (1 of 2), and Figure4: “Typical Power Topology (2 of 2),. Table 2:“Crystal Oscillator and External Clock Requirements and Performance”. Table23:“I/O States”.
*H	5445248	10/19/2016	Migrated to Cypress template format Added Cypress part numbering scheme
*I	5600195	01/12/2017	Removed FM Receiver and wireless Charging from the topic. Removed FM from Figure 1, Figure 2, Figure 3, Figure 4. Removed “8.4 Generic SPI mode” and “SPI Protocol”. Removed FM from Section 7: “Bluetooth Subsystem Overview” on page 30. Removed “8.5.1.FM power Management” and “8.6.3 FM over Bluetooth”. Updated Figure 32 (removed SPI). Removed Section 18: FM Receiver Specifications”. Removed FMRX from the Ordering Information.
*J	6947362	08/18/2020	Updated Figure 1 with SPI. Updated Figure 2 with gSPI. Updated Table 5 with gSPI Mode. Added Generic SPI Mode, SPI Protocol, and gSPI Host-Device Handshake. Updated Figure 32 with SPI.

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