XDPS2221 PFC + Hybrid-Flyback - Combo Controller

Datasheet

Product Highlights

- Digital combo controller for PFC-boost and dc-dc hybrid-flyback in DSO-14 (150mil) package
- Novel ZVS hybrid-flyback (asymmetrical half-bridge) topology for ultra-high system efficiency
- Integrated gate drivers supporting GaN and Si switches
- 600V high voltage start-up cell for fast VCC charging and active X-capacitor discharge
- Burst mode operation control for lowest no-load stand-by power
- Adaptive PFC bus voltage and PFC enable/disable control to maximize average and light load efficiency
- Configurable parameters for protection modes and system performance
- Pb-free lead plating, halogen-free (according to IEC61249-2-21), RoHS compliant

PFC control

- Configurable PFC QRM operation for improved average efficiency
- Pulse skipping for improved light load efficiency
- Automatic PFC disable/enable-control depending on operating conditions
- Adaptive PFC bus voltage level following operating conditions

Hybrid-flyback control

- Peak current mode control for robust and fast input and load control
- ZVS operation of high-side and low-side switch (with ZVS pulse insertion in DCM)
- Configurable multimode operation for improved average and light load efficiency

Description

The XDPS2221 PWM controller is a highly integrated device combining a multimode ac-dc PFC controller and a multimode dc-dc hybrid-flyback controller. The integration of PFC and hybrid-flyback into a single package enables the reduction of external bill of material components and optimizes the system performance by harmonized operation of the two stages.

Ordering Information

Product Name	Marking	Ordering Code	Firmware version	Package
XDPS2221	XDPS2221	SP005630569	3.1.1	PG-DSO-14

Potential Applications

Ultra high power density chargers / adapters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Innovations protected by patents and patent applications

Please read the sections "Important notice" and "Warnings" at the end of this document

Table of contents

1 Pin Configuration and Functionality

The pin configuration is shown in the figure below and the functions are described in the following table.

Table 1 **Pin Definitions and Functions**

Symbol	Pin	Type	Function
PFCGD	1	O	**PFC gate driver** This pin drives the PFC transistor via a gate resistor.
CS	2	I	**Hybrid-flyback current sense** Input pin for current sensing during the hybrid-flyback high-side gate driver turn-on phase.
VCC	3	I	**Power supply** This pin supplies the IC. During start-up VCC is supplied from the AC via the HV-pin, while during normal operation VCC is supplied from the auxiliary winding to the hybrid-flyback stage.
GND	4	O	Ground level of the IC for supply voltage, gate drive and sense signals.
ZCD	5	I	**Hybrid-flyback zero crossing detection** This pin provides zero crossing detection after low-side gate driver turned off and during pause phase in burst mode. Furthermore the reflected output voltage at the auxiliary winding can be measured during low-side gate driver turn-on phase.
PFCVS	6	I	**PFC bus voltage sense** This pin is connected to a high impedance resistor divider from the PFC controller output for bus voltage sensing.
HV	7	I	**High voltage input** The HV pin is connected to the input AC voltage. An internal HV startup-cell is used for initial VCC charging, AC monitoring and X-capacitor discharge.
MFIO	8	I	**Multi-functional Input Output** This pin is connected to GND through an external NTC resistor used to detect ambient temperature. Furthermore, UART communication for parameter configuration and failure mode reporting is provided by this pin.
FB	9	I	**Feedback** This pin receives feedback from the secondary side via an optocoupler.
PFCCS	10	I	**PFC current sense and PFC zero crossing detection** This pin is configured for PFC current sensing in combination with zero crossing detection of the PFC choke current.
LSGD	11	O	**Hybrid-flyback low-side gate driver** This pin drives the low-side transistor of the hybrid-flyback half-bridge via a resistor.
HSGND	12	I	**High-side Ground** Ground reference node for hybrid-flyback floating high-side driver domain.

(table continues...)

Table 1 (continued) Pin Definitions and Functions

Symbol	Pin	Type	Function
HSVCC	13	I	**High-side power supply** Power supply input for hybrid-flyback floating high-side driver domain.
HSGD	14	O	**High-side gate driver** This pin drives the high-side transistor of the hybrid-flyback half-bridge from the floating driver domain via a resistor.

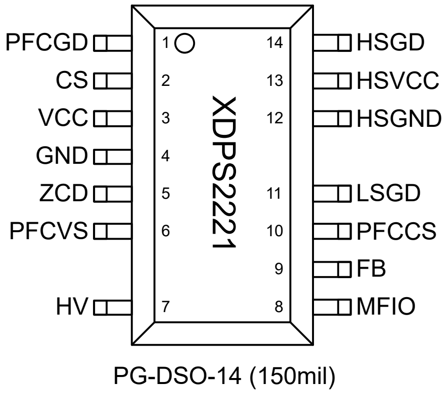

Figure 1 Pin configuration

2 Representative Block Diagram

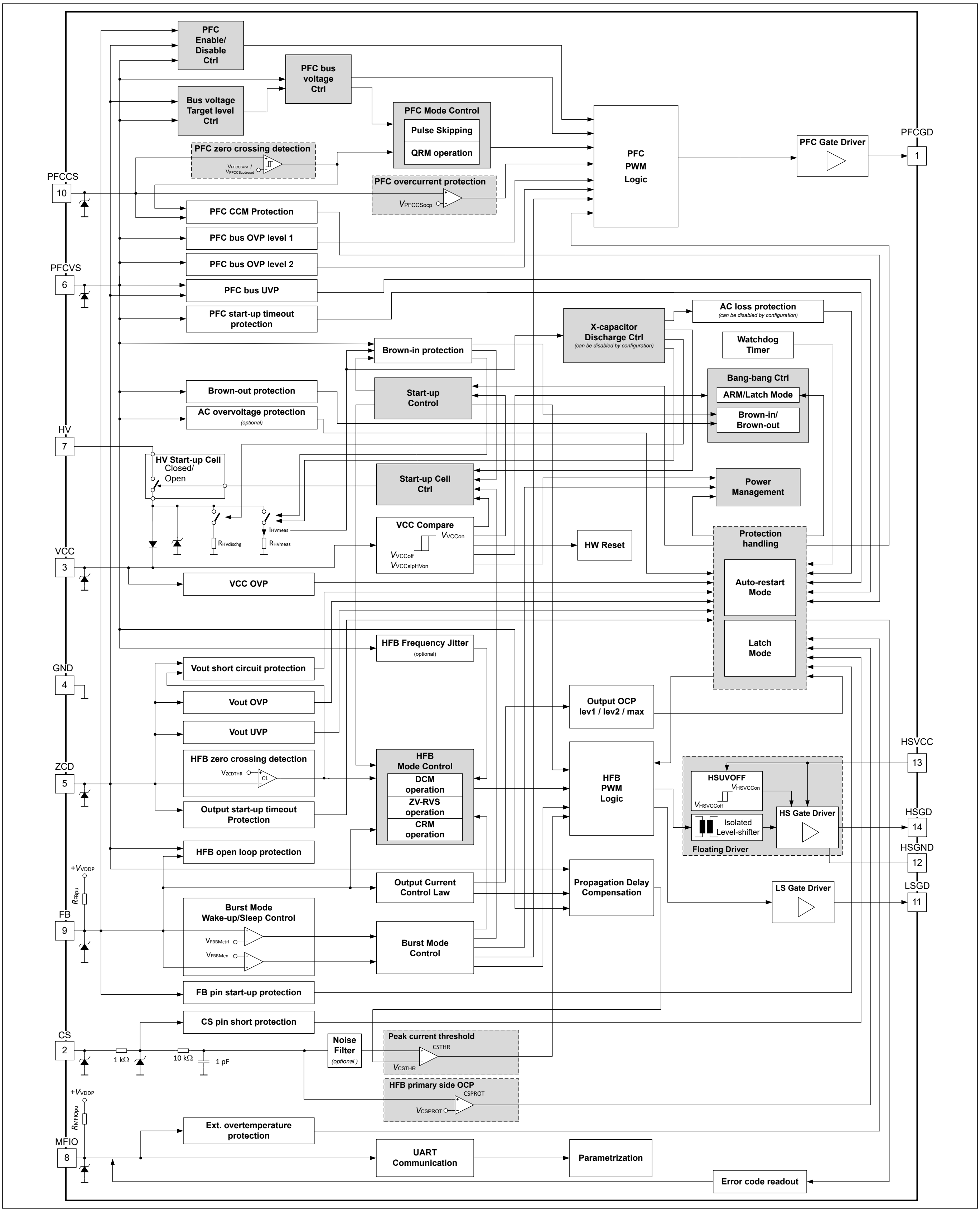

Figure 2 Block diagram

3 Introduction

The XDPS2221 PWM controller is a highly integrated device combining a multimode ac-dc PFC controller and a multimode dc-dc hybrid-flyback controller. The integration of PFC and hybrid-flyback into a single controller enables reduction of external parts and optimizes performance by joint operation of the two stages. It is meant to be used in USB-PD chargers / adapters with wide output voltage up to 28 V.

The system efficiency can further be increased using Infineon CoolMOS^{TM}, CoolGaN^{TM} and OptiMOS^{TM} transistors. Below a typical application schematics in a USB-PD application are depicted.

Figure 3 shows the potential application schematic using CoolGaN^{TM} and OptiMOS^{TM} transistors for highest efficiency and power density.

Figure 4 shows the potential application schematic using CoolMOS^{TM} and OptiMOS^{TM} transistors.

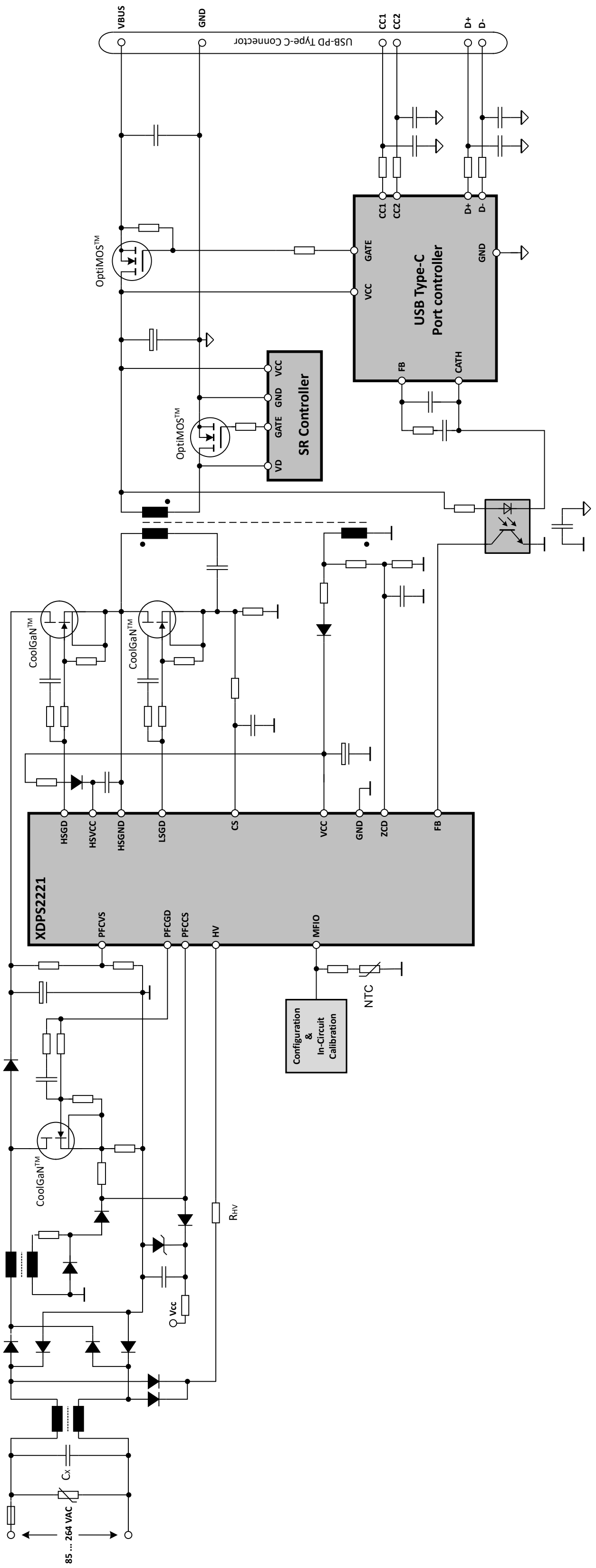

Figure 3 Typical application in combination with CoolGaN^{TM} transistors

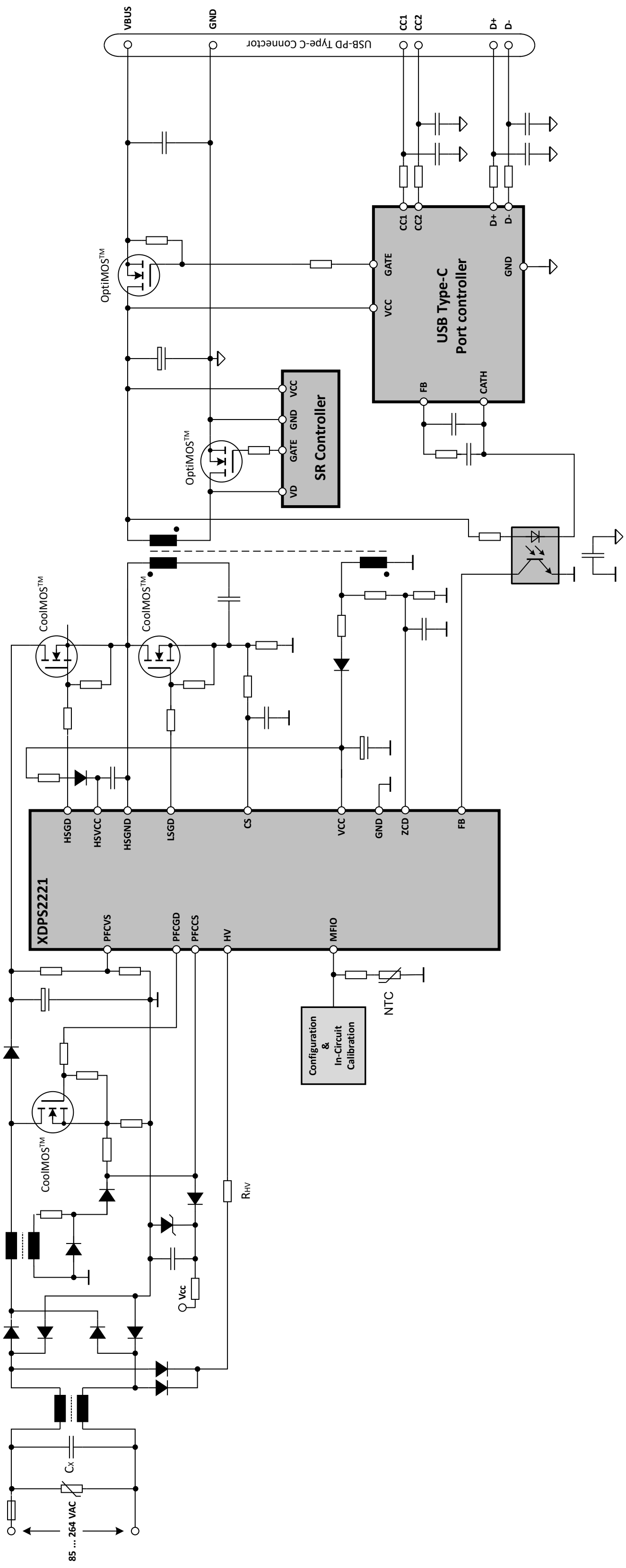

Figure 4 Typical application in combination with CoolMOS^{TM} transistors

4 Functional description

4.1 Power-supply and high voltage start-up cell management

The power supply management ensures a reliable and robust IC operation. Depending on the operation mode of the control IC, the power supply management unit runs in different ways for VCC supply, which are described as in the sequel.

4.1.1 VCC capacitor charge-up and start-up sequence

At VCC start-up the capacitor C_{VCC} is charged by the internal HV start-up cell via HV pin (see Figure 5). The internal HV start-up cell is turned on for V_{VCC} lower than the IC deactivation voltage threshold V_{VCCoff}. Once the voltage at pin VCC exceeds the threshold V_{VCCon} at time t0 the HV start-up cell is turned off and the IC is starting up (see Figure 6).

The IC operation is started at time t1 and the start-up conditions are validated afterwards.

Following conditions need to be fulfilled to start the hybrid-flyback operation at time t2 (hybrid-flyback switching is indicated by signal V_{HBGD}):

1. Two-level brown-in condition with $V_{ACrms} > V_{ACrmsbi}$ and $V_{bus} > V_{busbi}$ (see Chapter 4.5.2.4))
2. No input overvoltage with $V_{bus} < V_{busACovp}$ (see Chapter 4.5.2.9)
3. Feedback signal out of regulation range with $V_{FB} > V_{FBBMctrl}$
4. No overtemperature condition with $R_{MFIO} > R_{MFIOOTPrel}$. (see Chapter 4.5.2.18)

The conditions need to be met within the time period t_{HVbito}. With hybrid-flyback switching, the the external VCC self-supply takes over the IC supply. In case one of those conditions is not met the IC enters bang-bang during brown-in phase (see Chapter 4.1.2).

Note: In the typical application the output voltage target value is set by the USB-PD controller. At start-up, no load is applied and the target value is first set by the USB-PD controller to e.g. $V_{out,set1} = 5$ V *and only after having reached a stable output voltage condition the USB-PD controller activates the load and sets the proper output voltage required by the attached device.*

PFC operation depends on operating conditions and might not be required at start-up. Hybrid-flyback operation starts first, if required, PFC operation comes up afterwards. Figure 6 shows a situation with an output voltage request from USB-PD controller with $V_{out,set2} > V_{out,set1}$ after a while. In this case example operation is started at t_4.

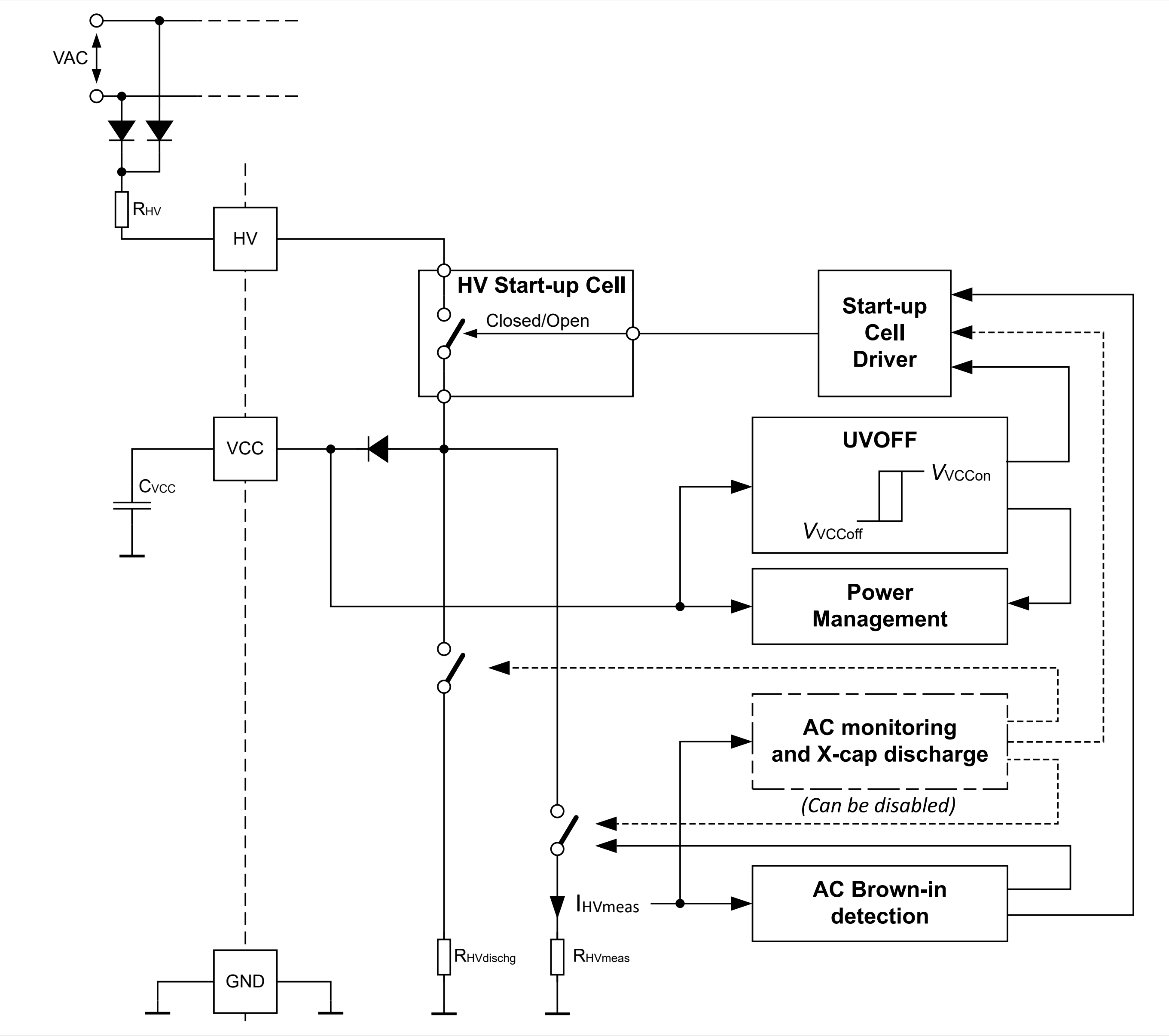

Figure 5 HV control for start-up, brown-in detection and X-capacitor discharge

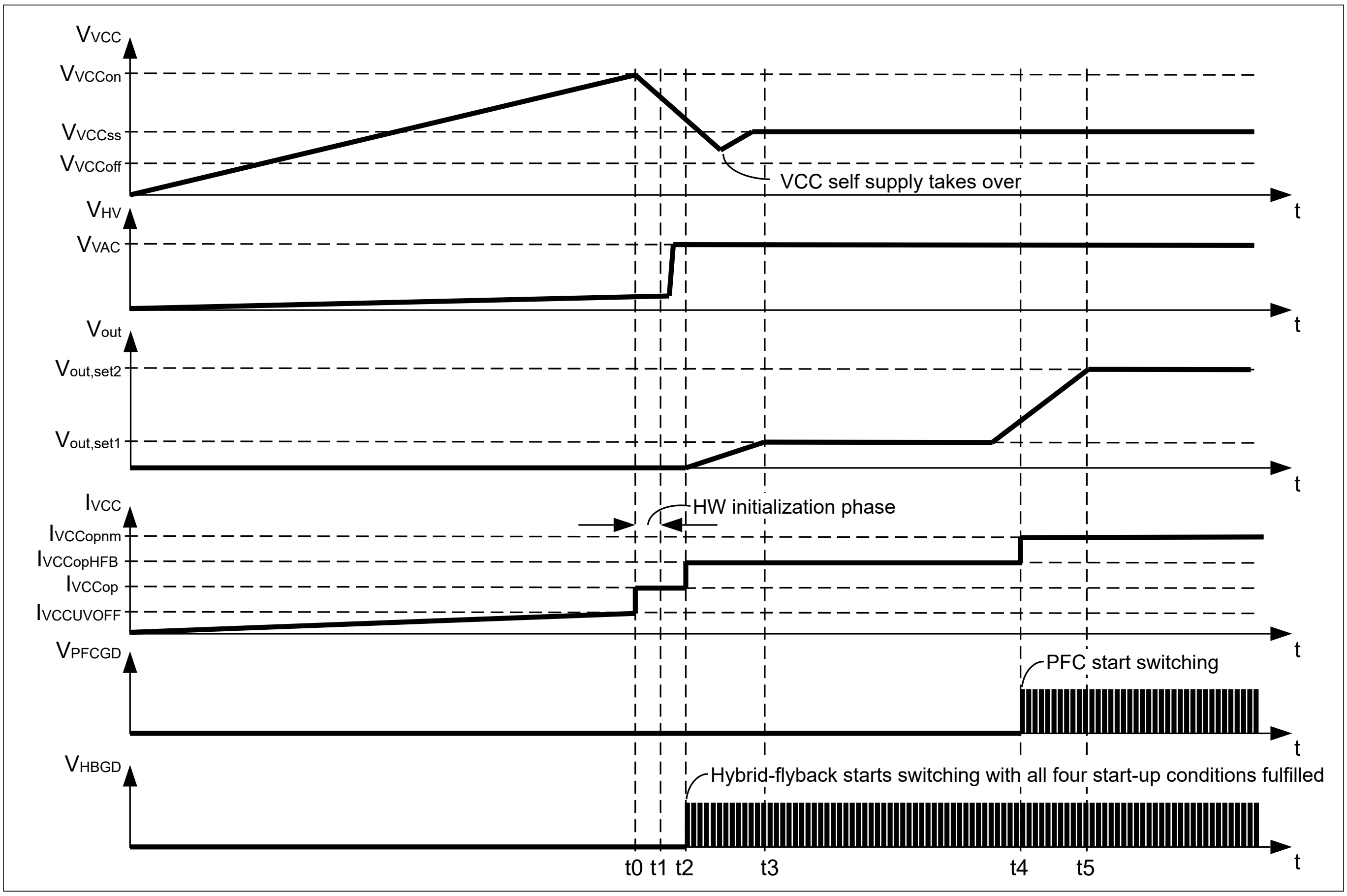

Figure 6 Typical start-up sequence

4.1.2 Bang-bang mode operation during brown-in phase

In order to support a fast activation as soon as brown-in condition is fulfilled, the VCC voltage is kept at a high level. A bang-bang mode operation for the start-up check phase is ensuring a high VCC level.

For example, after a brown-out event the IC enters a sleep mode with reduced current consumption I_{VCCBB}. The HV start-up cell turns on and tries to charge up the VCC voltage to the threshold V_{VCCon}. When AC input voltage comes back V_{VCC} can reach V_{VCCon} and the IC gets active for brown-in detection for a short time. If AC input voltage is high enough the IC detects the brown-in condition.

4.1.3 Bang-bang mode during protection mode operation

The bang-bang mode triggered by protection supports an IC operation during the latched and auto-restart operation (see Chapter 4.5.1). It controls the HV start-up cell by turning off at VCC pin threshold V_{VCCon} and turning on after a time period $t_{ARMbase}$ (see Figure 7). In auto-restart mode a system restart happens after the auto-restart time t_{arm} is expired. In latched operation a mode reset can only be achieved by disconnecting the AC line. A HW reset is taking place once the VCC voltage drops below the threshold V_{VCCoff}.

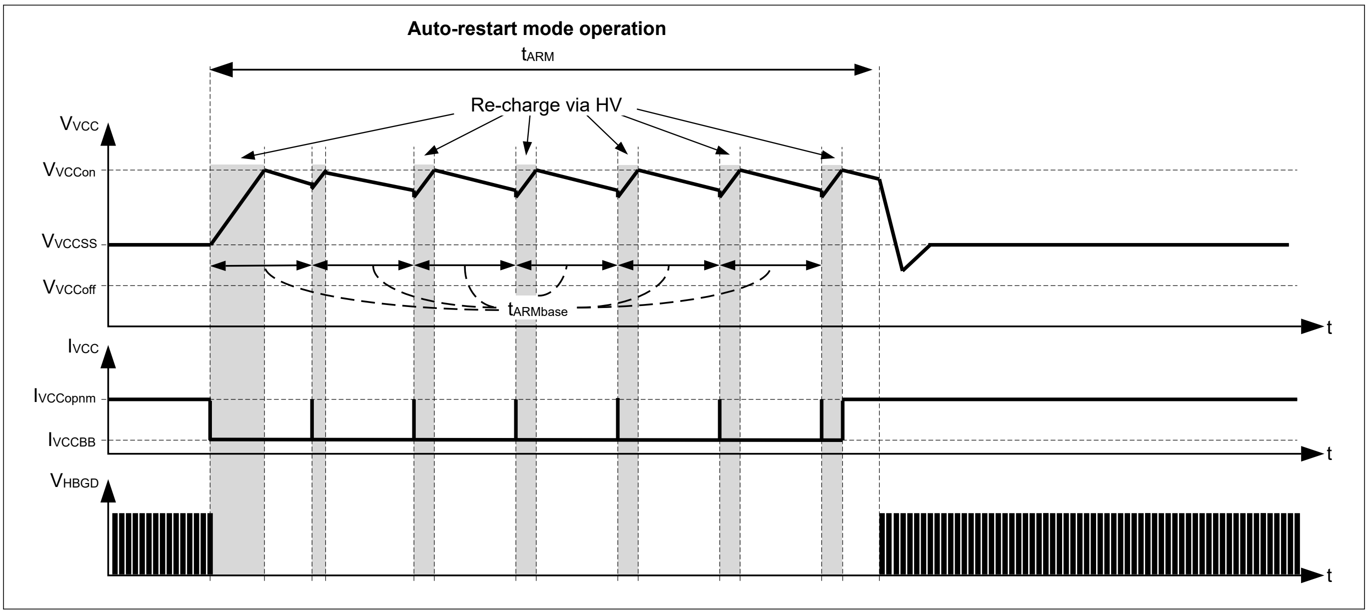

Figure 7 **Auto-restart mode operation**

4.1.4 VCC supply during burst mode (BM) operation

During burst mode operation the IC enters repeatedly a power saving mode, in which the IC current consumption is reduced to $I_{VCCBMpsm}$. During the burst active time, VCC should be supplied externally from the auxiliary winding.

The HV start-up cell can be configured in burst mode operation to re-charge VCC in case the external VCC cannot be guaranteed and VCC falls below $V_{VCCslpHVon}$. Note, that this operation will result in a higher input power consumption.

In burst-mode the controller can also be configured to use the HV start-up cell to support VCC supply. When enabled and the VCC voltage drops below the threshold $V_{VCCslpHVon}$, the HV start-up cell is activated and charges the VCC capacitor.

4.1.5 X-capacitor discharge

IEC 62368-1 safety standard requires the X-capacitors to be discharged below 60 V within two seconds once AC line is lost. The IC offers means for detection of AC loss and active X-capacitor discharge. This AC monitoring and X-capacitor discharge functionality can be enabled or disabled by configuration and is enabled by default. If enabled, it can eliminate the need of a passive resistor network parallel to the X-capacitor. In case of an AC voltage loss, the controller ensures active input capacitor discharge via the high voltage startup-cell. The high voltage start-up cell is available at pin HV which needs to be connected to line and neutral mains terminals via two separate diodes and a series resistor R_{HV} (see Figure 3).

In case it is enabled, the controller ensures active input capacitor discharge via the HV startup-cell within $t_{XCapdischg}$.

As soon as an AC unplug event is detected the HV start-up cell is activated and the input capacitors are discharged via HV pin through external and internal HV-resistors R_{HV} and $R_{HVdischrg}$ respectively (see Figure 5).

The discharge time for a given X-capacitor is determined by the size of the total resistance placed in series to the pin HV. The IC supports a component range determining this maximum discharge time $t_{XCapdischg}$. With X-capacitor discharge functionality enabled, a safe X-capacitor discharge is given with any combination of X-capacitor and resistor given in Table 2 for AC input voltages as specified in Table 3.

Table 2 **X-capacitor discharge component range**

Parameter	Min.	Max.	Unit	Remarks
Total capacitance of all X-capacitors	0.1	2.0	µF	Represented by C_X in Figure 3

(table continues...)

Table 2 (continued) X-capacitor discharge component range

Parameter	Min.	Max.	Unit	Remarks
Total external discharge resistance	48	54	kΩ	Represented by R_{HV} in Figure 3

Table 3 AC input voltage range and ratings for reliable AC detection

Parameter		Min.	Max.	Unit
Low line	Input voltage	90	150	$V_{ac,rms}$
	Frequency 1	47	53	Hz
	Frequency 2	57	63	Hz
High line	Input voltage	180	264	$V_{ac,rms}$
	Frequency 1	47	53	Hz
	Frequency 2	57	63	Hz

4.2 PFC control

The PFC controller turns on and off the PFC gate driver PFCGD so that a desired bus voltage V_{bus} is maintained while the AC input current I_{AC} follows the instantaneous line input voltage V_{AC} resulting in high power factor and low harmonic content. The operation mode is based on quasi-resonant operation mode (QRM), thus critical conduction mode, but with valley switching and valley skipping. The oscillation of the switch voltage $V_{PFC,ds}$ after choke current demagnetization is detected via an integrated zero crossing detection (ZCD) mechanism. The ZCD-function is combined with a PFC over-current protection at pin PFCCS. Figure 8 shows the PFC circuit arrangement including the AC input stage and the PFC control part of the IC.

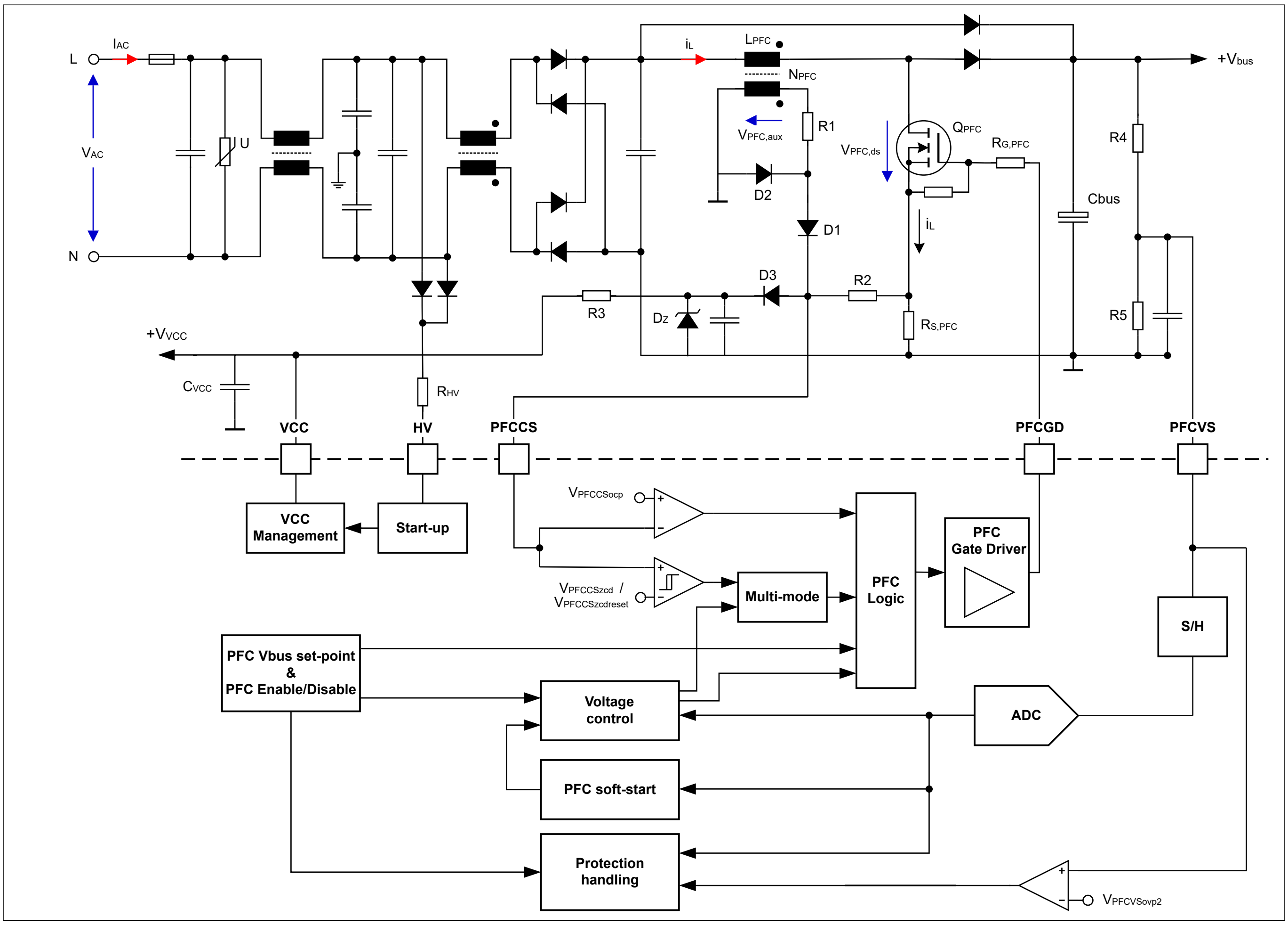

Figure 8 QRM-PFC circuit arrangement and associated PFC control

The PFC controller is operating in quasi-resonant mode (QRM) with valley switching. Typical waveforms are depicted in Figure 9. In the shown case, the PFC is turned on in the third valley.

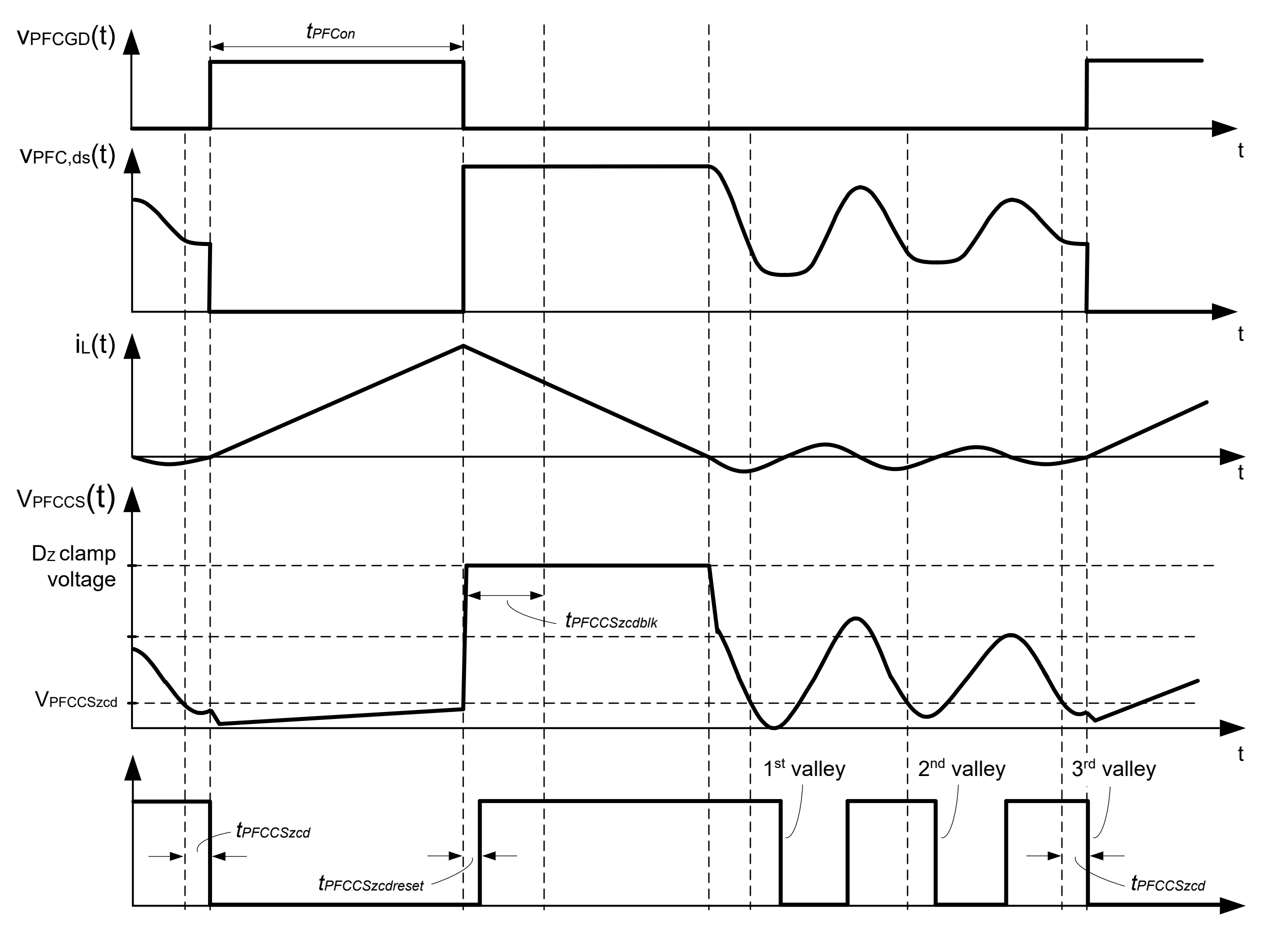

Figure 9 PFC switching cycle with transistor turn-on in the 3rd valley (QRM3)

4.2.1 Combined current sense (CS) and zero crossing detection (ZCD) function

The PFC stage uses a combined current sense (CS) and zero crossing detection (ZCD) functionality at pin PFCCS. During the PFC gate driver on-time the pin acts as a current sense (CS), while during the gate driver off-time the pin acts as a zero-crossing-detector (ZCD) for valley switching. Please refer to Figure 8 for the related circuitry for ZCD and CS.

Valley detection is done through an external circuit connected to the auxiliary winding of the PFC inductor. A hysteretic comparator with a lower threshold of $V_{PFCCSzcd}$ for falling edges and a upper threshold $V_{PFCCSzcdreset}$ for rising edges of the signal at PFCCS is used. A ZCD event is triggered in case V_{PFCCS} falls below the threshold $V_{PFCCSzcd}$. In case the target valley is reached, the gate driver output PFCGD only goes high after the delay time $t_{PFCCSzcd}$. However, a (new) ZCD event can only be detected after the voltage at PFCCS was above the upper comparator threshold $V_{PFCCSzcdreset}$ for longer than the configurable filter and delay time $t_{PFCCSzcdreset}$. For ringing suppression due to switching, the ZCD signal is blanked for $t_{PFCCSzcdblk}$ after PFGGD falling edge. The signal showing the hysteretic comparator output in Figure 9 illustrates this mechanism.

The measured voltage at the shunt resistor $R_{S,PFC}$ during the PFC gate driver on-time is used for PFC current limitation.

4.2.2 Multimode operation and frequency law

The PFC controller provides various modes of operation. When going from full to no load several operation modes are used in order to optimize efficiency and EMI behavior.

A PFC converter is used to emulate a resistive load $R_e = V_{AC,rms} / I_{AC,rms}$ to the AC input. The output of the PFC bus voltage controller $t_{PFCon,des}$ is inversely proportional to the emulated resistive load R_e. Thus, $t_{PFCon,des}$ varies as the AC line voltage magnitude varies and is proportional to the RMS input current $I_{AC,rms}$.

The frequency law depicted in Figure 10 indicates the operation mode for the complete range, which can be $t_{PFCon,des}$ or $I_{ac,rms}$ range. A limitation within a minimum switching frequency $f_{swPFCmin}$ and a maximum switching frequency $f_{swPFCmax}$ is applied in every switching cycle. In QRM (see Chapter 4.2.2.1) exceeding the thresholds $f_{swQRmax}$ and $f_{swQRmin}$ lead to a change of valley.

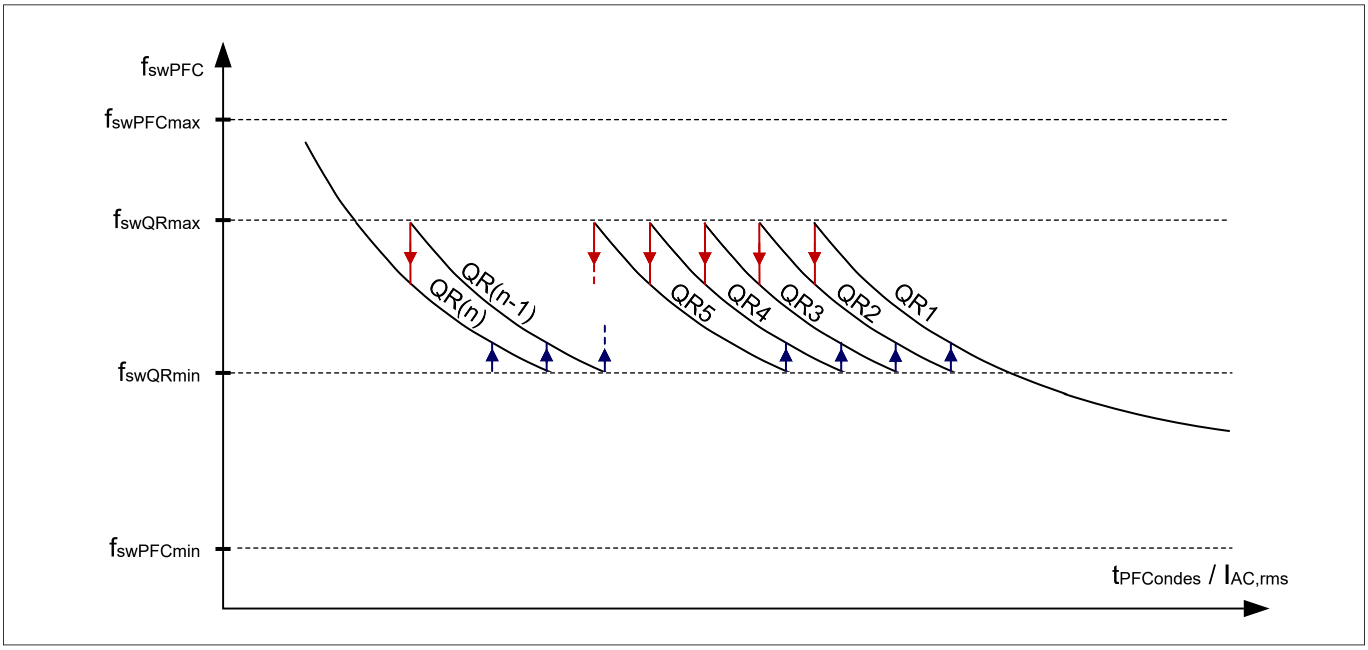

Figure 10 **Frequency law**

4.2.2.1 Quasi-resonant mode (QRM)

In quasi-resonant operation mode (QRM) the PFC MOSFET is turned on in the valley of the oscillation seen at the MOSFET's drain-source voltage after demagnetization. QRM reduces PFC MOSFET switching losses and ensures highest possible efficiency of the system.

In QR1 operation the first valley is used. The MOSFET is turned on as soon as a ZCD event is detected and the absolute minimum switching period $t_{swPFCmin} = 1 / f_{swPFCmax}$ is exceeded.

With decreasing load or increasing input voltage switching frequency is increasing and the maximum switching frequency $f_{swQRmax}$ is hit. In this case the valley number should be increased. With load getting higher or input voltage decreasing, the lower frequency limit $f_{swQRmin}$ will be hit and the valley number should be decreased.

However, in order to prevent valley number change within each AC half cycle, valley change blanking times $t_{QRblkinc}$ and $t_{QRblkdec}$ apply.

In order to ensure good ZCD detection before the PFCCS signal gets too small in amplitude, only 1st valley (QR1) to a configurable n-the valley $N_{PFCvalleymax}$ are supported. In case $N_{PFCvalleymax}$ is reached the frequency is only limited by $f_{swPFCmax}$.

The time during QR valley oscillation, when neither PFC switch nor PFC diode is conducting, is responsible for some AC input current waveform distortion and affects the PFC THD performance. The multimode PFC controller uses an algorithm that optimizes the applied on-time on a cycle by cycle basis so as to ensure good input current shaping and improve PFC THD performance.

4.2.2.2 Low power mode

In softstart and steady operation, a minimum on-time $t_{PFConmin}$ applies with $t_{PFConmin} \geq t_{PFCCSleb}$. As soon as the on-time $t_{PFCondes}$ determined by the bus voltage controller is less than a value $t_{PFConskip}$ the switching pulse is skipped and PFC gate driver is not switching. Depending on the configuration, the value of $t_{PFConskip}$ is same a $t_{PFConmin}$ or can be set to be scaled with the AC line rms voltage.

At low output load, the combo controller IC goes into burst mode. The PFC burst mode operation is synchronous to the hybrid-flyback burst mode operation.

4.2.3 PFC bus voltage sensing and regulation

The controller senses the PFC output voltage V_{bus} via pin PFCVS. The bus voltage is maintained by a nonlinear PIT1 controller that calculates the desired on-time $t_{PFCondes}$ in response to the sensed voltage.

The PFC on-time from regulation $t_{PFCondes}$ is limited to a configurable minimum value $t_{PFConmin}$ and a maximum value $t_{PFConmax}$.

The PFC target bus voltage and the bus voltage undervoltage protection level V_{busUVP} are set dynamically by the controller. In case the bus voltage V_{bus} drops and is getting close to V_{busUVP}, the controller reacts and increases the on-time to the maximum on-time $t_{PFConmax}$ in order to boost up the bus voltage.

In order to compensate for the AC line gain dependency of the boost power stage, the PIT1-controller processes the previous sample of $t_{PFCondes}$ in nonlinear way. This is used as a kind of AC input feedforward-control.

4.2.4 PFC bus voltage target setting

In contrast to a conventional PFC boost converter, the bus voltage target level $V_{bustarget}$ is not fixed but changing with operation conditions. On the one hand, the hybrid-flyback stage is requesting some bus voltage target level depending on the output voltage. On the other hand, the PFC itself can set a target bus voltage level following the AC peak voltage. This feature is described in more detail in Chapter 4.4.3.

4.2.5 PFC soft-start

Each time the PFC is enabled, the PFC initiates a soft start to minimize the switching stress on the power MOSFET, diode and inductor. During a soft start, the PFC operates in QR1-mode. The soft-starts ends as soon as the bus voltage has reached 93.75% of the target value $V_{bustarget}$ or when PFC pulse skipping mode is entered. The initial on-time depends on the configuration: It is either fixed or will be scaled with the AC line rms voltage.

4.2.6 PFC gate driver

A PFC gate driver is integrated in the controller at pin PFCGD. In order to drive discrete GaN-HEMT devices, a dedicated external RC-network is recommended.

4.2.7 PFC disable

The PFC can be disabled completely and permanently by configuration. At the same time all PFC related protections are automatically disabled. The hybrid-flyback and related house-keeping functions still enabled.

The controller with disabled PFC functionality is meant to be combined with an separate, standalone PFC controller providing a regulated bus voltage V_{bus} which is high enough for reliable operation of the hybrid-flyback in all operation conditions. Otherwise, PFC bus undervoltage protection will trigger (see Chapter 4.5.2.10).

4.3 Hybrid-flyback control

The hybrid-flyback converter is based on a resonant asymmetrical half-bridge topology with flyback output. Figure 11 shows the hybrid-flyback stage with the associated control blocks.

The hybrid-flyback power stage can achieve zero voltage switching (ZVS) operation on primary side and zero current switching (ZCS) operation on secondary side under all conditions of bus voltage V_{bus} and output voltage V_{out}. In order to achieve ZVS operation, two control methods are implemented:

- Continuous resonant mode (CRM) operation
- Zero voltage resonant valley switching (ZV-RVS) operation

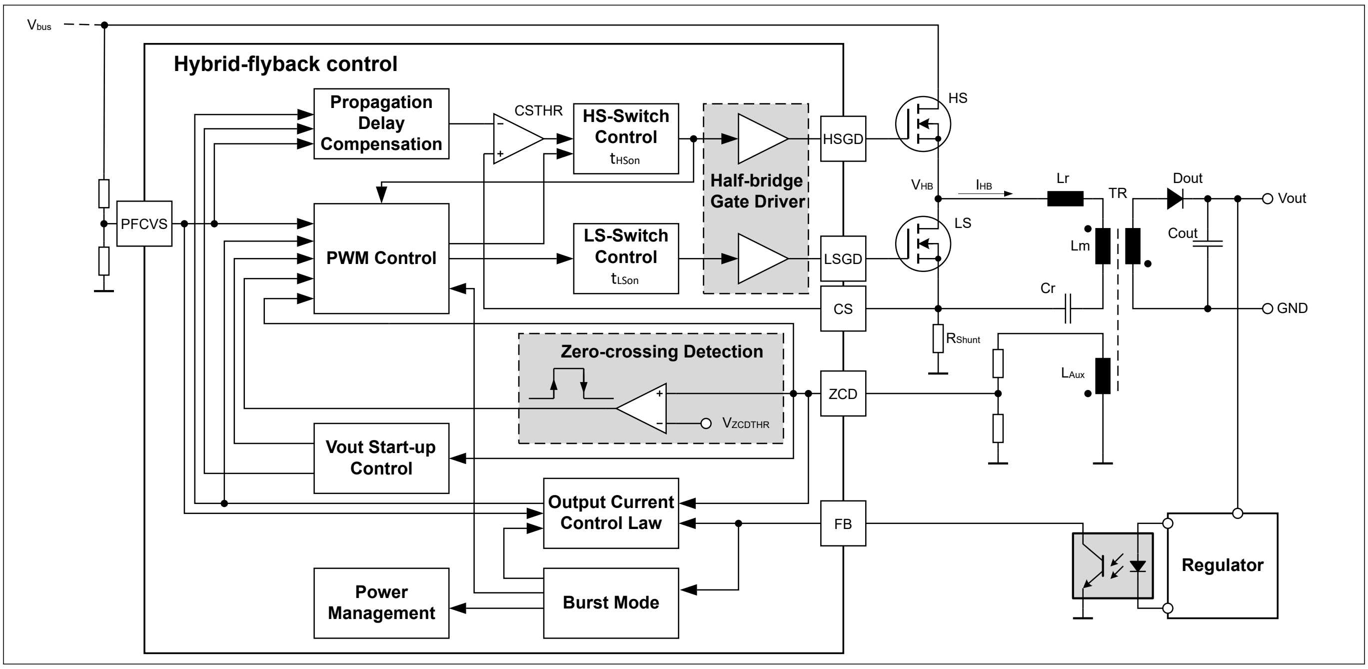

Figure 11 **Hybrid-flyback circuit arrangement with associated control blocks**

The output current control uses the CSTHR-comparator for peak current control via high-side switch on-time t_{HSon}.

4.3.1 PWM control schemes

In the following chapter the pulse width modulation (PWM) control methods for the different control modes and the associated mode transition are discussed. Depending on load, output voltage and bus voltage the control scheme is adjusted to ensure ZVS operation for both low-side and high-side switches.

4.3.1.1 CRM control scheme

In continuous resonant mode (CRM) the switching of high-side switch HS and low-side switch LS is done in a continuous alternating manner with short dead-times t_{deadHS} for the high-side switch turn-on and t_{deadLS} for the LS switch turn-on.

It targets a ZVS operation for every half-bridge switching cycle by tuning the negative current level I_{MAGneg}.
In Figure 12 typical waveforms are shown. The dead-time t_{deadLS} between HS and LS switch is fixed as the peak current is high enough to provide proper ZVS operation for LS switch.

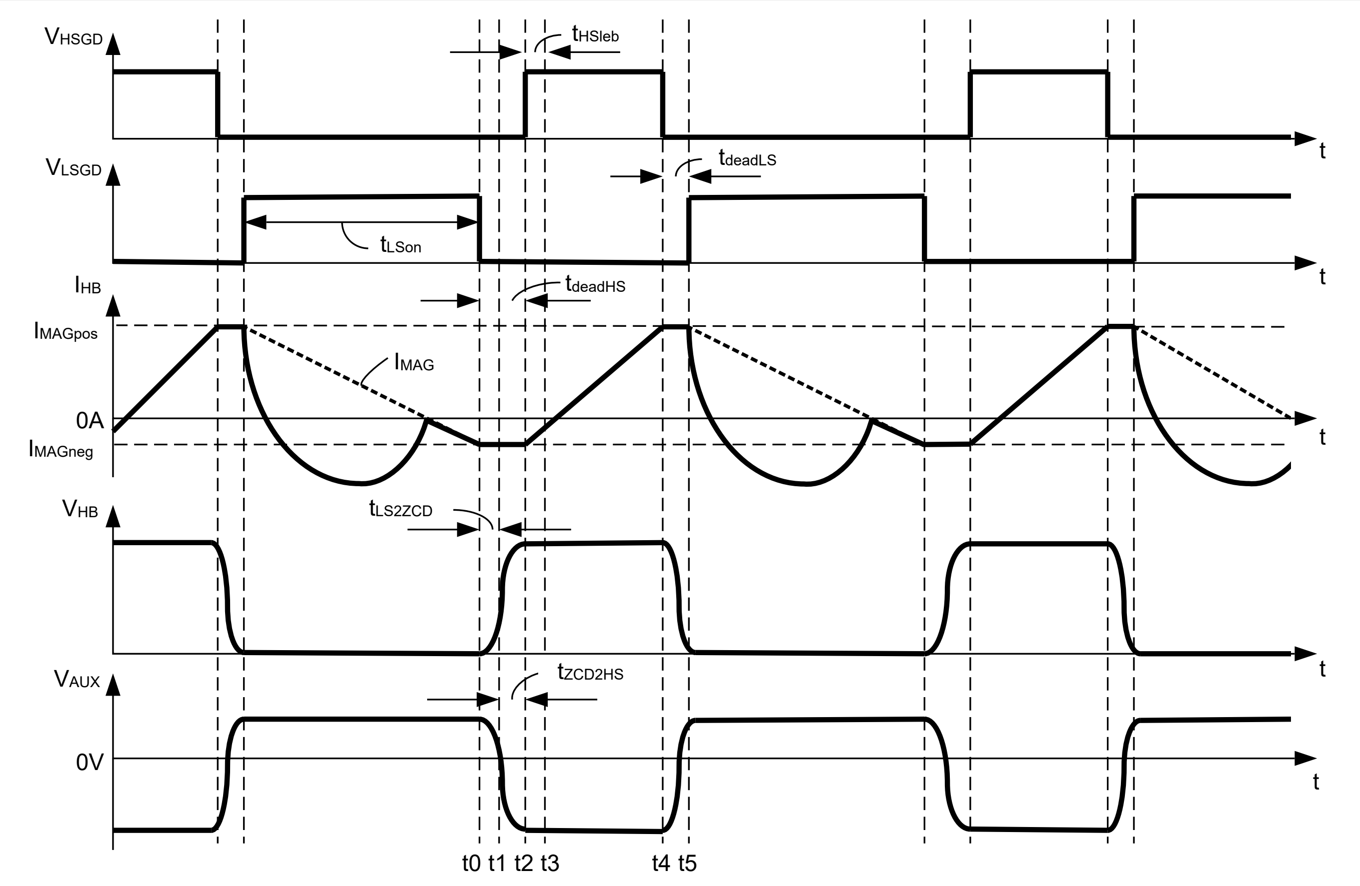

Figure 12 Half-bridge timings for CRM operation

In CRM operation the dead-time t_{deadHS} consists of two time intervals:

$$t_{deadHS}(CRM) = t_{LS2ZCD} + t_{ZCD2HS}$$

Equation 1

The LS on-time is adjusted cycle-by-cycle based on the target delay time t1 - t0 = t_{LS2ZCD} and target $I_{MAGneg}(V_{bus})$, see Chapter 4.3.2.2.

The fixed time period t2 - t1 = t_{ZCD2HS} is delaying the HS switch turn-on at time t2 so that HS ZVS is possible.

After the HS switch is activated, the peak current control determines the HS on-time. The magnetizing current can be measured after a leading edge spike blanking period t_{HSleb}, which therefore determines the minimum on-time of HS switch operation.

4.3.1.2 ZV-RVS control scheme

When decreasing the load the amount of circulating magnetization energy is proportionally increasing compared to the transmitted energy in CRM operation. When decreasing V_{out} the demagnetization time is becoming much longer than half of the resonant period of the LrCr tank, which can lead to further resonant half-bridge oscillations. Turning off the LS switch during an ongoing I_{HB} oscillation can lead to oscillations on the secondary side due to the secondary side leakage inductance.

To overcome these issues the zero voltage resonant valley switching (ZV-RVS) mode is provided. It keeps the peak magnetizing current in the desired range while maintaining soft switching of both HS and LS switch. Lower load is addressed by lower switching frequency. Figure 13 shows typical waveforms when operating in the second valley.

Compared to CRM, there are two LS pulses during HS off-time with a wait gap $t_{waitgap}$ in-between. The first LS pulse demagnetizes the LrCr tank and charges the output capacitor on the secondary side. The waiting time gap $t_{waitgap}$ is inserted at time t0 after a HS and LS switch half-bridge cycle. During the wait gap, a free-wheeling oscillation takes place which is sensed by pin ZCD with a comparator. The second LS pulse, the so-called ZVS pulse t_{ZVS}, starts shortly after the first or a later rising edge detection of the ZCD comparator at time t1 and a configurable delay time period $t_{ZCDfilRVS}$ so that the LS switch turns on at a valley of the drain-source voltage and zero magnetizing current. Hence, a resonant valley switching (RVS) operation is achieved. Selecting a later valley increases the wait gap duration $t_{waitgap}$ and lowers the switching frequency. The ZVS pulse further demagnetizes the the LrCr tank to a negative value I_{MAGneg} for zero-voltage switching (ZVS) of the HS switch. The required ZVS pulse length t_{ZVS} is determined by the target negative magnetization level I_{MAGneg}, the transformer magnetizing inductance Lm and depends on the output voltage Vout. The minimum ZVS pulse length occurs at lowest input and highest output voltage. In addition a lower limit t_{ZVSmin} applies.

The dead-time for turning on the HS switch after the ZVS pulse is fixed with using the value $t_{deadHSRVS}$. The subsequent dead-time t_{deadLS} is same as in CRM operation.

Selecting the appropriate valley and adjusting the magnetizing peak current within the desired range controls the load.

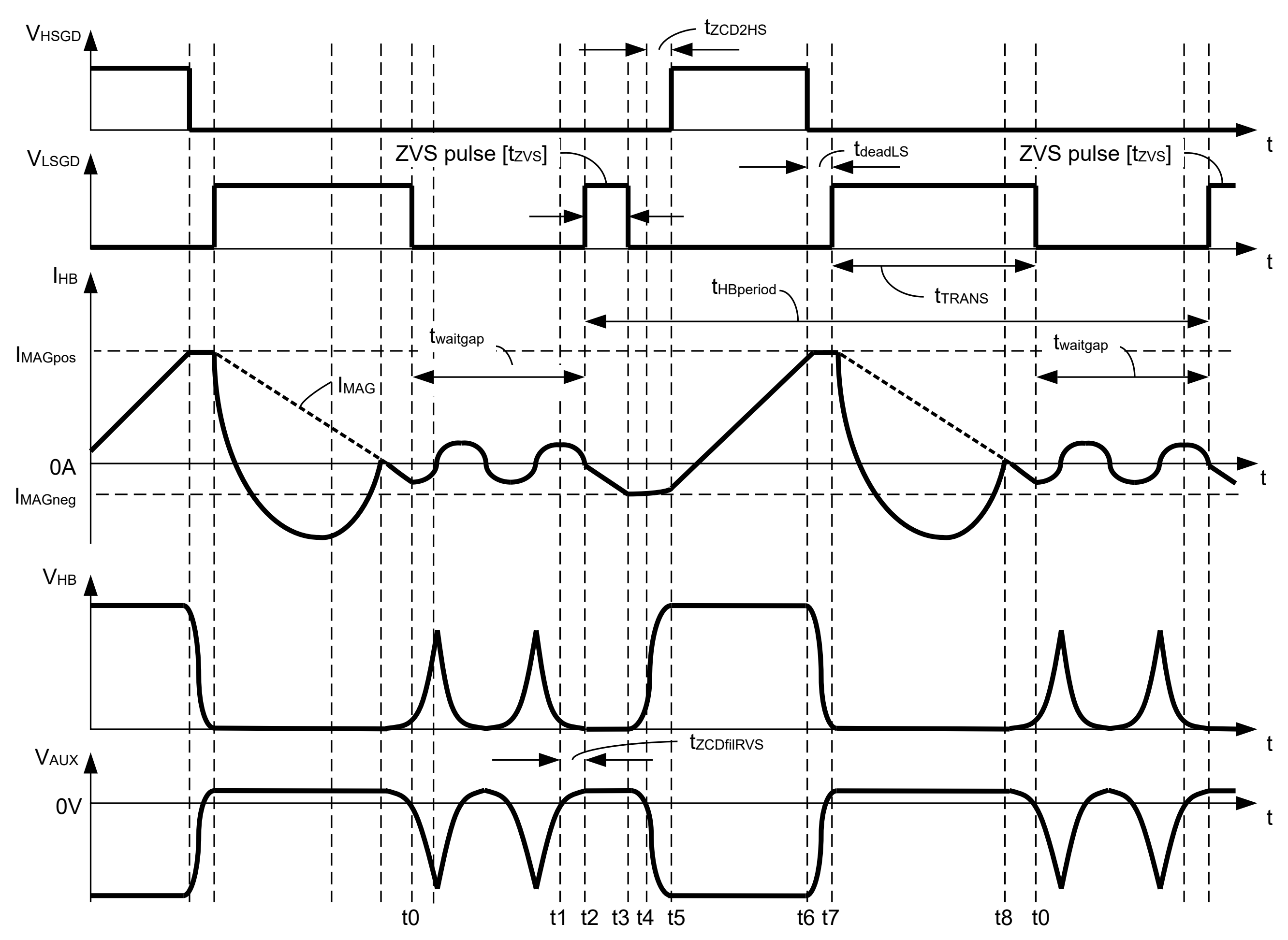

Figure 13 Hybrid-flyback operating in zero voltage resonant valley switching mode (ZV-RVS)

4.3.1.3 Valley skipping control

When operating in ZV-RVS mode, valley detection is taking place to determine the time for turning on the ZVS pulse. The waiting time $t_{waitgap}$ is controlled based on the target number of detected valleys.

The target valley number is chosen so that the magnetizing peak current is in the desired range to ensure an optimum operation. If the target valley cannot be detected, the controller will enter DCM operation with a similar fixed frequency.

4.3.1.4 DCM control scheme

ZV-RVS mode operation at light-load is limited by the maximum number of detectable zero-crossings at ZCD due to decreasing oscillation magnitude with prolongation of the inserted waiting time gap $t_{waitgap}$. When further reducing the output current the waiting time gap $t_{waitgap}$ is further increased until the ZVS pulse is initiated without zero-crossing detection. The subsequent half-bridge cycle is then again performed under ZVS condition. Increasing $t_{waitgap}$ takes only place until the half-bridge period $t_{HBperiod}$ reaches the associated minimum half-bridge switching frequency $f_{swDCMmin}$.

4.3.1.5 Mode transition between CRM and ZV-RVS

The mode transition control is based on the target peak current I_{MAGpos} and the voltage measured at ZCD pin. First, a transition from CRM to ZV-RVS mode and vice versa is only possible in case the output voltage, sensed via ZCD, has a certain value: The transition from ZV-RVS to CRM is only possible with a detected output voltage greater than $V_{outRVS2CRM}$ (in order to have some hysteresis, the transition from CRM back to ZV-RVS only happens for an output voltage smaller than $V_{outCRM2RVS}$). Second, the feedback signal V_{FB} is determining the internal current set-point I_{SET} and compared with the internal thresholds for changeover.

4.3.2 Output control

Similar as in standard flyback controllers primary peak current control is implemented to support a 1st order system for easier control loop compensation. The input power per half-bridge switching cycle is depending on the voltage at the resonant capacitor C_r that is charged by the half-bridge current I_{HB} during the on-time t_{HSon}. The input power in CRM-mode can be calculated as shown in the following equation:

$$P_{in} = \frac{1}{2} \cdot V_{Cr,avg} \cdot \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 2

$V_{Cr,avg}$ is the average voltage on the resonant capacitor C_r , which is the reflected output voltage V_{out} multiplied with the transformer turns ratio. The output voltage is reflected at winding L_{AUX} during the on-time period of LS switch.

$$V_{Cr,avg} = N \cdot V_{out}$$

Equation 3

Assuming an ideal system leads to a direct correlation between input half-bridge current I_{HB} and average output current I_{out}:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{1}{2} \cdot N \cdot \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 4

It shows that I_{out} can be controlled only by controlling I_{MAG} and can then be independent of V_{bus} and V_{out}.

The hybrid-flyback is controlling the magnetization time t_{mag} and demagnetization time t_{demag} in two different ways. t_{mag} is mainly controlled by the positive half-bridge current level I_{MAGpos} by means of peak current control via shunt resistor R_{shunt} at pin CS. Whereas t_{demag} is controlled by adjusting the on-time t_{LSon}. Increasing t_{demag} increases the negative magnetizing current level I_{MAGneg} when keeping I_{MAGpos} level constant.

Compared to CRM operation the ZV-RVS mode is adding waiting time gaps $t_{waitgap}$, where no energy is either taken from the input nor energy is transferred to the output. The average output current I_{out} is decreasing with increasing $t_{waitgap}$ accoding to

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{t_{HBperiod} - t_{waitgap}}{t_{HBperiod}} \cdot \frac{1}{2} \cdot N \cdot (I_{MAGpos} + I_{MAGneg})$$

Equation 5

The output current is only controlled by means of the positive magnetization current level I_{MAGpos}. During continuous operation the output current I_{out} is controlled by means of a linear relationship between the feedback voltage at FB pin and the associated internal current set-point I_{SET}, which is described in Chapter 4.3.2.1. The negative current I_{MAGneg} is controlled cycle by cycle via the turn-on time of LS switch t_{LSon}. The target for the negative peak current depends on the input voltage V_{bus} (see Chapter 4.3.2.2).

4.3.2.1 Output current control law

The positive magnetization level I_{MAGpos} equals the positive half-bridge peak current that is controlled via CS pin at the shunt resistor R_{Shunt}:

$$V_{CSpeak} = I_{MAGpos} \cdot R_{Shunt}$$

Equation 6

Peak current regulation is prone to error due to noise. CS pin related PCB design should consider this sensitivity. An external high-frequency R-C-filter at CS pin is recommended. In addition, a digital filter using a configurable filter time $t_{CSTHRfil}$ can be set to blank the CSTHR comparator event.

Figure 14 shows the control path from feedback signal input at FB pin to peak current setting at CS pin. The requested output current equals to the internal I_{SET} for the corresponding feedback signal. The required peak current setting is then calculated based on V_{bus} measurement and mode operation.

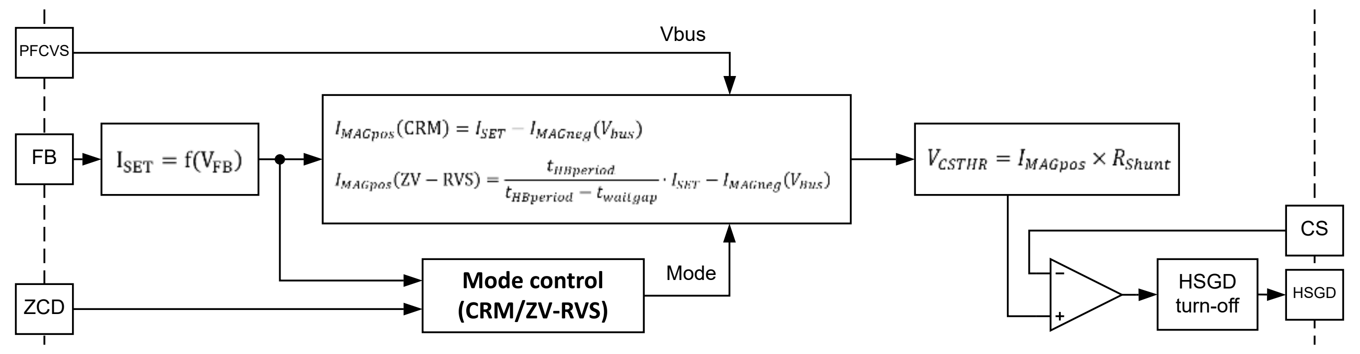

Figure 14 Control path from feedback input to peak current setting

The feedback pin has a pull-up resistor R_{FBpu} to V_{FBoc}. The value of the pull-up resistor R_{FBpu} is configurable. The feedback voltage V_{FB} has a linear correlation with the output current I_{out} between burst mode entry current level $I_{outBMen}$ and the maximum output current $I_{outOCPmax}$. Figure 15 shows the relationship between output current and feedback voltage.

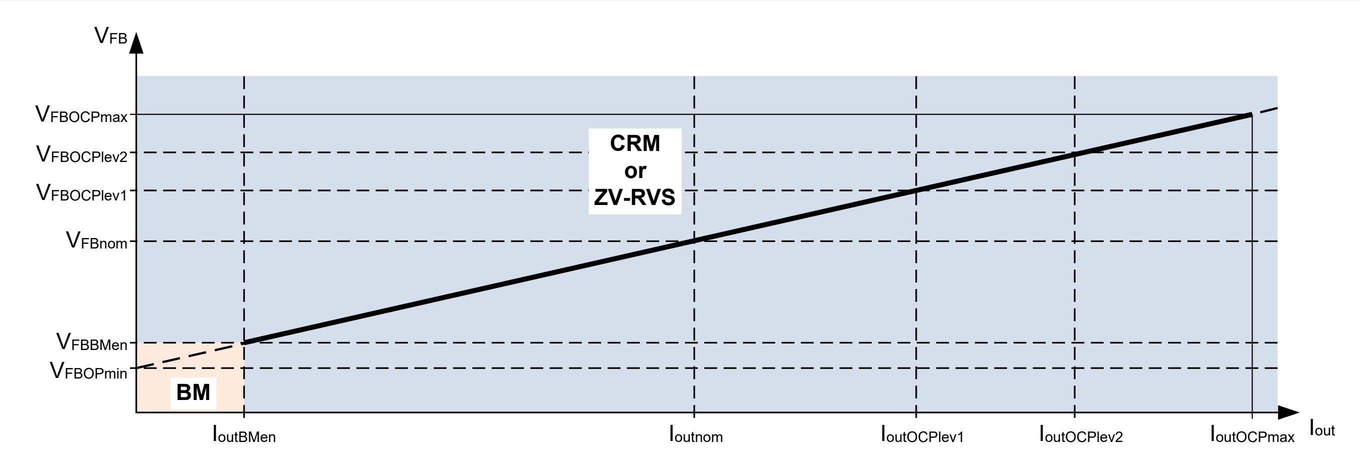

Figure 15 Control law for feedback voltage at FB pin

In the IC output current I_{out} is represented by the equivalent internal current set-point I_{SET}, which is then mapped to the positive magnetization level I_{MAGpos}. The peak current I_{MAGpos} is controlled by a comparator with variable threshold at pin CS. The relation between I_{SET} and I_{MAGpos} is different for CRM and ZV-RVS mode.

4.3.2.2 Keeping ZVS operation for wide Vbus voltage range

ZVS operation for wide input voltage range is achieved by the target negative magnetization level $I_{MAGneg}(V_{bus})$ based on two set-points for minimum and maximum V_{bus}(see Figure 16).

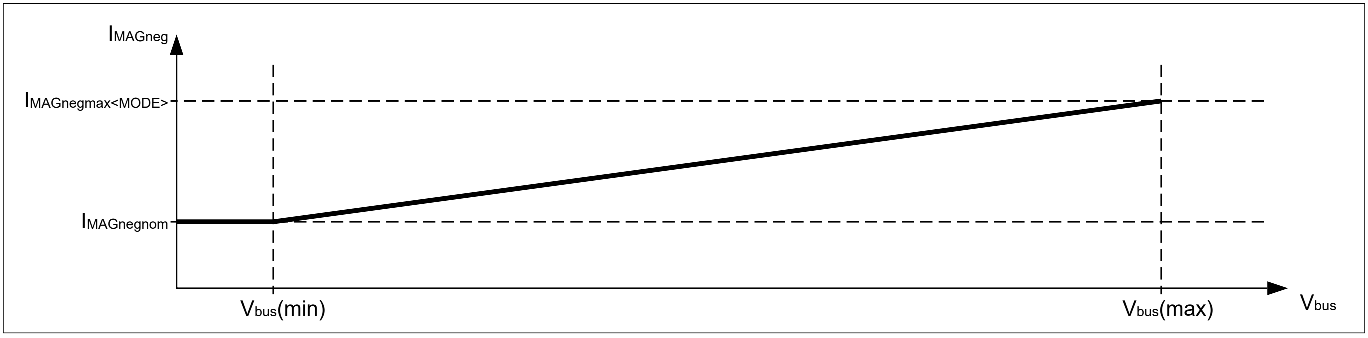

Figure 16 Target I_{MAGneg} as function of V_{bus}

4.3.2.3 Keeping ZVS operation for wide output voltage range

When output voltage Vout is decreasing the demagnetization takes longer. In CRM, ZVS operation is ensured by adjusting the turn-on time of the LS switch t_{LSon} to match with the changed Vout. In ZV-RVS, the ZVS pulse on-time t_{ZVS} is calculated from I_{MAGneg} and Vout and the first LS on-time t_{TRANS} decreases with increasing Vout (see Figure 17).

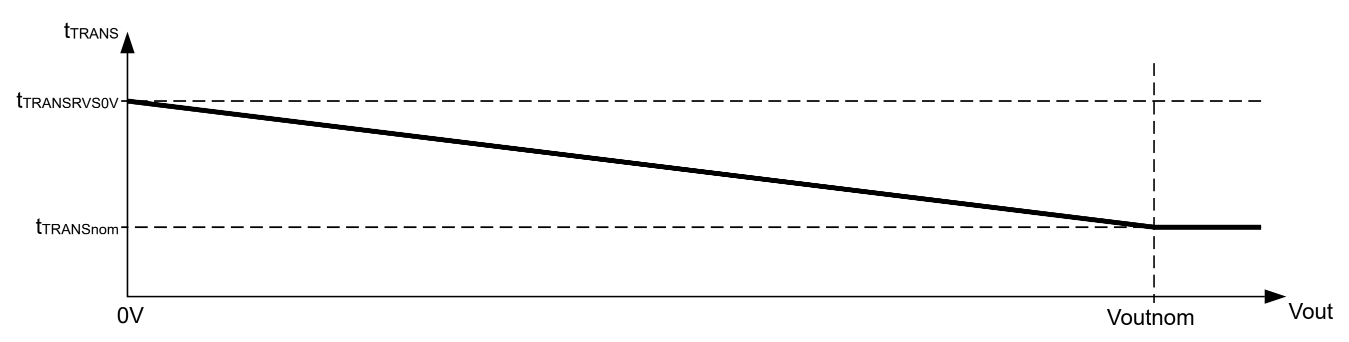

Figure 17 Vout compensation for t_{TRANS} in ZV-RVS mode

4.3.2.4 ZVS operation and body-diode cross-conduction prevention during CRM operation

A too short LS on-time can cause hard switching or even body diode cross conduction if the magnetizing current is still positive when LS is turned off. A too long on-time increases the reactive current and conduction losses and can even saturate the transformer. In order to exclude hard switching and body diode cross conduction, the controller activates the HS switch only after the voltage at pin ZCD indicates a changing half-bridge voltage V_{HB} (ZCD event). The controller adjusts the LS on-time to always ensure ZVS condition.

4.3.2.5 Propagation delay compensation (PDC)

During peak current control a propagation delay is impacting the peak current resulting in higher values. The overshoot depends on the voltage at the transformer winding L_m, the input voltage V_{bus} and reflected output voltage at resonant capacitor V_{Cr}. This dependency on V_{bus} and V_{Cr} impacts the current set-point threshold accuracy seen in the application and is therefore compensated to avoid errors on the feedback signal V_{FB} and the internal current set point I_{SET}.

4.3.3 Vout start-up control

A hybrid-flyback start-up takes place after the start-up conditions are met, see Chapter 4.1.1. At first several LS pulses are applied to precharge the bootstrap capacitor at HSVCC pin. After that ZV-RVS switching cycles smoothly ramp up the output voltage. Here, the first switching cycles run with a low fixed frequency until the voltage at pin ZCD is high enough for valley switching. The startup-phase is finished once the feedback loop takes over the peak current control.

During the first HS pulse the CS pin is checked for short circuit. For the ZVS pulse duration a maximum applies to prevent too long ZVS pulse due to very low ZCD voltage measurement. A transition from ZV-RVS to CRM may take place during the startup-phase if the voltage sampled at pin ZCD exceeds the related thresholds.

4.3.4 Frequency jitter

The switching frequency jitter function is only active in CRM operation and in case the bus voltage is above the configurable bus voltage threshold $V_{busJitteren}$ for enabling the jitter functionality. Switching frequency jitter is done by modulating the peak to peak magnetizing current I_{MAGpp}.

4.3.5 Half-bridge gate driver

The half-bridge gate driver consists of a low-side gate driver for LS switch, which is supplied by VCC and GND pin. The HS switch is driven by a floating high-side gate driver supplied by HSVCC and HSGND. The floating HS domain is galvanically isolated and steered via a coreless pulse transformer. The LS and HS gate drivers are enabled/disabled based on the corresponding undervoltage lockout thresholds (V_{VCCon}, V_{VCCoff}) and ($V_{HSVCCon}$, $V_{HSVCCoff}$) (see Chapter 4.5.2.1 and Chapter 4.5.2.2). Both drivers are clamping the maximum gate driver output voltage to $V_{LSGDhigh}$; $V_{HSGDhigh}$. If disabled the gate driver outputs are actively kept shut down. When HSVCC exceeds the threshold $V_{HSVCCon}$ the high-side gate driver is enabled after a time period of $t_{HSGDendel}$.

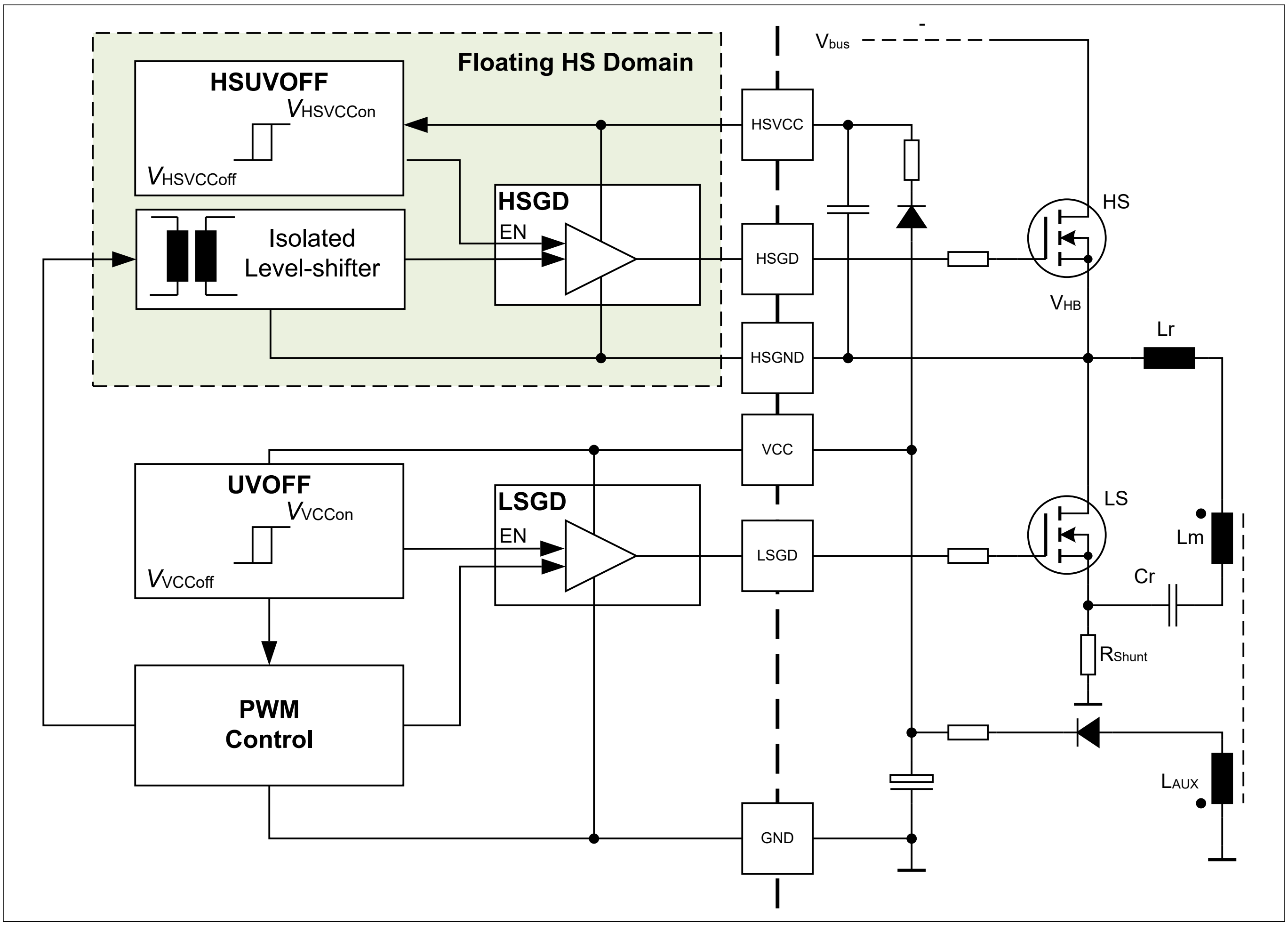

Figure 18 **Half-bridge gate driver**

In order to drive discrete GaN-HEMT devices in the half-bridge, a dedicated external RC-network is recommended, see Figure 3.

For the high voltage level $V_{LSGDhigh}$ of the LS gate driver two different values can be set by configuration.

4.4 Combo-control functions

In the following section the combo-controller functions with PFC and Hybrid-flyback controller interaction for an optimum system control are described.

4.4.1 Burst mode control

The IC contains a burst mode control block to enter a highly efficient operation mode at light-load. By introducing longer non-switching phases with IC entering a sleep mode the average switching and bias losses are reduced during burst mode operation. Both, the PFC stage and the hybrid-flyback, go into burst mode at low load. The burst mode operation is controlled by the hybrid-flyback controller in relation to the output current reflected by the feedback voltage V_{FB}. In general, the burst-mode operation of PFC and hybrid-flyback is synchronized. Figure 19 shows the main functions for the burst mode control.

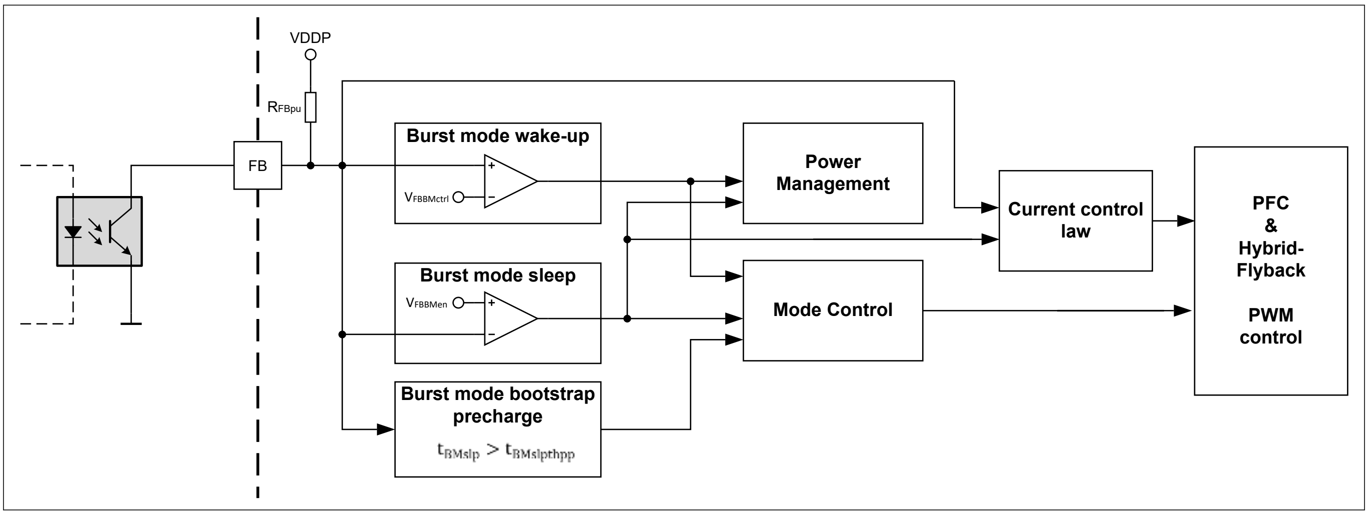

Figure 19 Burst mode control block

4.4.1.1 Burst mode entry

Once V_{FB} is dropping below V_{FBBMen} the generation of next switching pulse is stopped and burst mode is enabled by entering sleep mode with the reduced current consumption $I_{VCCBMpsm}$. At burst mode entry the HV start-up cell is turned on to charge up VCC until V_{VCCon} is reached.

At burst mode entry the HV start-up cell is turned on once to charge up the VCC and VCC current consumption is reduced during the sleep phases (see Chapter 4.1.4).

4.4.1.2 Burst mode operation

The steady state burst mode operation is based on a burst frame on/off control by means of comparing the voltage at FB pin with the feedback thresholds V_{FBBMen} and $V_{FBBMctrl}$. The threshold V_{FBBMen} determines when the IC enters the sleep phase. During the sleep phase the threshold $V_{FBBMctrl}$ is used for for waking up. The burst frame duty cycle and burst frame frequency is fully controlled by means of $V_{FB.}$ VCC current consumption is reduced during the sleep phases.

The PFC is always switching synchronously with the hybrid-flyback. However, depending on the operation conditions, PFC might also be disabled (see Chapter 4.4.2) and not switching.

4.4.1.3 Burst mode bootstrap precharge

Operation in burst mode at very light-load leads to long sleep phases without switching activities. During this sleep-time period the HSVCC voltage may drop below the off-threshold $V_{HSVCCoff}$ and deactivate the floating HS gate driver. To ensure that a proper HSVCC supply is in place for turning on the HS switch after a long IC sleep phase, a train of $N_{BMprepulse}$ precharge pulses is introduced before the first ZV-RVS switching cycle. The precharge pulse train is only introduced when the captured burst mode sleep time has exceeded the threshold $t_{BMslpthrpp}$. Figure 20 shows a precharge pulse train pattern for the case $N_{BMprepulse}$=3.

Note: *If a HS pulse is missing due to improper HSVCC supply, the subsequent LS pulse may lead to hard switching. Therefore, the controller tries to detect this case and may stop the switching operation.*

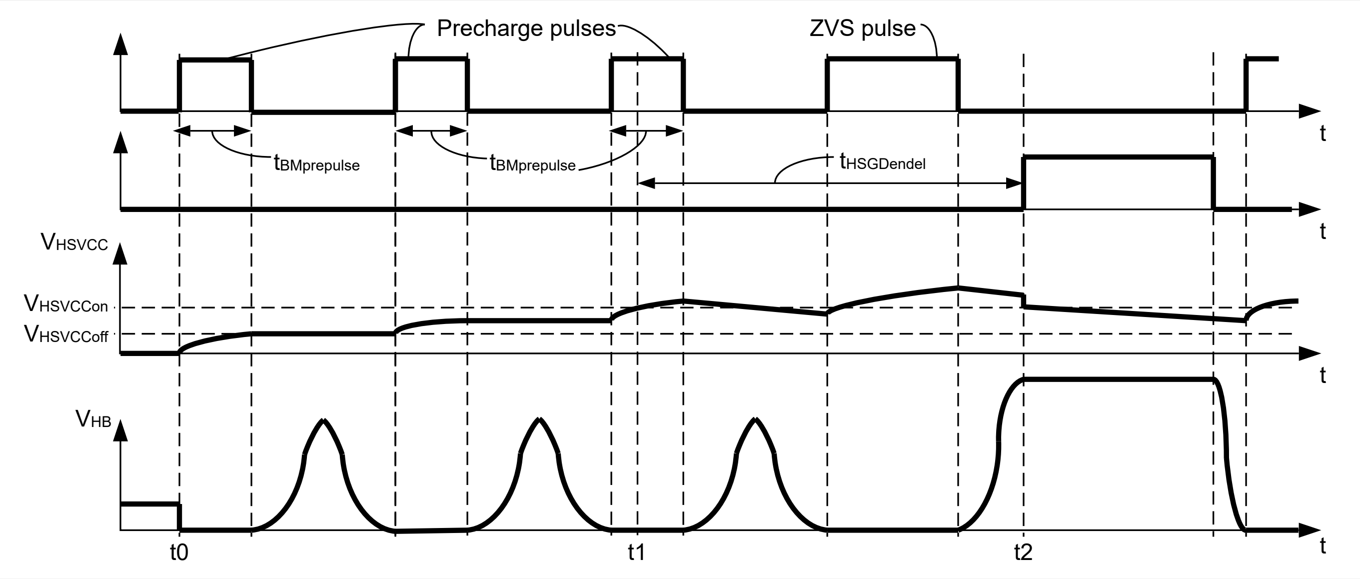

Figure 20 Precharge pulse train pattern

4.4.1.4 Burst mode exit

Burst mode exit is a smooth transition from on/off control back to the closed feedback control loop at load increase, no matter if the load jumps or increases slowly. In these cases the controller it will wake-up (in case it was not active yet) and starts switching. Since the load and the voltage at pin FB are high, the controller is not going to sleep anymore but changes to normal operation. This smooth transition is possible as in regular burst mode active phase regular peak current control based on the feedback control applies.

4.4.2 PFC enable/disable control

The PFC stage is enabled and active, when the load is above a certain level where power factor correction could be mandatory or the hybrid-flyback stage requires a minimum input voltage level for proper operation.

Whether the load requires PFC operation is decided by a hysteretic comparator with two thresholds $P_{PFCenable}$ and $P_{PFCdisable}$. Not that the PFC may be enabled although the estimated power is below $P_{PFCdisable}$ to ensure proper hybrid-flyback operation. Whether the hybrid-flyback stage requires PFC operation is decided by a hysteretic comparator evaluating the AC line peak voltage with two thresholds derived from the sensed output voltage.

4.4.3 Variable bus voltage target level

Compared to conventional PFC boost operation, the PFC bus voltage is not regulated to a fixed target value but the target voltage depends on the operation conditions and is set either by the hybrid-flyback stage or by the PFC itself. This functionality is closely related to the PFC enable/disable control (see Chapter 4.4.2).

For optimum operation of the hybrid-flyback stage over a wide output voltage range, the PFC bus voltage target level $V_{bustarget,HFB}$ requested by the hybrid-flyback stage is determined by the controller depending on the reflected output voltage $N \cdot V_{out}$ measured via pin ZCD.

A proper PFC operation is only possible in case the target bus voltage target level is somewhat above the given AC line peak voltage $|V_{ACpk}|$. For that reason the PFC controller also determines a bus voltage target level $V_{bustarget,PFC}$ which is the detected rectified AC peak voltage plus an offset.

Whenever PFC is enabled and switching the higher value of $V_{bustarget,HFB}$ and $V_{bustarget,PFC}$ is used as target value for the PFC regulation.

Furthermore, the bus voltage target value is limited to a minimum value $V_{bustargetmin}$ as well as to a maximum value $V_{bustargetmax}$.

4.5 Protections

The IC supports several protection functions resulting in different protection reactions.

For most protection events the IC enters a protection mode (see Chapter 4.5.1). In many cases the protection mode is configurable.

Table 4 Protection Features and Reaction

Protection Feature	Symbol	Protection Reaction
VCC undervoltage lockout	UVOFF	HW reset and restart
HSVCC undervoltage lockout	HSUVOFF	Disable HS gate driver
VCC overvoltage protection	VCCOVP	Configurable: Auto-restart or latch
Brown-in protection	BIP	Bang-bang mode, waiting for brown-in in start-up check phase
Brown-out protection	BOP	Stop operation and enter bang-bang mode for start-up check phase
AC loss protection	ACLOSS	Stop operation and enter bang-bang mode for start-up check phase and active X-capacitor discharge
PFC Start-up timeout protection	PFCSTTOP	Configurable: Auto-restart or latch
Output start-up timeout protection	VoutSTTOP	Configurable: Auto-restart or latch
AC overvoltage protection	ACOVP	Configurable: Auto-restart or latch
PFC bus overvoltage protection level 1	PFCOVP1	Stop PFC switching
PFC bus overvoltage protection level 2	PFCOVP2	Stop PFC switching (cycle-by-cycle)
PFC bus undervoltage protection	PFCUVP	Configurable: Auto-restart or Stop operation and enter bang-bang mode for start-up check phase
PFC overcurrent protection	PFCOCP	Stop PFC switching (cycle-by-cycle)
PFC CCM protection	PFCCCM	Configurable: Auto-restart or latch
Output overcurrent protection level 1	OCPlev1	Configurable: Auto-restart or latch
Output overcurrent protection level 2	OCPlev2	Configurable: Auto-restart or latch
Output maximum current protection	OCPmax	Configurable: Auto-restart or latch
HFB primary side overcurrent protection	CSPROT	Configurable: Auto-restart or latch
Vout overvoltage protection	VoutOVP	Configurable: Auto-restart or latch
Vout undervoltage protection	VoutUVP	Configurable: Auto-restart or latch
Vout short circuit protection	VoutSCP	Configurable: Auto-restart or latch

(table continues...)

Table 4 (continued) Protection Features and Reaction

Protection Feature	Symbol	Protection Reaction
CS pin short protection	CSSCP	Configurable: Auto-restart or latch
FB pin start-up protection	FBSTUP	Stop operation and enter bang-bang mode for start-up check phase
HFB open loop protection	HFBOLP	Configurable: Auto-restart or latch
External overtemperature protection	extOTP	Configurable: Auto-restart or latch
Watchdog timer	WDOG	Configurable: Auto-restart or latch

4.5.1 Protection modes

Once the protection mode is entered, the IC stops the gate driver switching at the PFCGD, LSGD and HSGD pins and enters stand-by mode. During stand-by mode, the HV start-up cell is operating in the bang-bang mode (see Chapter 4.1.3) to keep the VCC voltage at a high level to have enough energy stored in the VCC capacitor for the system start-up. Three protections modes are supported as described in the sequel.

4.5.1.1 Deactivate IC after under-voltage lockout

In case VCC drops below V_{VCCoff} the under-voltage lockout protection is triggered, the IC is completely deactivated and is only restarted with the regular start-up mechanism, see Chapter 4.1.1.

4.5.1.2 Auto-restart mode

When auto-restart mode is activated, the controller stops switching at the gate driver pins. After a configurable auto restart time t_{ARM}, the control IC resumes its operation with soft-start after the VCC capacitor is charged up and the VCC voltage has reached its turn-on threshold V_{VCCon}. During the auto restart time t_{ARM} the controller wakes up very t_{ARMbase} in order to re-charge VCC (see Chapter 4.1.3).

4.5.1.3 Latch mode

In latched operation the system keeps staying in stand-by mode without any restart attempt. The latched operation can only be reset by VCC dropping below the UVOFF HW reset threshold V_{VCCoff}. Like in auto-restart mode the controller wakes up very t_{ARMbase} in order to re-charge VCC (see Chapter 4.1.3).

4.5.2 Protection features

4.5.2.1 VCC undervoltage lockout

The implemented VCC undervoltage lockout (UVOFF) ensures a defined activation and deactivation of the IC operation depending on the supply voltage at pin VCC. The UVOFF contains a hysteresis with the upper voltage threshold V_{VCCon} for activating the IC. A VCC voltage level dropping below the bottom threshold V_{VCCoff} resets and deactivates the IC during normal operation. In reset state the HV start-up cell is turned on, starting the next VCC charge cycle until VCC voltage exceeds V_{VCCon} (see Chapter 4.1.1).

4.5.2.2 HSVCC undervoltage lockout

The implemented HSVCC undervoltage lockout (UVOFF) ensures a defined activation and deactivation of the floating high-side driver. The HSUVOFF contains a hysteresis with the upper voltage threshold V_{HSVCCon} for activating the high-side gate driver. A HSVCC voltage level dropping below the bottom threshold V_{HSVCCoff} turns off and deactivates immediately the high-side driver. During deactivation phase the high-side driver current consumption is reduced.

4.5.2.3 VCC overvoltage protection

There is an over voltage detection at pin VCC. The detection function consists of a threshold V_{VCCOVP} and a blanking time of t_{VCCOVP}. The protection reaction once the overvoltage protection is triggered can be configured.

4.5.2.4 Brown-in protection

For successful brown-in two conditions must be fulfilled:

1. AC voltage above threshold with $V_{ACrms} > V_{ACrmsbi}$ sensed via pin HV
2. PFC bus voltage above threshold with $V_{bus} > V_{busbi}$ sensed via pin PFCVS

When AC brown-in condition is not met before the timeout duration t_{HVbito} is expired, the AC brown-in time out protection reaction is triggered.

Since the brown-in is also based on the sensed bus voltage, this protection also acts as PFC open-loop protection during start-up.

4.5.2.5 Brown-out protection

Brown-out detection is based on AC peak voltage estimation: In case the PFC is disabled, the AC peak voltage is determined from the bus voltage V_{bus} sensed at pin PFCVS. In case the PFC is enabled the AC peak voltage is determined using the captured PFC switching cycle timings. If the estimated AC peak voltage is below the configurable threshold $V_{ACrmsbo}$ for longer than the blanking time t_{bo}, the protection mode will be triggered and the IC enters brown-in mode. Please be aware, that the blanking time is only counted during active time, so that during burst-mode with sleep phases the duration to detect a brown-out is increased.

Afterwards, as described in Chapter 4.1.2, bang-bang mode is entered for an fast re-start in case AC input voltage comes back.

4.5.2.6 AC loss protection with X-capacitor discharge

In case this feature is enabled, an AC detection algorithm checks via pin HV if there is an alternating AC line voltage voltage during normal operation and burst mode. As soon as the voltage at pin HV stops alternating an AC loss event is detected, the IC goes into protection mode and the HV startup cell is turned on to discharge the X-capacitor until VCC drops below V_{VCCoff}. From then, the controller tries to re-charge VCC to V_{VCCon} for a fast re-start in case AC input voltage comes back (see Chapter 4.1.2).

The X-capacitor discharge and the related protection mechanism can be enabled or disabled by configuration using parameter $EN_{Xcapdischg}$.

4.5.2.7 Start-up timeout protections

After the PFC is activated, the PFC performs a soft-start. In case the softstart cannot be completed within $t_{startPFC}$, the configured protection mode (auto-restart or latch) is entered.

A second start-up time-out function is implemented for the hybrid-flyback output. In case of overload during start-up the output voltage V_{out} may not reach the regulation target voltage, preventing the system from entering regulation. A timeout is detected if the current set-point determined by V_{FB} is not dropping below the current set-point determined by V_{out} start-up control within the maximum time period $t_{startto}$.

4.5.2.8 PFC bus overvoltage protection

The first overvoltage protection (PFCOVP1) threshold is given by the configurable parameter $V_{PFCVSovp1}$. Shortly after this threshold is exceeded, the PFC stops switching. The hybrid-flyback stage continues switching. The PFC resumes operation when the measured voltage falls below the threshold $V_{PFCVSovp1res}$.

A second overvoltage protection mechanism (PFCOVP2) is implemented using an hardware comparator. It protects the system in case the bus voltage increases above the first OVP threshold in very short time without triggering PFCOVP1. The corresponding threshold $V_{PFCVSovp2}$ is a fixed voltage. In case the voltage sensed at PFCCVS exceeds the threshold, no new PFC gate driver pulse is generated. As soon as the voltage at PFCVS is below the threshold $V_{PFCVSovp2}$ again, PFC pulses are generated again.

Neither in case of OVP1 nor in case of OVP2 a protection mode is entered.

4.5.2.9 AC overvoltage protection

The AC overvoltage protection (ACOVP) is also based on the bus voltage measured at PFCVS via external voltage divider. Compared to the bus overvoltage protections OVP1 and OVP2, which only stop PFC from switching (see Chapter 4.5.2.8), the ACOVP stops PFC and hybrid-flyback operation and enters protection mode. In case of AC overvoltage, the PFC stops switching due to OVP2, the bus voltage and thus the voltage at pin PFCVS represent the AC peak. In case the voltage measured at PFCVS is greater than the threshold $V_{PFCVSacovp}$ for longer than the configurable blanking time t_{ACovp} the configured protection mode (auto-restart or latch) is entered.

ACOVP can be enabled or disabled by configuration using parameter EN_{ACovp}.

4.5.2.10 Vbus undervoltage protection

Undervoltage detection of the PFC bus voltage is sensed at the PFCVS pin and acts as protection mechanism for the hybrid-flyback stage.

The bus voltage undervoltage protection compares the voltage at pin PFCVS with the voltage $V_{PFCVSuvp}$ every t_{sample} whereas the value of V_{busuvp} is set to $V_{CrUVPoffset} + V_{Cr,avg}$ representing output voltage but not below a minimum value of $1.5 \cdot V_{Cr,avg}$. The undervoltage protection is blanked with the configurable blanking time t_{busuvp} and is sampled with a time period t_{sample}.

4.5.2.11 PFC overcurrent protection

Once the voltage across the PFC shunt resistor exceeds the over current threshold $V_{PFCCSocp}$ for longer than the blanking time $t_{PFCCSocp}$ the MOSFET gate PFCGD is turned off. Afterwards, the ZCD signal or the PFC maximum period time-out signal initializes the next switching cycle. This protection mechanism is active in every switching cycle.

4.5.2.12 PFC CCM cycle protection

During CCM operation, the magnetizing current in the PFC choke does not decay to zero prior to MOSFET turn on. Quasi-resonant oscillation is missing in the V_{PFCCS} signal before the maximum switching period time-out is reached that turns the MOSFET on. This turn-on event without ZCD oscillation is monitored to protect the PFC converter from continuous CCM operation. Extended CCM operation protection is implemented within FW. If quasi-resonant oscillation is missing in the ZCD signal for longer than the blanking time $t_{PFCCSccm}$ the protection is triggered.

4.5.2.13 Hybrid-flyback overcurrent protection

The hybrid-flyback overcurrent protection contains several detection functions, which protect the application when operating under output overcurrent conditions or when exceeding a primary side peak current (see Figure 21).

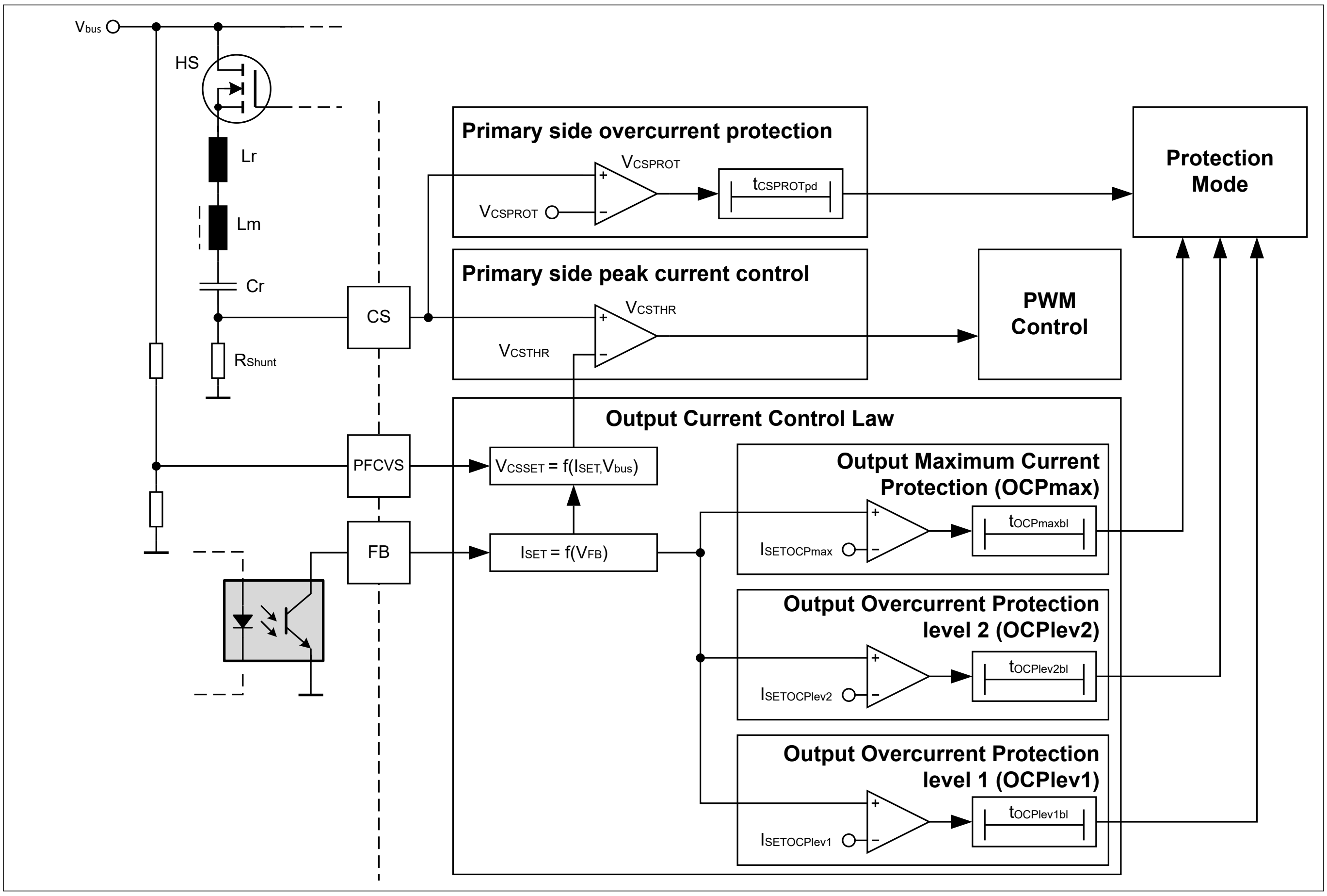

Figure 21 Overcurrent protection overview

4.5.2.13.1 Output overcurrent protection

The output overcurrent protection is implemented as a three level protection:

- Output overcurrent protection level 1
- Output overcurrent protection level 2
- Output maximum current protection

using different overcurrent level thresholds $I_{SETOCPlev1/lev2/max}$ and blanking times $t_{OCPlev1bl/lev2bl/maxbl}$.

The output overcurrent protection levels $I_{SETOCPlev1/lev2/max}$ are defined by the output current control law, whereas $I_{SETOCPmax}$ corresponds to the maximum output current level. Once the current set-point I_{SET} crosses the threshold levels a timer is started. The configured protection mode (auto-restart or latch) is entered when the timer reaches the thresholds $t_{OCPlev1bl/lev2bl/maxbl}$. The timer is reset when I_{SET} is dropping back below the thresholds.

Be aware, that once a higher output current corresponding to a current set point $I_{SET} > I_{SETOCPmax}$ is requested via V_{FB} control, the output current is kept limited. During this phase the output voltage is dropping because output current is higher than what is provided by the converter.

4.5.2.13.2 Primary side overcurrent protection CSPROT

V_{CSPROT} is a fixed threshold at CS pin and beyond the maximum operating range $V_{CSOPmax}$. The CSPROT function is not blanked during the leading edge blanking time t_{HSleb}. Once exceeded the configured protection mode (auto-restart or latch) is entered.

In order to avoid false CSPROT events at the initial start due to charging of the high-side supply an extended, configurable blanking time $t_{CSPROTfilstart}$ applies.

4.5.2.14 Output voltage protection

The IC provides two output voltage Vout protection mechanisms for output undervoltage and output overvoltage to ensure a reliable operation within a defined Vout operating range. The measurement is done at pin ZCD via the reflected voltage at the auxiliary winding of the transformer during the demagnetization phase when the LS switch is turned on (see Figure 22). Furthermore the zero-crossing detection during start-up phase is observed to detect short circuit conditions at the output.

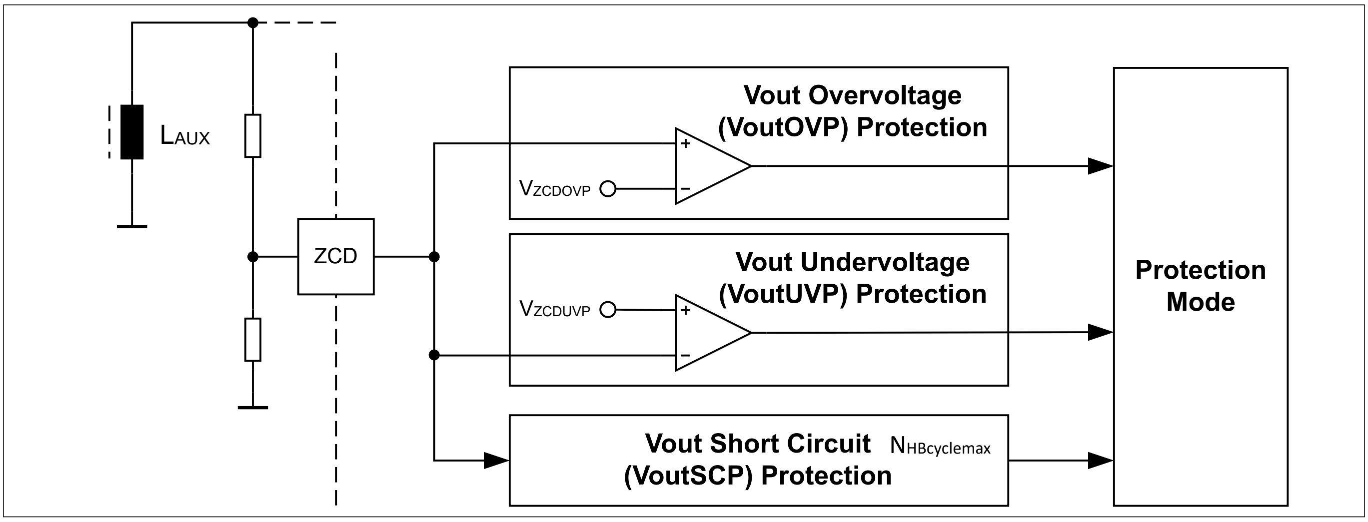

Figure 22 Output voltage protections

4.5.2.14.1 Vout overvoltage protection

The IC provides primary side output over-voltage detection via the voltage measured every switching cycle during the LS on-time at the ZCD-pin from the auxiliary transformer winding. Output over-voltage is detected when the reflected output voltage is exceeding the threshold V_{ZCDovp} (corresponding to the configurable threshold V_{outovp}) longer than the configurable blanking time $t_{outovpbl}$. Once detected a protection mode is immediately triggered and the configured protection mode (auto-restart or latch) is entered.

4.5.2.14.2 Vout undervoltage protection

Output under-voltage detection is detected via the voltage measured at the ZCD-pin. After the start-up is finished Vout under-voltage can triggered when the voltage measured at pin ZCD is dropping below the threshold V_{ZCDuvp}, which corresponds to the configurable threshold V_{outuvp}. Once detected the configured protection mode (auto-restart or latch) is entered.

4.5.2.14.3 Vout short circuit protection

For a short circuit protection at the output, two different mechanisms are implemented. One is only active during start-up, the other one is meant for protection during active operation.

During start-up, the Vout short circuit protection limits the number of half-bridge switching cycles. After a start-up request only a maximum of $N_{HBcyclemax}$ consecutive half-bridge switching cycles without zero-crossing detection are allowed. If $N_{HBcyclemax}$ is exceeded or if the feedback voltage V_{FB} is already below $V_{FBBMctrl}$ the restart phase is stopped and the configured protection mode (prematurely auto-restart mode sleeping phase or latch) is entered.

During operation another Vout short circuit protection mechanism is active using two criteria. If the difference between the actual voltage V_{ZCD} and its internally averaged value V_{ZCDavg} is bigger than the internal threshold $\Delta V_{ZCDshort}$, an output short circuit protection is triggered and the configured protection mode (auto-restart or latch) is entered.

4.5.2.15 CS pin short circuit protection

During Vout start-up a short circuit detection at CS pin is activated for the very first HS switch pulse to protect the application operating with a shortened R_{Shunt}.

4.5.2.16 FB pin start-up protection

During the start-up check phase, the voltage at pin FB is evaluated for error. The system will only start up in case $V_{FB} > V_{FBBMctrl}$. In case the system cannot be started due to too low voltage at pin FB the configured protection event with parameter $EV_{StartFBlow}$ will be triggered.

4.5.2.17 Hybrid-flyback open loop protection

The open control loop protection is using a similar method as the output short protection (see Chapter 4.5.2.14.3). Only in case of a saturated feedback voltage at FB, the reflected output voltage measured via ZCD pin is evaluated: If the difference between the actual voltage V_{ZCD} and its internally averaged value V_{ZCDavg} is bigger than the internal threshold ΔV_{ZCDolp}, which is related to the configurable output voltage threshold ΔV_{outolp}, an open loop protection is triggered and the configured protection mode (auto-restart or latch) is entered.

4.5.2.18 External overtemperature protection

The external overtemperature protection (ExtOTP) is based on measuring an external NTC thermistor at pin MFIO, see Figure 23. Once the external resistance is falling below the threshold $R_{MFIOOTPtrig}$ a protection mode is entered. The protection reaction can be configured. In case of auto-restart, a restart cycle can only take place in case the value of the the external resistance exceeding the threshold $R_{MFIOOTPrel}$. The auto-restart cycles after ExtOTP was triggered are counted. When the number of auto-restarts after external OTP events exceeds the threshold $N_{OTPevmax}$ latch mode is entered, too.

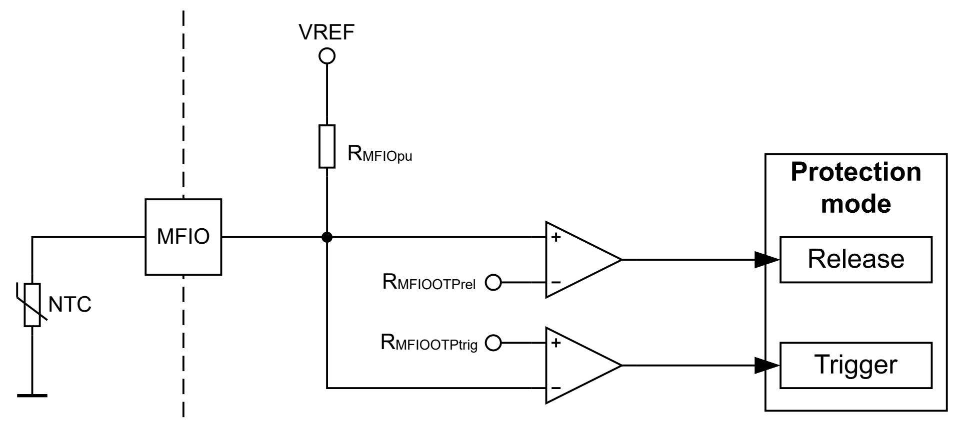

Figure 23 External overtemperature protection using NTC-thermistor at MFIO pin

4.5.3 Error read-out at MFIO-pin

After a latched protection mode as been entered an error code showing which protection has been triggered, can be read out at pin MFIO.

5 Configuration

The configuration of the controller is supported by the GUI tool dpVision provided by Infineon. This chapter gives an overview about the configurable parameters, which are programmable via the UART interface at MFIO pin. Chapter 4.1 shows the relationship between the parameter symbols described in the functional description and the parameter names shown in .dp Vision GUI tool. Furthermore the associated tolerance classes are assigned to the configurable typical parameters, which can be found in Chapter 4.2.

5.1 Configurable parameters and functions

5.1.1 System settings

Table 5 **System settings**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Ratio of resistor divider connected at PFCVS pin and bulk voltage	k_{PFCVS}		[1]			
Maximum nominal output current without over-current condition	I_{outnom}		[1]		A	
Transformer turns ratio of primary winding Np and secondary winding Ns, defined by Np/Ns	N		[1]			
Maximum nominal regulated output voltage	V_{outnom}		[1]		V	

5.1.2 Supply Management

Table 6 **Supply Management**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External resistor connected to HV pin	R_{HV}		[2]		kΩ	
Typical voltage drop from AC terminal to HV pin	$V_{dropAC2HV}$		[2]		V	
Enable X-capacitor discharge	$EN_{Xcapdischg}$		[2]			
Enable of HV cell charging during burst-mode	$EN_{VCCcharge}$		[2]			

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[1] See XDPS2221 parameter file
[2] See XDPS2221 parameter file

5.1.3 Start-up

Table 7 Start-up

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
AC rms voltage for brown-in	$V_{ACrmsbi}$		[3]		V	Tolerance Class: TC_I1 for I_{HVBI}
Brown-in bus voltage threshold	V_{busbi}		[3]		V	Tolerance Class: TC_V1b
Bus voltage threshold for AC overvoltage protection	$V_{busACovp}$		[3]		V	Tolerance Class: TC_V1b
Maximum number of allowed half-bridge switching cycles without subsequent zero-crossing detection (ZCD) during ZCD search phase at Vout start-up	$N_{HBcyclemax}$		[3]			
Maximum time period without zero-crossing detection for generating next pulse only during ZCD search phase	$t_{startzcdto}$		[3]		μs	Tolerance Class: TC_T1
Blanking time of primary overcurrent protection CSPROT at start-up and 1st pulse in burst-mode	$t_{CSPROTfilstart}$		[3]		ns	Tolerance Class: TC_T1

5.1.4 Hybrid-flyback operation

Table 8 Hybrid-flyback operation

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LS switch on-time during energy transfer at V_outnom in ZV-RVS mode	$t_{TRANSnom}$		[4]		µs	
Dead-time between HS pulse falling edge and LS pulse rising edge	t_{deadLS}		[4]		ns	Tolerance Class: TC_T1
Dead-time between LS (ZVS pulse) falling edge and HS pulse rising edge in ZV-RVS mode during start-up	$t_{deadHSRVS}$		[4]		ns	Tolerance Class: TC_T1
HS switch leading edge blanking (LEB) determining minimum on-time (blanking time of CSTHR)	t_{HSleb}		[4]		ns	Tolerance Class: TC_T1
Filtering time between ZCD pulse rising edge and LS pulse rising edge in ZV-RVS mode operation	$t_{ZCDfilRVS}$		[4]		ns	

(table continues...)

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[3] See XDPS2221 parameter file
[4] See XDPS2221 parameter file

Table 8 **(continued) Hybrid-flyback operation**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ZCD pin nominal voltage during LS switch turn-on at V_outnom	V_{ZCDnom}		[4]		V	
Blanking time of CSTHR events	$t_{CSTHRfil}$		[4]		ns	Tolerance Class: TC_T1
Propagation delay compensation time	t_{CSPDC}		[4]		ns	
Minimum switching frequency limit during DCM operation	$f_{swDCMmin}$		[4]		kHz	Tolerance Class: TC_T1
LS gate driver output voltage at high state	$V_{LSGDhigh}$		[4]		V	
t_TRANS in ZV-RVS mode for Vout = 0V in percentage of t_TRANSnom for t_TRANS modulation depending on output voltage	$t_{TRANSRVS0V\%}$		[4]		%	
Target time delay for LS pulse falling edge to ZCD pulse falling edge in CRM	t_{LS2ZCD}		[4]		ns	
Target negative magnetizing current level in percent required to achieve ZVS	$I_{MAGnegnom\%}$		[4]		%	
Maximum negative magnetizing current level in percent required to achieve ZVS at maximum bus voltage Vbus during CRM operation	$I_{MAGnegmaxCRM\%}$		[4]		%	
Maximum negative magnetizing current level in percent required to achieve ZVS at maximum bus voltage Vbus during ZV-RVS mode operation	$I_{MAGnegmaxRVS\%}$		[4]		%	
Minimum ZVS pulse width during ZV-RVS mode operation	t_{ZVSmin}		[4]		ns	Tolerance Class: TC_T1
Minimum FB feedback voltage	$V_{FBOPmin}$		[4]		V	Tolerance class TC_V4a
Pull-up resistor at pin FB	R_{FBpu}		[4]		kΩ	Tolerance ±20%
Minimum peak current for V_ZCD_nom after entering DCM mode in percentage	$I_{MAGposRVSmax\%}$		[4]		%	
Minimum peak current for V_ZCD = 0V after entering DCM mode in percentage	$I_{MAGposRVS0V\%}$		[4]		%	
Absolute minimum peak current after hitting minimum DCM switching frequency in percentage	$I_{MAGposRVSabsmin\%}$		[4]		%	
Offset of peak current used for change from CRM to ZV-RVS mode in percentage of peak current	$I_{MAGposhysteresisCRM2RVS\%}$		[4]		%	

(table continues...)

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[4] See XDPS2221 parameter file

Table 8 (continued) Hybrid-flyback operation

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output voltage threshold for switching over from ZV-RVS mode to CRM	$V_{outRVS2CRM}$		(4)		V	
Output voltage threshold for switching over from CRM to ZV-RVS mode	$V_{outCRM2RVS}$		(4)		V	
Burst mode entry FB feedback voltage threshold	V_{FBBMen}		(4)		V	Tolerance Class: TC_V4a
Pulse width to precharge the bootstrap capacitor after a period longer than tBMslpthrpp	$t_{BMprepulse}$		(4)		µs	Tolerance Class: TC_T1
Number of precharge pulses	$N_{BMprepulse}$		(4)			
Maximum precharge pulse period	$t_{BMppswmax}$		(4)		µs	Tolerance Class: TC_T1
Burst sleep time threshold for enabling precharge pulse	$t_{BMslpthrpp}$		(4)		ms	
Bus voltage jitter enable threshold	$V_{busJitteren}$		(4)		V	Tolerance Class: TC_V1b
Time delay for next frequency jitter step	$t_{Jitterstpdel}$		(4)		ms	Tolerance Class: TC_T3
Frequency jitter spread on a percentage base of switching frequency	$d_{Jitterspread\%}$		(4)		%	

5.1.5 PFC operation

Table 9 PFC operation

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Enable PFC operation (if disabled, PFC is completely and permanently disabled)	$EN_{PFCoperation}$		(5)			
Leading edge blanking time of PFCCS	$t_{PFCCSleb}$		(5)		ns	Tolerance Class: TC_T1
PFC ZCD filter and delay time for comparator low threshold	$t_{PFCCSzcd}$		(5)		ns	
PFC ZCD filter and delay time for comparator high threshold	$t_{PFCCSzcdreset}$		(5)		ns	
PFC ZCD blanking time after PFCGD off	$t_{PFCCSzcdblk}$		(5)		ns	

(table continues...)

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[4] See XDPS2221 parameter file

[5] See XDPS2221 parameter file

Table 9 (continued) PFC operation

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum PFC on-time	$t_{PFConmin}$		[5]		µs	Tolerance Class: TC_T1
Maximum PFC on-time	$t_{PFConmax}$		[5]		µs	Tolerance Class: TC_T1
Minimum PFC switching frequency	$f_{swPFCmin}$		[5]		kHz	Tolerance Class: TC_T1
Maximum PFC switching frequency	$f_{swPFCmax}$		[5]		kHz	Tolerance Class: TC_T1
Lower PFC switching frequency threshold leading to valley transition	$f_{swQRmin}$		[5]		kHz	Tolerance Class: TC_T1
Upper PFC switching frequency threshold leading to valley transition	$f_{swQRmax}$		[5]		kHz	Tolerance Class: TC_T1
Maximum valley number during PFC QRM	$N_{PFCvalleymax}$		[5]			
Blanking time before decreasing valley number	$t_{QRblkdec}$		[5]		ms	Tolerance Class: TC_T3
Blanking time before incrementing valley number	$t_{QRblkinc}$		[5]		ms	Tolerance Class: TC_T3
Configuration for initial soft-start on-time and on-time threshold for pulse skipping	CFG PFContime		[5]			
PFC regulator PI-filter coefficient A during steady state (tracking operation)	PFC_{CoefA}		[5]			
PFC regulator PI-filter coefficient B during steady state (tracking operation)	PFC_{CoefB}		[5]			
PFC regulator T1-filter coefficient during steady state (tracking operation)	PFC_{CoefT1}		[5]			

5.1.6 PFC bus voltage target setting

Table 10 PFC bus voltage target setting

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output power level at which the PFC is enabled	$P_{PFCenable}$		[6]		W	
Output power level at which the PFC is disabled	$P_{PFCdisable}$		[6]		W	

(table continues...)

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[5] See XDPS2221 parameter file

[6] See XDPS2221 parameter file

Table 10 (continued) PFC bus voltage target setting

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Offset of Vbus target voltage setting over 2 x Vcr	$V_{bustarget2Vcroffset}$		[6]		V	
Offset on Vbus for PFC enable condition	$V_{busPFCenable2Vcroffset}$		[6]		V	
Maximum PFC bus target voltage	$V_{bustargetmax}$		[6]		V	Tolerance class: TC_V1b
Minimum PFC bus target voltage	$V_{bustargetmin}$		[6]		V	Tolerance Class: TC_V1b
Offset of Vbus target voltage setting over Vacpk	$V_{bustargetVacpkoffset}$		[6]		V	
Hysteresis on AC peak voltage to disable PFC	$V_{ACpkPFCdisablehysteresis}$		[6]		V	

5.1.7 Protections

Table 11 Protections

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Auto-restart time	t_{ARM}		[7]		s	Tolerance Class: TC_T2
Reaction event to VCC overvoltage protection	EV_{VCCOVP}		[7]			
AC rms voltage threshold for brown-out protection	$V_{ACrmsbo}$		[7]		V	
Enable AC overvoltage protection	EN_{ACovp}		[7]			
Reaction event on AC overvoltage protection	EV_{ACOVP}		[7]			
AC overvoltage protection blanking time	t_{ACovp}		[7]		µs	Tolerance class: TC_T3
Reaction event to low FB-voltage at start-up	$EV_{startFBlow}$		[7]			
Reaction event to start-up no-ZCD protection	$EV_{STNOZCD}$		[7]			
Maximum allowed start-up time until start drop of feedback voltage	$t_{startto}$		[7]		ms	Tolerance Class: TC_T3
Reaction event to PFC soft-start timeout	$EV_{PFCSTTOP}$		[7]			

(table continues...)

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[6] See XDPS2221 parameter file
[7] See XDPS2221 parameter file

Table 11 (continued) Protections

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
PFC bus voltage first level overvoltage protection (OVP1) threshold	$V_{busovp1}$		[7]		V	Tolerance Class: TC_V1b
PFC bus voltage threshold to resume switching after OVP1	$V_{busovp1res}$		[7]		V	Tolerance Class: TC_V1b
Reaction to Vbus undervoltage protection	EV_{busUVP}		[7]			
Offset of dynamic PFC bus undervoltage protection	$V_{CrUVPoffset}$		[7]		V	
Blanking time of bus undervoltage protection (PFCUVP)	t_{busuvp}		[7]		ms	Tolerance Class: TC_T3
Difference of Vbus voltage level to bus undervoltage protection level for enabling max. PFC on-time	$V_{busPFCtonmaxUVP offset}$		[7]		V	
Reaction event for CCM protection	EV_{PFCCCM}		[7]			
CCM protection blanking time	$t_{PFCSccm}$		[7]		ms	Tolerance class: TC_T3
Reaction to output overcurrent protection level 1	$EV_{OCPlev1}$		[7]			
Current set-point in percentage of nominal set-point for output maximum current limitation	$I_{SETOCPmax\%}$		[7]		%	
Current set-point threshold in percentage of nominal set-point for output overcurrent protection level 1	$I_{SETOCPlev1\%}$		[7]		%	
Output overcurrent protection level 1 blanking time	$t_{OCPlev1bl}$		[7]		us	Tolerance Class: TC_T4
Reaction to output overcurrent protection level 2	$EV_{OCPlev2}$		[7]			
Current set-point threshold in percentage of nominal set-point for output overcurrent protection level 2	$I_{SETOCPlev2\%}$		[7]		%	
Output overcurrent protection level 2 blanking time	$t_{OCPlev2bl}$		[7]		ms	Tolerance Class: TC_T3
Reaction event for output maximum overcurrent protection	EV_{OCPmax}		[7]			
Maximum overcurrent limitation blanking time	$t_{OCPmaxbl}$		[7]		ms	Tolerance Class: TC_T3
Reaction event primary side overcurrent protection CSPROT	EV_{CSPROT}		[7]			

(table continues...)

[7] See XDPS2221 parameter file

Table 11 (continued) Protections

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Reaction event to open-loop protection	EV_{OLP}		[7]			
Threshold for difference in output voltage for open loop protection	ΔV_{outolp}		[7]		V	Tolerance Class: TC_V3b for the voltage sampled at pin ZCD
Reaction event to CS pin short protection	EV_{CSSCP}		[7]			
Reaction event for Vout overvoltage protection	$EV_{VoutOVP}$		[7]			
Threshold for Vout overvoltage protection	V_{outovp}		[7]		V	
Vout overvoltage protection blanking time	$t_{outovpbl}$		[7]		ms	Tolerance Class: TC_T3
Reaction event for Vout undervoltage protection	$EV_{VoutUVP}$		[7]			
Threshold for Vout undervoltage protection	V_{outuvp}		[7]		V	Tolerance Class: TC_V3b
Configuration of blanking for output undervoltage protection after burst-mode wake-up	$CFG_{VoutUVPBM}$		[7]			
Reaction event to Vout short-circuit protection	$EV_{VoutSCP}$		[7]			
Reaction event to Vout start-up timeout protection	$EV_{VoutSTTOP}$		[7]			
Threshold for difference in output voltage for output short detection	$\Delta V_{outshort}$		[7]		V	Tolerance Class: TC_V3b for the voltage sampled at pin ZCD
Reaction on external overtemperature protection	EV_{OTP}		[7]			
Overtemperature protection trigger threshold	$R_{MFIOOTPtrig}$		[7]		kΩ	Tolerance class: TC_R1
Overtemperature protection release threshold	$R_{MFIOOTPrel}$		[7]		kΩ	Tolerance class: TC_R2
External overtemperature protection number of allowed triggered events before entering latch mode	$N_{OTPevmax}$		[7]			
Reaction event to watchdog timer protection	EV_{WDOG}		[7]			

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[7] See XDPS2221 parameter file

5.2 Tolerance classes for configurable parameters

The are several configurable parameters available, having different tolerance classes. Parameters defining events, configuration registers, digital numbers or constants are not assigned to tolerance ranges. The available tolerance classes are named with TC_xxx and listed in the following Table 28. Described is how minimum and maximum tolerance values can be derived for the typical value Xtyp of the configurable parameters.

Table 12 Tolerance classes

Tol.-Class	Description	Min. value	Max. value
TC_T1	Timing parameter below 1215ns (based on main clock t_{MCLK} = 15.8 ns(typ.))	t_{typ} x 0.95 - 15.8ns	t_{typ} x 1.05 + 15.8ns
	Timing parameter above 1215ns (based on main clock t_{MCLK} = 15.8 ns(typ.))	t_{typ} x 0.937	t_{typ} x 1.063
	Frequency parameter below 500kHz (based on main clock t_{MCLK} = 15.8 ns(typ.))	F_{typ} x 0.937	F_{typ} x 1.063
TC_T2	Timing parameter based on stand-by clock (t_{STBCLK} = 10 µs(typ.))	t_{typ} x 0.90	t_{typ} x 1.12
TC_T3	Timing parameter (integer multiple of 0.1ms) based on slow task period (t_{STBCLK} = 0.12 ms(typ.)), does not apply in case of burst mode operation.	t_{typ} x 0.937 - 0.13ms	t_{typ} x 1.063 + 0.13ms
TC_T4	Timing parameter (integer multiple of 5ms) based on very slow task period (t_{STBCLK} = 5 ms(typ.)), does not apply in case of burst mode operation.	t_{typ} x 0.937 - 5.5ms	t_{typ} x 1.063 + 5.5ms
TC_V1a	Voltage threshold at pin PFCVS	(V_{VStyp} x 0.994) - 0.099V	(V_{VStyp} x 1.006) + 0.099V
TC_V1b	Voltage threshold at pin PFCVS	(V_{VStyp} x 0.994) - 0.040V	(V_{VStyp} x 1.006) + 0.040V
TC_V2	Voltage threshold for CSTHR comparator at pin CS	$V_{CSTHRtyp}$ - 0.034V	$V_{CSTHRtyp}$ + 0.034V
TC_V3a	Voltage threshold at pin ZCD	(V_{ZCDtyp} x 0.995) - 0.091V	(V_{ZCDtyp} x 1.005) + 0.091V
TC_V3b	Voltage threshold at pin ZCD	(V_{ZCDtyp} x 0.995) - 0.024V	(V_{ZCDtyp} x 1.005) + 0.024V

(table continues...)

Table 12 **(continued) Tolerance classes**

Tol.-Class	Description	Min. value	Max. value
TC_V3c	Voltage change threshold at pin ZCD	V_{ZCDtyp} - 0.077V	V_{ZCDtyp} + 0.077V
TC_V4	Voltage threshold at pin FB	(V_{FBtyp} x 0.984) - 0.084V	(V_{FBtyp} x 1.016) + 0.084V
TC_V4a	Voltage threshold at pin FB	(V_{FBtyp} x 0.984) - 0.026V	(V_{FBtyp} x 1.016) + 0.026V
TC_I1	Current threshold at pin HV	(I_{HVtyp} x 0.98) - 0.004mA	(I_{HVtyp} x 1.02) + 0.004mA

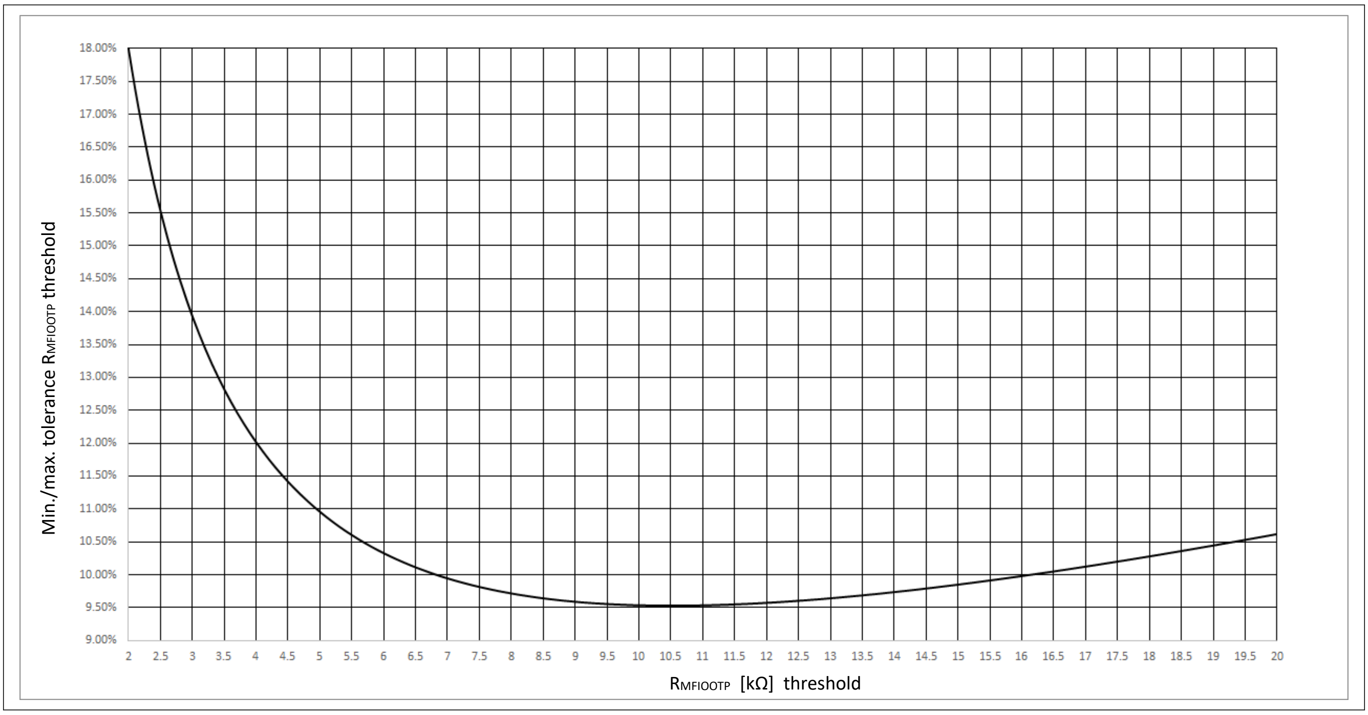

Figure 24 **Tolerance class TC_R1 for resistor threshold at pin MFIO**

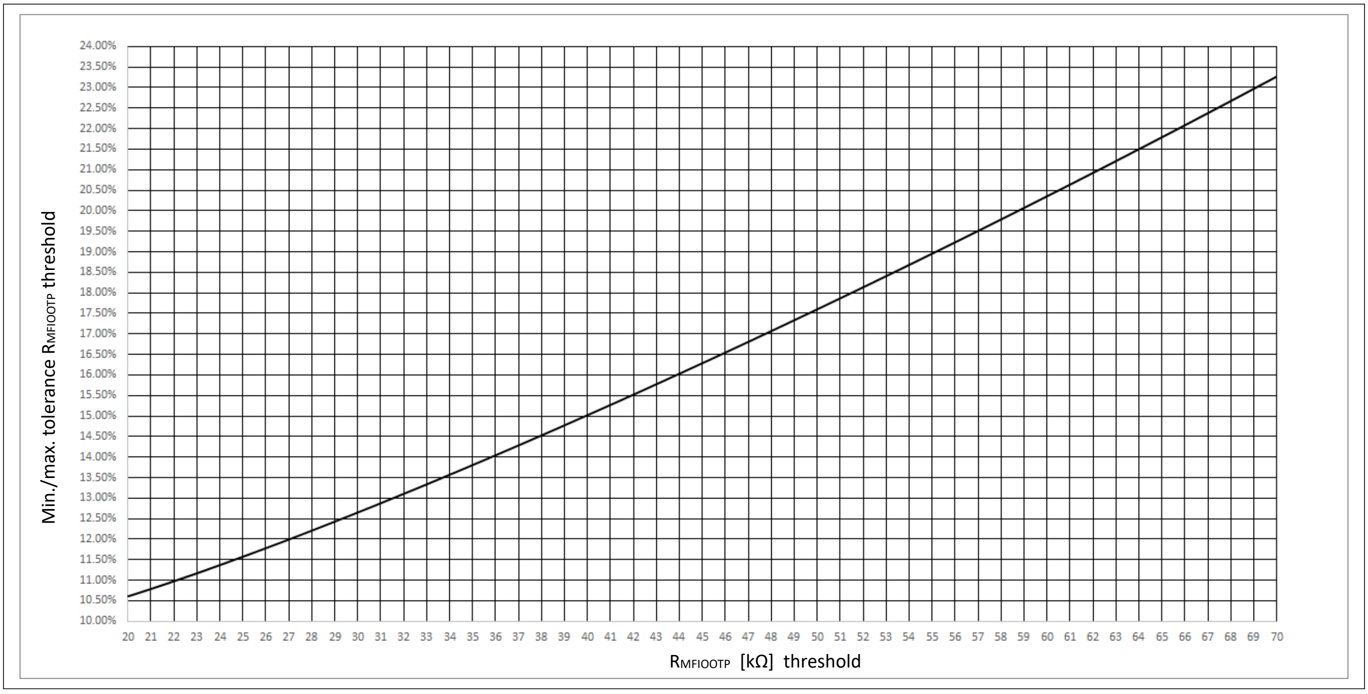

Figure 25 **Tolerance class TC_R2 for resistor threshold at pin MFIO**

Timing parameters relating to external switch events have an offset from system delays that is not included in TC_T1

6 Electrical characteristics

All signals are measured with respect to ground GND pin. The voltage levels are valid if other ratings are not violated.

Figure 26 illustrates the definition for the voltage and current parameters used in this data sheet.

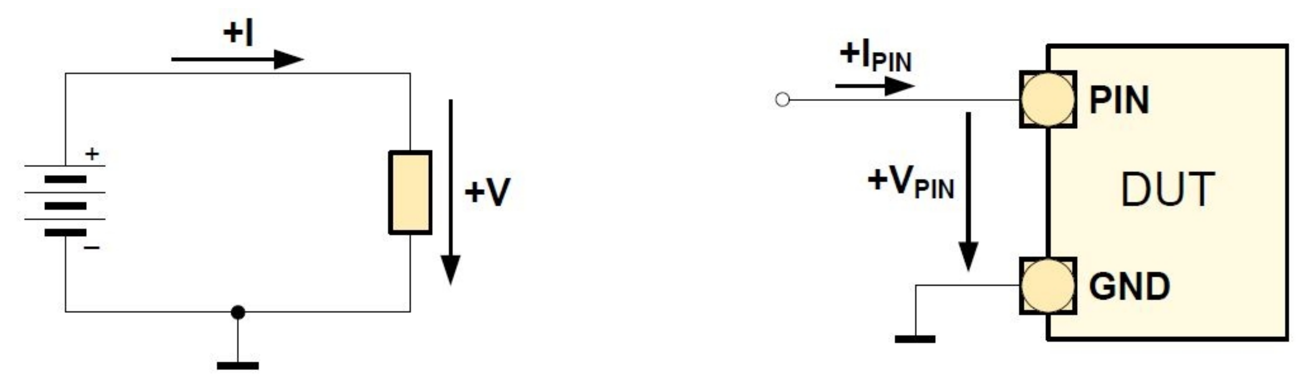

Figure 26 **Voltage and current definitions**

6.1 Absolute maximum ratings

Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for given periods may affect device reliability. Maximum ratings are absolute ratings; exceeding anyone of these values may cause irreversible damage to the device.

Table 13 **Absolute maximum rating**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at pin HV	V_{HV}	–0.3		600	V	[8]
Current into pin HV	I_{HV}	-		10	mA	[8]
Voltage at pin VCC	V_{VCC}	–0.5		26	V	[8]
Voltage at pin MFIO	V_{MFIO}	–0.5		3.6	V	[8]
Voltage at pin PFCVS	V_{PFCVS}	–0.5		3.6	V	[8]
Voltage at pin FB	V_{FB}	–0.5		3.6	V	[8]
Voltage at pin ZCD	V_{ZCD}	–0.5		3.6	V	[8]
Maximum negative transient voltage at pin ZCD	$-V_{ZCDN\_TR}$	-		1.5	V	pulse < 500ns
Maximum permanent negative clamping current for pin ZCD	$-I_{ZCDCLN\_DC}$	-		2.5	mA	RMS
Maximum transient negative clamping current for pin ZCD	$-I_{ZCDCLN\_TR}$	-		10	mA	pulse < 500ns
Voltage at pin CS	V_{CS}	–0.5		3.6	V	[8]
Maximum negative transient voltage at pin CS	$-V_{CSN\_TR}$	-		3	V	pulse < 500ns

(table continues...)

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[8] Permanently applied as DC value.

Table 13 (continued) Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum permanent negative clamping current for pin CS	$-I_{CSCLN\_DC}$	-		2.5	mA	RMS
Maximum transient negative clamping current for pin CS	$-I_{CSCLN\_TR}$	-		10	mA	pulse < 500ns
Maximum permanent positive clamping current for pin CS	I_{CSCLP_DC}	-		2.5	mA	RMS
Maximum transient positive clamping current for pin CS	I_{CSCLP_TR}	-		10	mA	pulse < 500ns
Voltage at pin PFCCS	V_{PFCS}	−0.5		3.6	V	8)
Voltage at pin LSGD	V_{LSGD}	−0.5		V_{VCC}+ 0.3	V	Limited by internal clamping
Voltage at pin PFCGD	V_{PFCGD}	- 0.5		V_{VCC}+ 0.3	V	
Voltage at pin HSGND	V_{HSGND}	-650		650	V	referred to GND
Voltage at pin HSVCC	V_{HSVCC}	−0.5		26	V	referred to HSGND
Voltage at pin HSGD	V_{HSGD}	−0.5		V_{HSVCC}+0.3	V	referred to HSGND
Slew-rate for floating high-side domain	dV_{HS}/dt	−50		50	V/ns	
Junction operation temperature	T_J	−40		125	°C	
Storage temperature	T_S	−55		150	°C	
Maximum power dissipation	P_{TOT}	-		0.63	W	$T_A = 50$ °C, $T_J = 125$ °C, $R_{thJA} = 119$ K/W
Soldering temperature	T_{Sold}	-		260	°C	9) Wave soldering
ESD HBM capability	V_{HBM}	-		2000	V	10) Human body model
ESD CDM capability	V_{CDM}	-		500	V	11) Charged device model
Latch-up capability	I_{LU}	-		150	mA	12) Pin voltages acc. to abs. max. rating
Maximum negative transient voltage at pin PFCCS	$-V_{PFCCSN\_TR}$	-		3	V	pulse < 500ns

(table continues...)

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[8] Permanently applied as DC value.
[9] According to JESD22-A111
[10] According to ANSI/ESDA/JEDEC JS-001
[11] According to JESD22-C101
[12] According to JESD78, 85 °C (Class II) temperature

Table 13 **(continued) Absolute maximum rating**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum permanent negative clamping current for pin PFCCS	$-I_{PFCCSCLN\_DC}$	-		2.5	mA	RMS
Maximum transient negative clamping current for pin PFCCS	$-I_{PFCCSCLN\_TR}$	-		10	mA	pulse < 500ns
Maximum permanent positive clamping current for pin PFCCS	$I_{PFCCSCLP\_DC}$	-		2.5	mA	RMS
Maximum transient positive clamping current for pin PFCCS	I_{CSCLP_TR}	-		10	mA	pulse < 500ns

6.2 Package Characteristics

Table 14 **Package characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance from junction to ambient	R_{thJA}	-		119	K/W	
Creepage distance between HV and HSxxx to GND-related pins	D_{crp}	2.1		-	mm	

6.3 Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Table 15 **Operating range**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction operation temperature	T_J	-25		125	°C	
Voltage at pin HV	V_{HV}	−0.3		600	V	
External voltage at pin VCC	V_{VCC}	11		24	V	Max. value needs to consider internal power losses
Voltage at pin MFIO	V_{MFIO}	−0.3		3.3	V	
Voltage at pin FB	V_{FB}	−0.3		3.3	V	
Voltage at pin ZCD	V_{ZCD}	−0.3		3.3	V	
Voltage at pin CS	V_{CS}	−0.3		3.3	V	
Total current out of pins FB and MFIO	$-I_{FB}-I_{MFIO}$	-		0.63	mA	During sleep phase in burst mode

(table continues...)

Table 15 (continued) Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at pin LSGD	V_{LSGD}	–0.3		V_{VCC} + 0.3	V	Internally clamped at $V_{LSGDhigh}$
Low state output reverse current at pin LSGD	$-I_{LSGDLREV}$	-		100	mA	[13] Applies if V_{LSGD} < 0 V and driver at low state
Voltage at pin HSGD	V_{HSGD}	–0.3		V_{HSVCC} + 0.3	V	Internally clamped at $V_{HSGDhigh}$
Low state output reverse current at pin HSGD	$-I_{HSGDLREV}$	-		100	mA	Applies if V_{HSGD} < 0 V and driver at low state
Voltage at pin HSVCC	V_{HSVCC}	10		24	V	Referred to HSGND
Voltage at pin HSGND	V_{HSGND}	–0.3		600	V	
UART Baudrate at pin MFIO	t_{BD}	10k		115k	Bd	
Voltage at pin PFCVS	V_{PFCVS}	–0.3		3.3	V	
Voltage at pin PFCCS	V_{PFCCS}	–0.3		3.3	V	
Voltage at pin PFCGD	V_{PFCGD}	–0.3		V_{VCC} + 0.3	V	Internally clamped at $V_{PFCGDhigh}$

6.4 Characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature. Typical values represent the median values related to T_A = 25 °C. All voltages refer to GND, and the assumed supply voltage is VCC = 14.0 V if not otherwise specified.

6.4.1 High voltage (HV pin)

Table 16 Electrical characteristics of HV-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HV VCC charge current capability	$I_{HVchargeVCC}$	2.4	5.0	7.5	mA	[14] V_{VCC} = 1 V, V_{HV} = 30 V; Peak current limited in application by external resistor

(table continues...)

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[13] Assured by design.

[14] Max. peak charge current will be limited in the application by an external resistor connected to HV pin.

Table 16 **(continued) Electrical characteristics of HV-pin**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current at HV pin	I_{HVLK}	-		10	µA	V_{HV} = 600 V, HV start-up cell disabled
Brown-in timeout	t_{HVbito}	-	20	-	ms	I_{HVbi} > 0 mA
Brown-in timeout	t_{HVbito}	-	2	-	ms	I_{HVbi} = 0 mA

6.4.2 Power supply (VCC pin)

Table 17 **Electrical characteristics of power supply (VCC pin)**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Turn-on threshold	V_{VCCon}	19.0	20.5	22.0	V	Rising slope
Turn-off threshold	V_{VCCoff}	7.98	8.4	8.82	V	Falling slope
Threshold to activate HV cell for VCC-supply during burst mode	$V_{VCCslpHVon}$	9.97	10.5	11.03	V	Falling slope
UVOFF current	$I_{VCCUVOFF}$	-	20	40	µA	$V_{VCC} < V_{VCCoff(min)} - 0.3$ V
Supply current	$I_{VCCopnm}$	-	11	14.5	mA	Without gate driver gate charge losses and during brown-in phase
Quiescent current during burst mode power saving-phase	$I_{VCCBMpsm0}$	-	0.7	3.4	mA	Burst mode entered; pin MFIO and FB open
Quiescent current during bang-bang mode	I_{VCCBB}	-	0.32	0.58	mA	Protection mode entered; pin MFIO and FB open
Overvoltage protection threshold	V_{VCCOVP}	22.0	23.0	24.0	V	
Overvoltage protection blanking time	t_{VCCOVP}	-	1.0	-	ms	

6.4.3 Floating HS domain (HSGND, HSVCC and HSGD pin)

Table 18 **Electrical characteristics of HS domain pins**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HSVCC turn-on threshold	$V_{HSVCCon}$	8.7	9.2	9.7	V	Rising slope
HSVCC turn-off threshold	$V_{HSVCCoff}$	6.2	6.7	7.2	V	Falling slope

(table continues...)

Table 18 **(continued) Electrical characteristics of HS domain pins**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HSVCC idle current	$I_{HSVCCidle}$	-	0.3	0.8	mA	Without gate driver gate charge losses, VHSVCC = 14 V
HSGD enabling delay time after HSVCC voltage is exceeding turn-on threshold	$t_{HSGDendel}$	-	2.3	4.1	µs	$V_{HSVCC} = 11$ V
HSGD voltage at high state	$V_{HSGDhigh}$	10	11	12	V	$I_{HSGD} = -20$ mA
HSGD voltage at active shutdown	$V_{HSGDaSD}$	-	25	200	mV	$I_{HSGD} = 20$ mA, $V_{HSVCC} = 5$ V
HSGD peak source current	$-I_{HSGDpksrc}$	130	-	-	mA	
HSGD peak sink current	$I_{HSGDpksnk}$	450	-	-	mA	
HSGD driver output low impedance	R_{HSGDLS}	-	-	5	Ω	$I_{HSGD} = 100$ mA

6.4.4 Bus voltage sensing (PFCVS pin)

Table 19 **Electrical characteristics of PFCVS-pin**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	$I_{PFCVSlk}$	–0.2	-	0.2	µA	$0 \text{ V} < V_{PFCVS} < 2.9$ V
Dynamic voltage range	V_{PFCVS}	0.13	-	2.75	V	
Second level overvoltage protection (OVP2) threshold	$V_{PFCVSovp2}$	2.7	2.8	2.9	V	
PFC soft-start timeout	$t_{startPFC}$	-	500	-	ms	

6.4.5 PFC current sense and zero crossing detection (PFCCS pin)

Table 20 **Electrical characteristics of PFCCS pin**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Over-current protection (OCP) threshold	$V_{PFCCSocp}$	594	627	660	mV	
Over-current protection (OCP) blanking time	$t_{PFCCSocp}$	37.5	47.4	58.1	ns	
ZCD comparator logic "0" threshold	$V_{PFCCSzcd}$	0.42	0.54	0.66		
ZCD comparator logic "1" threshold	$V_{PFCCSzcdreset}$	1.41	1.53	1.65	V	

6.4.6 Hybrid-flyback zero crossing detection (ZCD pin)

Table 21 Electrical characteristics of ZCD pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	I_{ZCDlk}	–10	-	10	µA	V_{ZCD} = 0 V / 3.0 V
Maximum pin voltage threshold for Vout overvoltage protection	$V_{ZCDOVPmax}$	-	2.75	-	V	
Zero-crossing detection threshold	V_{ZCDTHR}	15	40	70	mV	Falling slope
Delay from falling edge ZCD and HS pulse rising edge	t_{ZCD2HS}	-	190	-	ns	
Input voltage negative clamping	$-V_{ZCDCLN}$	140	180	220	mV	

6.4.7 Multifunctional input and output (MFIO pin)

Table 22 Electrical characteristics of MFIO-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-up resistor	R_{MFIOpu}	-	11	-	kΩ	During active phase
Open circuit output voltage	V_{MFIOoc}		V_{REF}		V	During active phase
Input high current with active weak pull-down	$-I_{MFIOhpd}$	90	-	300	uA	Measured at min. V_{MFIOIH}
Leakage current	I_{MFIOlk}	-5	-	1	uA	V_{MFIO} = 0 V / 3.0 V
Input capacitance	C_{MFIOIN}	-	-	10	pF	
Input threshold for logic “0”	V_{MFIOIL}	-	-	1	V	
Input threshold for logic “1”	V_{MFIOIH}	2	-	-	V	
Output voltage for logic “0”	V_{MFIOOL}	-	-	0.8	V	I_{MFIOOL} = 2 mA
Output voltage for logic “1”	V_{MFIOOH}	2.2	-	-	V	I_{MFIOOH} = –2 mA
Output sink current	I_{MFIOOL}	-	-	2	mA	
Output source current	$-I_{MFIOOH}$	-	-	2	mA	
Output rise time (0 → 1)	$t_{MFIOrise}$	-	-	25	ns	20 pF load
Output fall time (1 → 0)	$t_{MFIOfall}$	-	-	25	ns	20 pF load

6.4.8 Hybrid-flyback current sensing (CS pin)

Table 23 **Electrical characteristics of CS-pin**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	I_{CSlk}	–10	-	10	µA	0 V < VCS < 2.8 V
Maximum operating current range	$V_{CSTHRmax}$	394	426	458	mV	
CSTHR propagation delay	$t_{CSTHRpd}$	121	213	305	ns	input signal slope, dVCS/dt = 150 mV/µs
CSPROT threshold	V_{CSPROT}	550	600	650	mV	
CSPROT propagation delay	$t_{CSPROTpd}$	125	135	190	ns	dVCS/dt = 100 V/µs

6.4.9 Hybrid-flyback output feedback (FB pin)

Table 24 **Electrical characteristics of FB-pin**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Open circuit output voltage	V_{FBoc}	3.04	3.2	3.36	V	
Threshold maximum usable range	$V_{FBOPmax}$	-	-	2.428	V	
Burst mode wake-up threshold	$V_{FBBMctrl}$	510	581	604	mV	During sleep phase in burst mode

6.4.10 Low-side gate driver (LSGD pin)

Table 25 **Electrical characteristics of LSGD-pin**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at active shutdown	$V_{LSGDaSD}$	-	-	1.6	V	I_{LSGD} = 5 mA, V_{VCC} = 5 V
Peak sink current	$I_{LSGDpksnk}$	500	-	-	mA	V_{LSGD} = 4.0 V
Peak source current	$-I_{LSGDpksrc}$	-	120	-	mA	
Driver output low impedance	R_{LSGDLS}	-	-	7.0	Ω	I_{LSGD} = 100 mA

6.4.11 PFC gate driver (PFCGD pin)

Table 26 Electrical characteristics of PFCGD-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nominal output high voltage	$V_{PFCGDhigh}$	9.9	10.5	11.1	V	I_{PFCGD} = –20 mA
Voltage at active shutdown	$V_{PFCGDaSD}$	-	-	1.6	V	I_{PFCGD} = 5 mA, V_{VCC} = 5 V
Peak sink current	$I_{PFCGDpksnk}$	800	-	-	mA	V_{PFCGD} = 4.0 V
Peak source current	$-I_{PFCGDpksrc}$	-	360	-	mA	
Driver output low impedance	$R_{PFCGDLS}$	-	-	4.4	Ω	I_{PFCGD} = 100 mA

6.4.12 Central control functions

Table 27 Electrical characteristics of central control functions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDP power supply	V_{VDDP}	3.04	3.2	3.36	V	
VREF reference voltage	V_{VREF}	2.391	2.428	2.465	V	
Main clock oscillation period time base	t_{MCLK}	15	15.8	16.6	ns	
Stand-by clock oscillation period time base	t_{STBCLK}	9	10	11.2	µs	
Slow task period time base	$t_{SLWTASK}$	111	120	129	µs	
Very slow task period time base	$t_{VSLWTASK}$	4.68	5	5.32	ms	
Sampling time period	t_{sample}		$t_{SLWTASK}$		µs	
Restart step time base for auto-restart mode	$t_{ARMbase}$	270	300	336	ms	$EN_{Xcapdischg}$ = Disabled; Base for configurable auto-restart time tARMslp when auto-restart mode entered
Restart step time base for auto-restart mode	$t_{ARMbase}$	27	30	34	ms	$EN_{Xcapdischg}$ = Enabled; Base for configurable auto-restart time t_{ARMslp} when auto-restart mode entered.

(table continues...)

Table 27 **(continued) Electrical characteristics of central control functions**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Limited maximum change in on-time control for HS switch during CRM operation	$\Delta t_{HSonmaxCRM}$	75	80	85	ns	CRM operation, t_{HSon} not limited by V_{CSSET}, only applies for small V_{bus}
Blanking time for brown-out protection	t_{bo}	-	70	-	ms	
Safe X-capacitor discharge time between AC off and X-capacitor voltage no longer above 60V	$t_{XCapdischg}$	-	-	2.0	s	$EN_{Xcapdischg}$ = Enabled, $C_{X,max}$ = 2.0 uF, R_{HV} = 48 ... 54 kΩ, diode drop below 2.0 V

7 Package dimensions

You can find all of our packages, sorts of packing and others in our Infineon internet page “Products: http://www.infineon.com/products”.

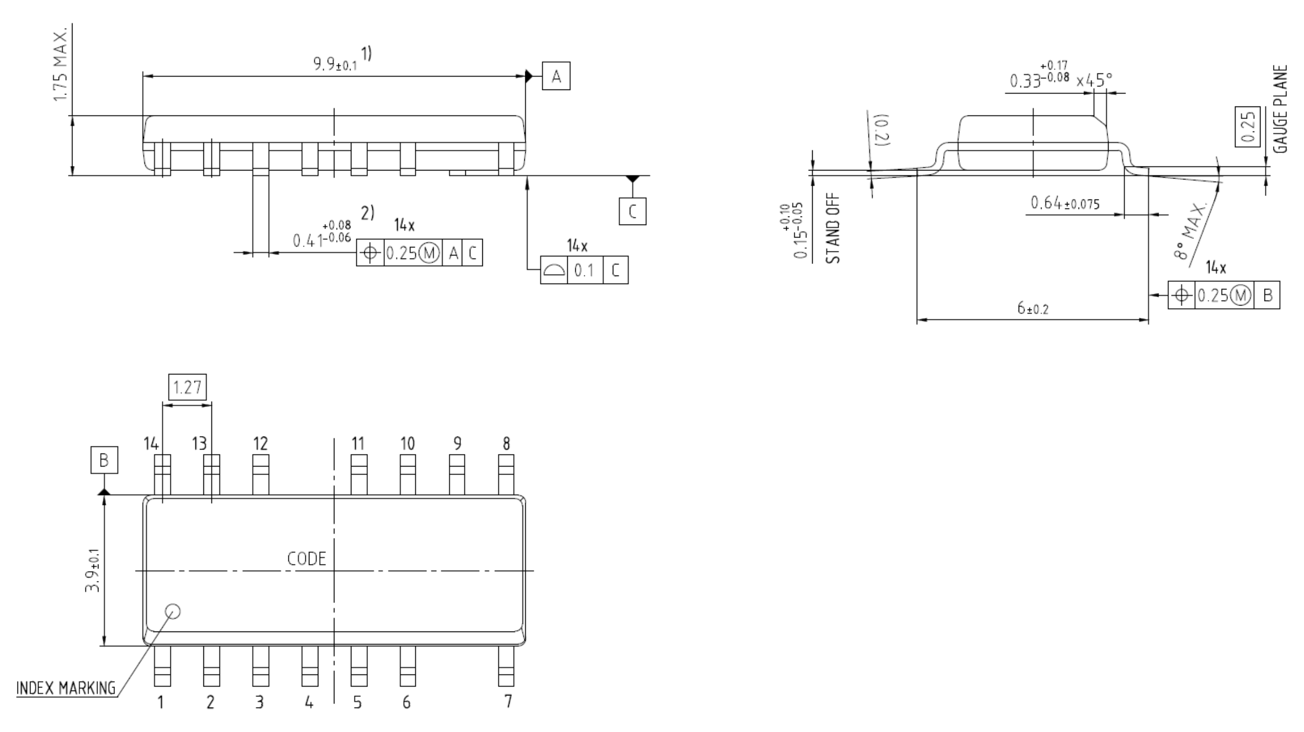

Figure 27 PG-DSO-14 outline

Description
Dimensions:
e = 1.27
A = 5.69
L = 1.31
B = 0.65

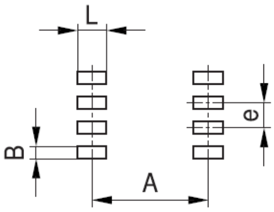

Figure 28 PG-DSO-14 footprint

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pbfree finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

8 Revision history

Document version	Date of release	Description of changes
Rev 1.0	2022-10-13	Initial release

8 Revision history

Document version	Date of release	Description of changes
Rev 1.1	2022-11-09	• Added firmware version to "Ordering Information" • Refined X-capacitor discharge description • Corrections in chapter 4.3 • Corrections in configurable parameter tables • Corrections in electrical characteristics

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Edition 2022-11-09

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-wpg1663764152324

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