19-3322; Rev 0; 8/04

MAXIM

I²C-Compatible Real-Time Clocks with µP Supervisor and NV RAM Controller

General Description

The MAX6909/MAX6910 are I²C-compatible real-time clocks (RTCs) with a microprocessor supervisor, optional trickle charger (MAX6910 only), backup power source, and NV RAM controller. The MAX6909/MAX6910 provide alarm outputs to indicate a crystal failure, a switchover to battery power, and time and date indication. The NV RAM is 31 bytes of static RAM that are available for scratchpad storage. The MAX6909/MAX6910 are controlled through a 2-wire serial bus.

The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date is automatically adjusted for months with fewer than 31 days, including corrections for leap year up to the year 2100. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. A time/date-programmable ALARM output completes the features list for the real-time clock section of the MAX6909/MAX6910. The alarm function can also be used in a polled mode by periodically reading the alarm out status bit in the minutes register. A crystal fail output, $\overline{\text{CX FAIL}}$, indicates loss of accurate timekeeping due to crystal problems.

A built-in µP supervisor with an open-drain reset ensures the µP powers up in a known state. A reset threshold is available for 3V or 3.3V supplies. The piezo transducer output, PZT, is register selectable for one of four frequencies, can be turned on and off through a register bit, or selected to go on when the $\overline{\text{ALM}}$, alarm output, goes active.

The MAX6909/MAX6910 are available in a 20-pin QSOP package and operate over the -40°C to +85°C temperature range.

Applications

Point-of-Sale Equipment

Programmable Logic Controller

Handheld Instruments

Medical Instrumentation

Features

- **RTC Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year, with Leap Year Compensation Valid Up to 2100**
- **31 Bytes of RAM for Scratchpad Data Storage**
- **Uses Standard 32.768kHz, 6pF Load, Watch Crystal**
- **Programmable Time/Date, Open-Drain ALARM Output (Status Can also Be Polled)**
- **Chip Enable Gating (Control of $\overline{\text{CE}}$ with Reset and Power Valid)**
- **OUT Pin for SRAM Power**
- **µP Reset Output**
- **Watchdog Input**
- **Manual Reset Input with Push-Button Switch Debounce**
- **Independent Power-Fail and Reset Comparators**
- **400kHz 2-Wire Interface**
- **Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock Registers or RAM**
- **Bus Timeout to Prevent Lockup of Malfunctioning Bus Interface**
- **Dual Power-Supply Pins for Primary and Backup Power**
- **Programmable Trickle Charger (MAX6910)**
- **Uses Less than 1µA Timekeeping Current at 3.0V**
- **Operating Voltages of 3V and 3.3V**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6909EO30	-40°C to +85°C	20 QSOP
MAX6909EO33	-40°C to +85°C	20 QSOP
MAX6910EO30	-40°C to +85°C	20 QSOP
MAX6910EO33	-40°C to +85°C	20 QSOP

Pin Configuration/Selector Guide/Typical Operating Circuit appear at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

All Voltages (with respect to GND)
BATT or V_{CC} ..... -0.3V to +6.0V
OUT, $\overline{ALM}$, SCL, SDA, $\overline{CX\ FAIL}$, $\overline{PFO}$, $\overline{RESET}$ ..... -0.3V to +6.0V
All Other Pins ..... -0.3V to (V_{SUP} + 0.3V)
(where V_{SUP} is greater of V_{BATT} or V_{CC})
Input Current
V_{CC} 500mA
BATT 100mA
GND 20mA
Output Current
OUT Continuous 450mA
All Other Outputs 20mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin QSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	MAX69__EO30 (Note 3)		2.7		3.3	V
		MAX69__EO33 (Note 3)		3.0		3.6	
Operating Voltage Range BATT	V_{BATT}	MAX69__EO30 (Note 4)		2.0		3.6	V
		MAX69__EO33 (Note 4)		2.0		3.6	
BATT Current (Note 5)	I_{BATT}	Crystal fail-circuit disabled	V_{BATT} = 2V, V_{CC} = 0V			0.75	µA
			V_{BATT} = 3V, V_{CC} = 0V			0.95	
			V_{BATT} = 3.6V, V_{CC} = 0V			1.1	
Timekeeping Current (Note 5)	I_{BATT}	Crystal fail-circuit enabled	V_{BATT} = 2V, V_{CC} = 0V			0.9	µA
			V_{BATT} = 3V, V_{CC} = 0V			4	
			V_{BATT} = 3.6V, V_{CC} = 0V			9	
Active Supply Current (Note 6)	I_{CCA}	PZT disabled, crystal-disabled	V_{CC} = 3.3V, V_{BATT} = 0V			0.14	mA
			V_{CC} = 3.6V, V_{BATT} = 0V			0.15	
Standby Current (Note 5)	I_{CCS}	PZT disabled, crystal-disabled	V_{CC} = 3.3V, V_{BATT} = 0V			7	µA
			V_{CC} = 3.6V, V_{BATT} = 0V			7	
Standby Current (Note 5)	I_{CCS}	Crystal fail-circuit enabled	V_{CC} = 3.3V, V_{BATT} = 0V			18	µA
			V_{CC} = 3.6V, V_{BATT} = 0V			25	
Trickle-Charge Diode Voltage Drop (Two Diodes)					1.2		V
Trickle Charge Resistors	R1				1.7		kΩ
	R2				2.8		
	R3				5.0		
OUT							
OUT in Battery-Backup Mode (Note 4)	V_{OUT}	V_{BATT} = 3.0V, V_{CC} = 0V, I_{OUT} = 20mA		V_{BATT} - 0.15		V_{BATT} - 0.1	V
		V_{BATT} = 2.0V, V_{CC} = 0V, I_{OUT} 10mA		V_{BATT} - 0.1		V_{BATT} - 0.05	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT in V_{CC} Mode (Note 4)	V_{OUT}	V_{CC} = 3.0V, V_{BATT} = 0V, I_{OUT} = 100mA	V_{CC} - 0.15	V_{CC} - 0.1		V
		V_{CC} = 2.7V, V_{BATT} = 0V, I_{OUT} = 50mA	V_{CC} – 0.1	V_{CC} - 0.05		
V_{BATT} to V_{CC} Switchover Threshold	V_{TRU}	Power-up (V_{CC} < V_{RST}) switch from V_{BATT} to V_{CC} (Note 7)		V_{BATT} + 0.05		V
V_{CC} to V_{BATT} Switchover Threshold	V_{TRD}	Power-down (V_{CC} < V_{RST}) switch from V_{CC} to V_{BATT} (Note 7)		V_{BATT} - 0.05		V
$\overline{CE\ IN}$ AND $\overline{CE\ OUT}$						
$\overline{CE\ IN}$ Leakage Current		Disabled, V_{CC} < V_{RST}, $V_{\overline{CE\ IN}}$ = V_{CC} or GND	-1		+1	µA
$\overline{CE\ IN}$ to $\overline{CE\ OUT}$ Resistance		V_{CC} = $V_{CC(min)}$, V_{IH} = 0.9V_{CC}, V_{IL} = 0.1V_{CC}		70	140	Ω
$\overline{CE\ IN}$ to $\overline{CE\ OUT}$ Propagation Delay		50Ω source impedance driver, C_{LOAD} = 10pF, V_{CC} = $V_{CC(MIN)}$, V_{IH} = 0.9V_{CC}, V_{IL} = 0.1 V_{CC} (Note 8), measured from 50% point on $\overline{CE\ IN}$ to the 50% point on $\overline{CE\ OUT}$		5	15	ns
$\overline{RESET}$ (or RESET) Active to $\overline{CE\ OUT}$ disabled and pulled to V_{OUT} Delay	t_{RCE}	$\overline{MR}$ low to high, $V_{CC(MIN)}$ < V_{CC} < $V_{CC(MAX)}$	2	10	50	µs
$\overline{CE\ OUT}$ Enabled and Connected to $\overline{CE\ IN}$ After V_{CC} > V_{RST}	t_{RP}		140	200	280	ms
$\overline{CE\ OUT}$ High ($\overline{RESET}$ or RESET Active)	V_{OH}	V_{CC} = 0V, I_{OUT} = -100µA, V_{BATT} = 2V	0.95 x V_{OUT}			V
MANUAL RESET INPUT						
$\overline{MR}$ Input Threshold	V_{IL}				0.3 × V_{CC}	V
	V_{IH}		0.7 × V_{CC}			
$\overline{MR}$ Internal Pullup Resistance				50		kΩ
$\overline{MR}$ Minimum Pulse Width			1			µs
$\overline{MR}$ Glitch Immunity		(Note 8)			50	ns
$\overline{MR}$ to Reset Delay		(Note 8)		200	350	ns
POWER-FAIL INPUT AND POWER-FAIL OUTPUT						
PFI Input Threshold	V_{PFT}	V_{CC} = $V_{CC(MIN)}$	1.19	1.27	1.31	V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PFI Input Current				-100	+2	+100	nA
PFI to PFO Delay		(Note 8)	PFI rising	0.06	0.2	2.2	µs
			PFI falling	2.4	5	12	
PFI Hysteresis	V_{PFH}	PFI rising			30		mV
$\overline{PFO}$ Output Voltage High	V_{OH}	I_{SOURCE} = 200µA, PFI = V_{CC} = $V_{CC(MIN)}$		0.9 × V_{CC}			V
$\overline{PFO}$ Output Voltage Low	V_{OL}	I_{SINK} = 1.2mA, V_{BATT} = 2V, PFI = V_{CC} = 0V				0.2	V
WATCHDOG INPUT							
Watchdog Timeout Period Initial	t_{WD}	Before first WDI edge, after reset timeout		1.00	1.6	2.25	s
Watchdog Timeout Period	t_{WD}	Register select—long		1.00	1.6	2.25	s
	t_{WDS}	Register select—short		140	200	280	ms
Minimum WDI Input Pulse Width	t_{WDI}			100			ns
WDI Input Threshold	V_{IL}					0.3 × V_{CC}	V
	V_{IH}			0.7 × V_{CC}			
WDI Input Current	I_{IL}	V_{WDI} = V_{CC} or GND		-100		+100	nA
PZT OUTPUT							
PZT Output Short-Circuit Current (V_{CC} Must Be > V_{RST} for PZT to Be Active)	I_{PZT}	MAX69_ _EO30	Sink current	5		18	mA
			Source current	5		20	
		MAX69_ _EO33	Sink current	6		20	
			Source current	6.5		25	
PZT Frequency 1	PZT_{f1}				1024		Hz
PZT Frequency 2	PZT_{f2}				2048		Hz
PZT Frequency 3	PZT_{f3}				4096		Hz
PZT Frequency 4	PZT_{f4}				8192		Hz
PZT Off-Leakage Current	I_{OLKG}			-1		+1	µA
CRYSTAL-FAIL OUTPUT							
$\overline{CX\ FAIL}$ Output Low Voltage	V_{OL}	V_{BATT} = 2.0V, V_{CC} = 0V, I_{OL} = 3mA			0.1	0.2	V
		V_{CC} = 2.7V, I_{OL} = 5mA, V_{BATT} = 0V				0.25	
$\overline{CX\ FAIL}$ Off-Leakage Current	I_{OLKG}			-1		+1	µA
ALARM OUTPUT							
$\overline{ALM}$ Output Low Voltage	V_{OL}	I_{OL} = 3mA, V_{BATT} = 2.0V, V_{CC} = 0V				0.2	V
		I_{OL} = 5mA, V_{CC} = 2.7V, V_{BATT} = 0V				0.25	
$\overline{ALM}$ Off-Leakage Current	I_{OLKG}			-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BATTERY ON OUTPUT							
$\overline{BATT\ ON}$ Output Low Voltage	V_{OL}	V_{BATT} = 2.0V, I_{OL} = 3mA, V_{CC} = 0V				0.2	V
		V_{BATT} = 2.7V, I_{OL} = 5mA, V_{CC} = 0V				0.25	
$\overline{BATT\ ON}$ Off-Leakage Current	I_{OLKG}			-1		+1	µA
RESET FUNCTION							
Reset Threshold	V_{RST}	MAX69_ _EO33		2.80	2.93	3.00	V
		MAX69_ _EO30		2.50	2.63	2.70	
V_{RST} Hysteresis	V_{HYST}				10		mV
V_{CC} Falling Reset Delay		V_{CC} falling from $V_{RST(MAX)}$ to $V_{RST(MIN)}$ at 10V/ms, measured from the beginning of V_{CC} falling to RESET asserting high			10	50	µs
Reset Active Timeout Period	t_{RP}			140	200	280	ms
$\overline{RESET}$ Output Low Voltage	V_{OL}	Reset asserted	I_{OL} = 1.6mA, V_{BATT} = 2.0V, V_{CC} = 0V			0.2	V
$\overline{RESET}$ Off-Leakage Current	I_{LKG}			-1		+1	µA
RESET Output High Voltage	V_{OH}	Reset asserted	I_{OH} = 50µA, V_{CC} = 1.0V, V_{BATT} = 0V	0.8 × V_{CC}			V
			I_{OH} = 1mA, V_{CC} = 2V, V_{BATT} = 0V	0.9 × V_{CC}			
RESET Output Low Voltage	V_{OL}	V_{CC} = $V_{CC(MIN)}$, I_{OL} = 1.6mA			0.032	0.1	V
2-WIRE DIGITAL INPUTS (SCL, SDA) ($V_{CC(MIN)}$ < V_{CC} < $V_{CC(MAX)}$)							
Input High Voltage	V_{IH}			0.7 × V_{CC}			V
Input Low Voltage	V_{IL}					0.3 × V_{CC}	V
Input Hysteresis	V_{HYS}				0.05 × V_{CC}		V
Input Leakage Current		V_{IN} = GND or V_{CC}		-1		+1	µA
Input Capacitance		(Note 8)				10	pF
Output Low Voltage	V_{OL}	I_{OL} = 4mA, V_{CC} = $V_{CC(MIN)}$				0.4	V

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AC ELECTRICAL CHARACTERISTICS

($V_{CC(MIN)}$ < V_{CC} < $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE BUS TIMING						
SCL Clock Frequency	f_{SCL}	(Note 9)	0.32		400.00	kHz
Bus Timeout	$t_{TIMEOUT}$		1		2	s
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
Hold Time After (Repeated) START Condition; After This Period, the First Clock Is Generated	$t_{HD:STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 10, 11)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
SCL Low to Data Out Valid	$t_{VD:DAT}$	(Note 8)	50			ns
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
SCL/SDA Rise Time	t_R	(Note 12)	20 + 0.1 x C_B		300	ns
SCL/SDA Fall Time (Receiving)	t_F	(Notes 12, 13)	20 + 0.1 x C_B		300	ns
SCL/SDA Fall Time (Transmitting)	t_F	(Notes 12, 13)	20 + 0.1 x C_B		250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 8)			50	ns
Capacitive Load of Each Bus Line	C_B				400	pF

Note 1: V_{RST} is the reset threshold for V_{CC}. See the *Ordering Information*.
Note 2: All parameters are 100% tested at T_A = +85°C. Limits over temperature are guaranteed by design and not production tested.
Note 3: 2-wire serial interface is operational for V_{CC} > V_{RST}.
Note 4: See the *Detailed Description* section (BATT function).
Note 5: I_{BATT} and I_{CCS} are specified with SDA and SCLK pulled high, OUT floating, and $\overline{CE\ OUT}$ floating.
Note 6: 2-wire serial interface operating at 400kHz, SDA pulled high.
Note 7: For OUT switch over to BATT, V_{CC} must fall below V_{RST} and V_{BATT}. For OUT switchover to V_{CC}, V_{CC} must be above V_{RST} or above V_{BATT}.
Note 8: Guaranteed by design. Not production tested.
Note 9: Due to the 2-wire bus timeout feature, there is a minimum specification on the SCL clock frequency based on a 31-byte burst-mode transaction to RAM. See the *Timeout Feature* section.
Note 10: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ min}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
Note 11: The maximum $t_{HD:DAT}$ only has to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 12: C_B = total capacitance of one bus line in pF.
Note 13: The maximum t_F for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_F is specified at 250ns. This allows series protection resistors to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_F.

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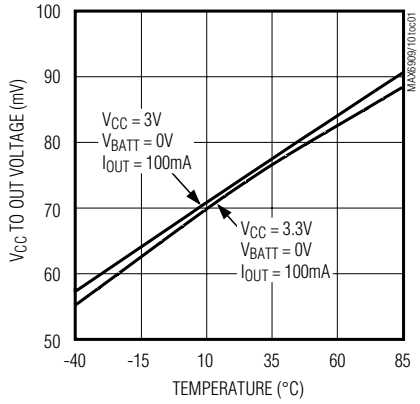
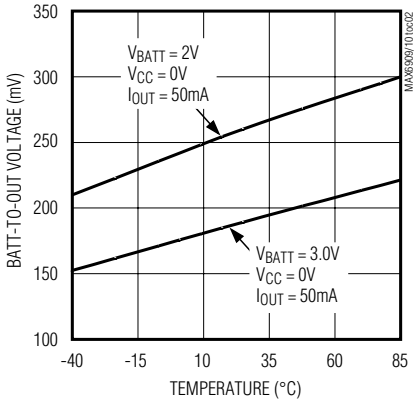
Typical Operating Characteristics

(V_{CC} = 3.3V, V_{BATT} = 3V, T_A = +25°C, unless otherwise noted.)

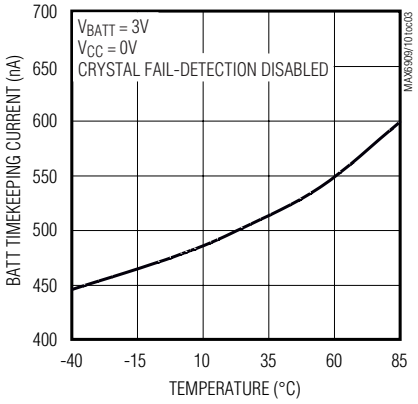
V_{CC} TO OUT VOLTAGE vs. TEMPERATURE



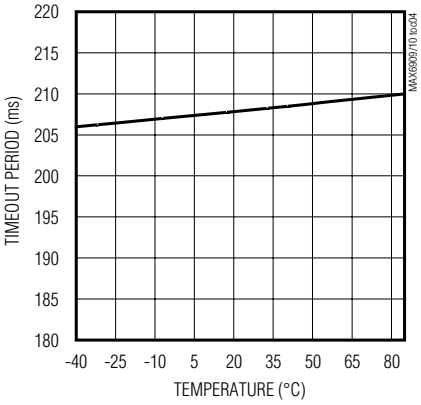
BATT-TO-OUT VOLTAGE vs. TEMPERATURE



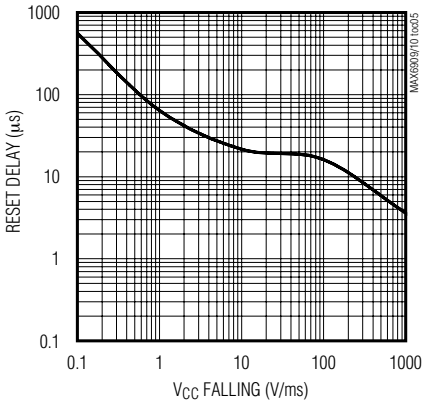
BATT TIMEKEEPING CURRENT vs. TEMPERATURE



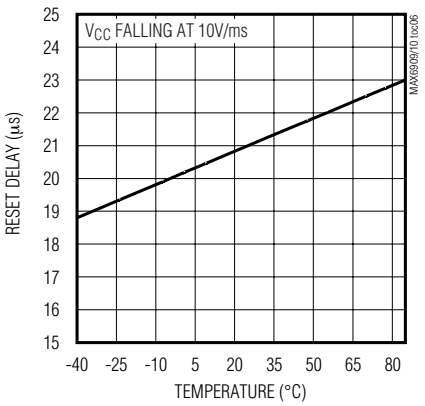
RESET TIMEOUT PERIOD vs. TEMPERATURE



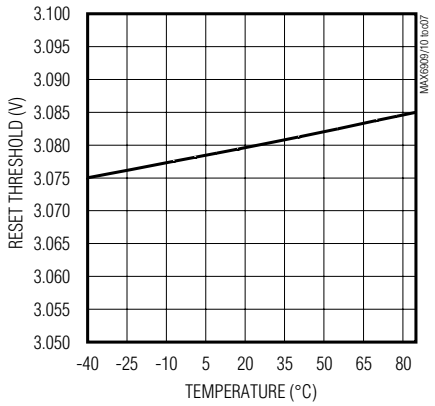
RESET COMPARATOR DELAY vs. V_{CC} FALLING



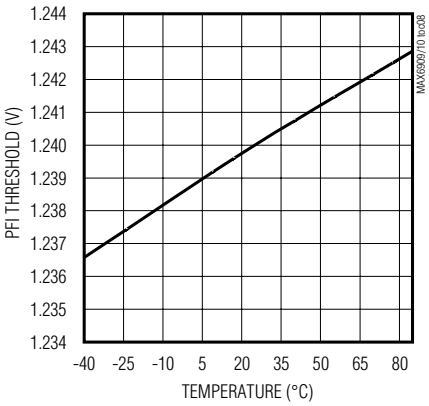
RESET COMPARATOR DELAY vs. TEMPERATURE



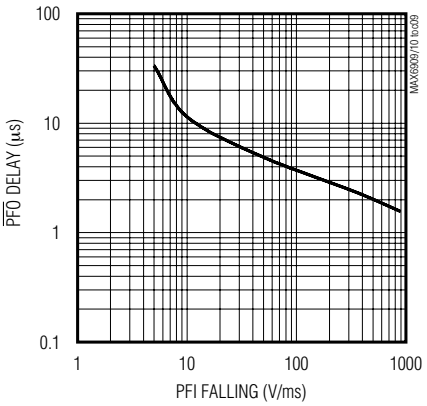
RESET THRESHOLD vs. TEMPERATURE



PFI THRESHOLD vs. TEMPERATURE



PFI-TO-$\overline{PFO}$ DELAY vs. PFI FALLING

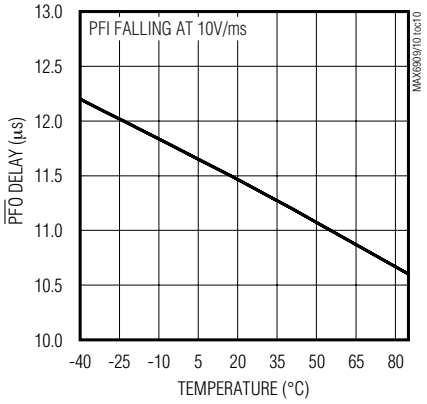


I²C-Compatible Real-Time Clocks with µP Supervisor and NV RAM Controller

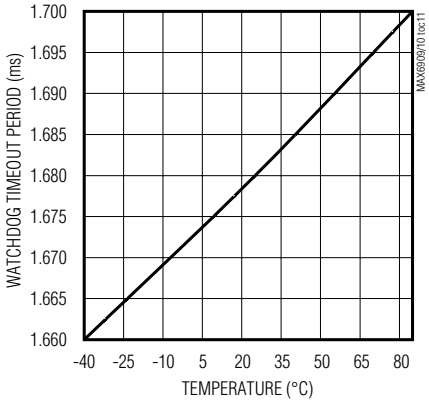
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{BATT} = 3V, T_A = +25°C, unless otherwise noted.)

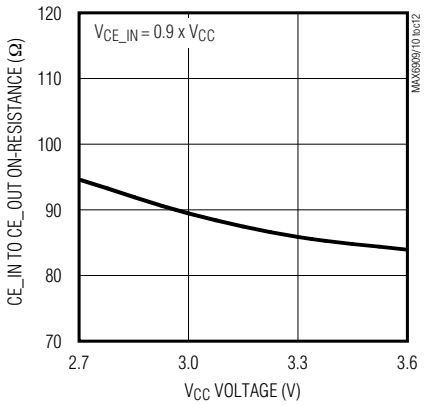
PFI-TO-$\overline{PFO}$ DELAY vs. TEMPERATURE



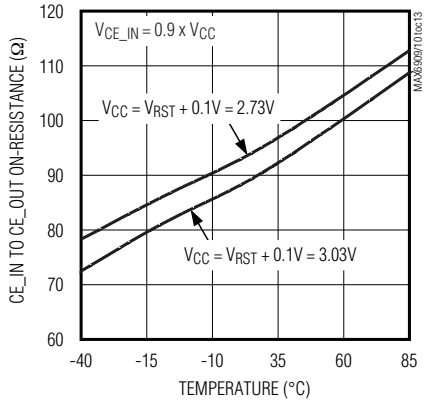
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



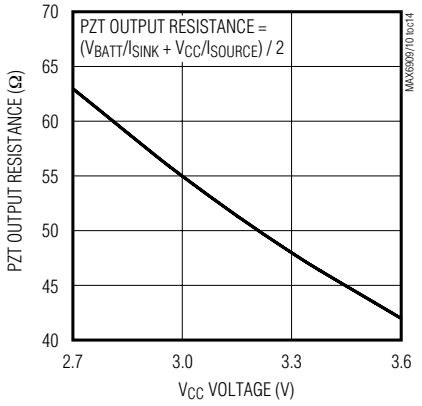
CE_IN TO CE_OUT ON-RESIGTANCE vs. V_{CC}



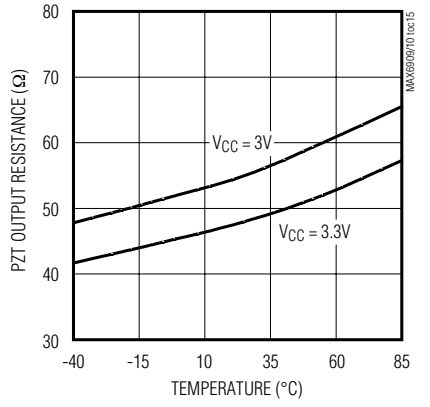
CE_IN TO CE_OUT ON-RESISTANCE vs. TEMPERATURE



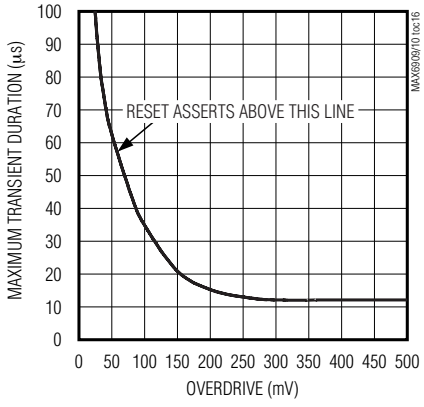
PZT OUTPUT RESISTANCE vs. V_{CC}



PZT OUTPUT RESISTANCE vs. TEMPERATURE



MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE



Pin Description

PIN	NAME	FUNCTION
1	BATT	Backup Battery Input. When V_{CC} falls below the reset threshold and V_{BATT}, OUT connects to BATT. Connect BATT to GND if no backup battery supply is used.
2	OUT	Supply Output for CMOS RAM or Other ICs Requiring Use of Backup Battery Power. Bypass to GND with at least a 0.1µF capacitor.
3	$\overline{\text{BATT ON}}$	Logic Output Open Drain. $\overline{\text{BATT ON}}$ is low when the MAX6909/MAX6910 are powered from BATT.
4	$\overline{\text{CE IN}}$	Chip-Enable Input. Input to the chip-enable switch used for external RAM. Connect to V_{CC} if unused.
5	PFI	Power-Fail Comparator Input. For monitoring external power supplies.
6	$\overline{\text{MR}}$	Manual Reset Input. The active-low input has an internal pullup resistor. Internal debouncing circuitry ensures noise immunity. Leave open if unused.
7	WDI	Watchdog Input
8	GND	Ground
9	X1	32.768kHz Crystal Pin; Oscillator Input
10	X2	32.768kHz Crystal Pin; Oscillator Output
11	$\overline{\text{CX FAIL}}$	Crystal Fail Output. Open drain, active low.
12	SDA	Serial Data Line. Data input/output connection for the 2-wire serial interface.
13	SCL	Serial Clock Line. Clock input connection for the 2-wire serial interface.
14	$\overline{\text{ALM}}$	Alarm Output. Open drain, active low.
15	PZT	Piezo Transducer Output. Push-pull Piezo transducer output.
16	$\overline{\text{PFO}}$	Power-Fail Comparator Output. Push-pull active low.
17	$\overline{\text{CE OUT}}$	Chip-Enable Output. For controlling external RAM.
18	$\overline{\text{RESET}}$	Open-Drain, Active-Low Reset Output
19	RESET	Push-Pull, Active-High Reset Output. Complement of $\overline{\text{RESET}}$.
20	V_{CC}	Main Supply Input. Bypass to GND with at least a 0.01µF capacitor.

Detailed Description

The MAX6909/MAX6910 contain eight 8-bit timekeeping registers, two burst address registers, a trickle charge register, a control register, a configuration register, an alarm configuration register, and seven alarm threshold registers, all controlled through a 2-wire serial interface. Figure 1 is the MAX6909/MAX6910 block diagram.

The OUT pin supplies voltage for CMOS RAM or other ICs requiring the use of backup battery power. When V_{CC} rises above the reset threshold (V_{RST}) or above V_{BATT}, OUT is connected to V_{CC}. When V_{CC} falls below V_{RST} and V_{BATT}, BATT is connected to OUT. If enabled, an on-board trickle charger charges BATT from V_{CC}. BATT can act as a backup supply from either a battery or SuperCap™. When operating from BATT, the battery-on output ($\overline{\text{BATT ON}}$) is pulled low and can be used as an indicator of operation in battery backup mode.

SuperCap is a trademark of Baknor Industries.

There are two reset outputs, $\overline{\text{RESET}}$ and RESET. They become active while V_{CC} is below the reset threshold (V_{RST}) or while manual reset ($\overline{\text{MR}}$) is held low, and for t_{RP} after $\overline{\text{MR}}$ goes high, V_{CC} rises above the reset threshold, or a WDI pulse is not received when the watchdog function is enabled. Reset thresholds are available for 3V and 3.3V applications. See the *Ordering Information* for specifics. $\overline{\text{MR}}$ is internally pulled high and contains debounce circuitry to accommodate a manual pushbutton reset switch. The WDI, when enabled, keeps RESET and $\overline{\text{RESET}}$ from becoming active if it is strobed once every t_{WDS} or t_{WD}. The watchdog timeout is selectable in the configuration register.

Other features include internal chip-enable gating logic, which accepts a valid $\overline{\text{CE IN}}$ from a microprocessor and only gates it through as valid to $\overline{\text{CE OUT}}$ when the MAX6909/MAX6910 are not in a reset state. This can be used for disabling CMOS RAM to limit current consumption when OUT is switched to BATT.

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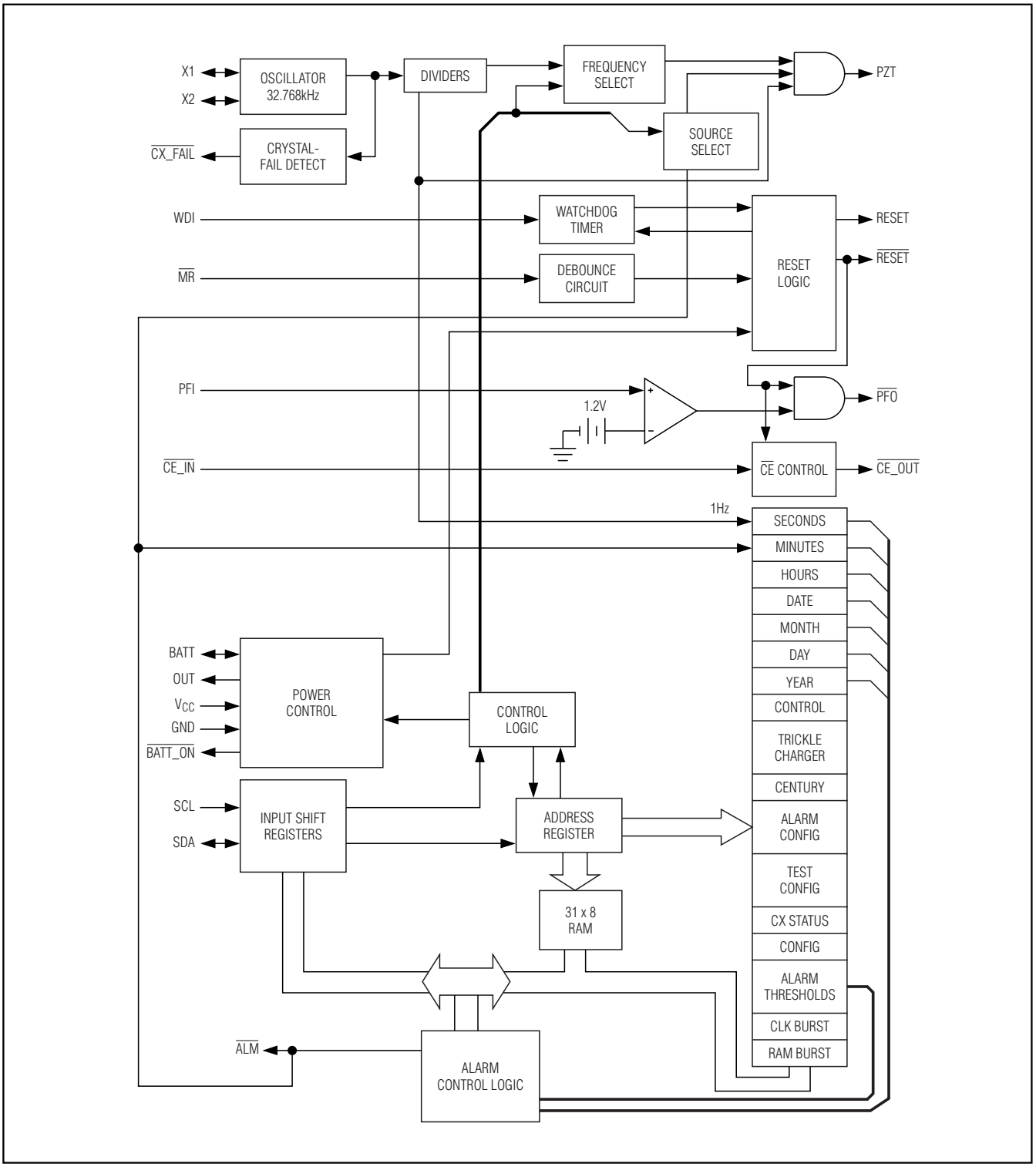

Figure 1. MAX6909/MAX6910 Block Diagram

A power-fail comparator is available to monitor other system voltages through PFI and report the status through $\overline{PFO}$. If the MAX6909/MAX6910 are in reset, $\overline{PFO}$ is low; otherwise, it is high as long as PFI is greater than 1.27V (typ).

The piezo transducer drive output (PZT) has register-selectable frequencies of 1.024kHz, 2.048kHz, 4.096kHz, or 8.192kHz. This output can be selected to become active when the alarm is triggered or can be independently controlled through the configuration register. When activated, the PZT outputs a frequency with an attention-getting 1Hz duty cycle of 50% on and 50% off.

An on-chip crystal oscillator maintaining circuit, for use with a 32.768kHz crystal, provides the clock for timekeeping functions. A crystal fail output ($\overline{CX\ FAIL}$) alerts the user when the 32.768kHz crystal oscillator has failed for 30 cycles (typ), resulting in conditions that produce invalid timekeeping data. The crystal fail function can also be polled by reading the status bit in the CX status register.

Crystal Selection

A 32.768kHz crystal is connected to the MAX6909/MAX6910 through pins 9 and 10 (X1 and X2). The crystal selected for use should have a specified load capacitance (C_L) of 6pF where the capacitive load is included in the MAX6909/MAX6910. When designing the PC board, keep the crystal as close to the X1 and X2 pins as possible. Keep the trace lengths short and small and place a guard ring around the crystal and connect the ring to GND to reduce capacitive loading and prevent unwanted noise pickup. Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling. Finally, an additional local ground plane on an adjacent PC board layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane should be isolated from the regular PC board ground plane, should be no larger than the perimeter of the guard ring, and connected to the GND pin of the MAX6909/MAX6910. Ensure that this ground plane does not contribute to significant capacitance between signal line and ground on the connections that run from X1 and X2 to the crystal. Figure 2 shows the recommended crystal layout.

Some crystal manufacturers and part numbers for their SMT, 32.768kHz watch crystals that require 6pF loads are listed in Table 1. In addition, these manufacturers offer other package options depending upon the specific application considerations.

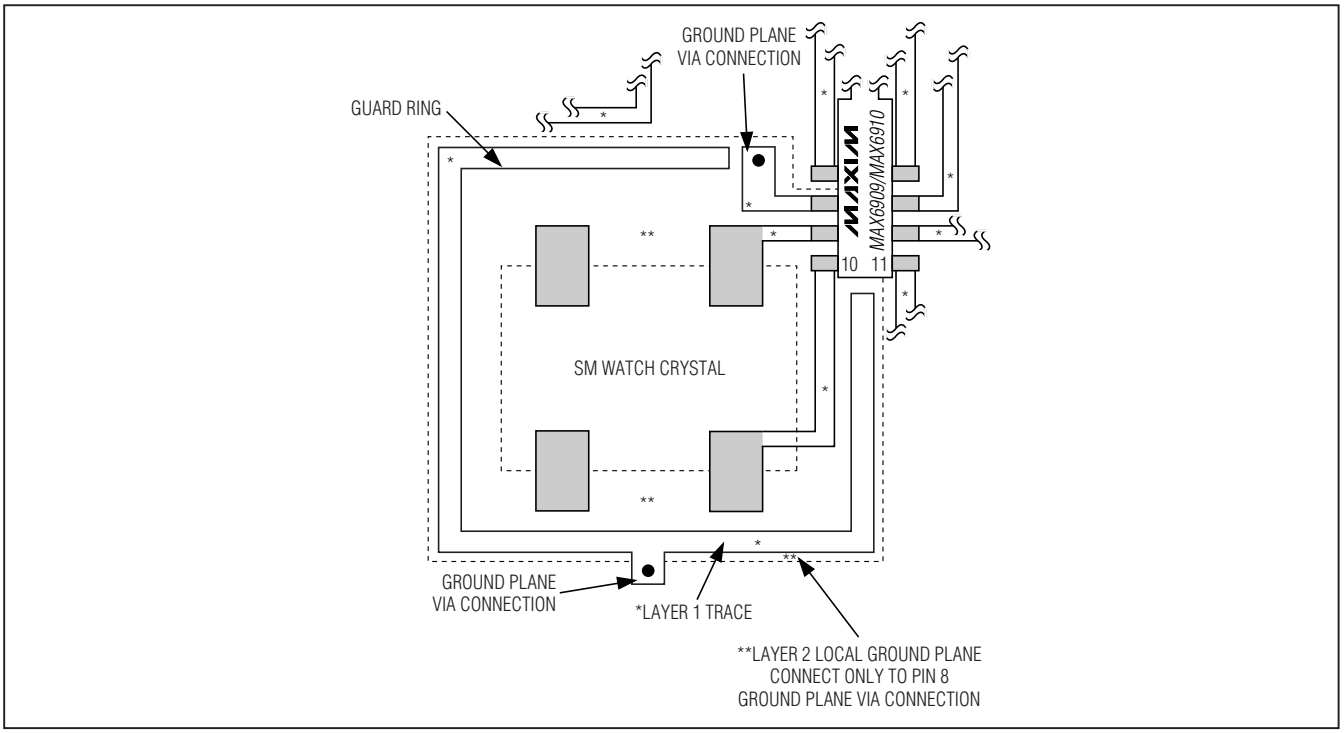

Figure 2. Recommended Crystal Layout

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Table 1. Crystal Manufacturers and Part Numbers

MANUFACTURER	PART	TEMP RANGE (°C)	C_L (pF)	+25°C FREQUENCY TOLERANCE (ppm)
Caliber Electronics	AWS2A-32.768KHz, AWS2B-32.768KHz	-20 to +70	6	±20
ECS INC International	ECS-.327-6.0-17	-10 to +60	6	±20
Fox Electronics	FSM327	-40 to +85	6	±20
M-tron	SX2010/ SX2020	-20 to +75	6	±20
Raltron	RSE-32.768-6-C-T	-10 to +60	6	±20

Timekeeping accuracy of the MAX6909/MAX6910 is dependent on the frequency stability of the external crystal. To determine frequency stability, use the parabolic curve of Figure 3 and the following equations:

$$\Delta f = f \times k \times (T_0 - T)^2$$

where:

Δf = change in frequency from +25°C (Hz)

f = nominal crystal frequency (Hz)

k = parabolic curvature constant (-0.035 ±0.005ppm/°C² for 32.768kHz watch crystals)

T_0 = turnover temperature (+25°C ±5°C for 32.768kHz watch crystals)

T = temperature of interest (°C)

For example: What is the worst-case change in oscillator frequency from +25°C ambient to +45°C ambient?

$$\Delta f_{drift} = 32{,}768Hz \times (-0.04ppm/°C)^2 \times (20°C - 45°C)^2 = -0.8192Hz$$

What is the worst-case timekeeping error per second?

1) Error due to temperature drift:

$$\Delta t_{drift} \{[1 / [(f + \Delta f_{drift}) / 32{,}768]] - 1s\} / 1s$$

$$\Delta t_{drift} \{[1 / [(32{,}768Hz - 0.8192Hz) / 32{,}768]] - 1s\} / 1s = 0.000025s / s$$

2) Error due to +25°C initial crystal tolerance of ±20ppm:

$$\Delta f_{initial} = 32{,}768Hz \times (-20ppm) = -0.65536Hz$$

$$\Delta t_{initial} = \{[1 / [(f + \Delta f_{initial}) / 32{,}768]] - 1\} / 1s$$

$$\Delta t_{initial} = \{[1 / [32{,}768 - 0.65536 / 32{,}768]] - 1\} / 1s = 0.000020s / s$$

3) Total timekeeping error per second:

$$\Delta t_{total} = \Delta t_{drift} + t_{initial}$$

$$\Delta t_{total} = 0.000025s / s + 0.000020s / s = 0.000045 s / s$$

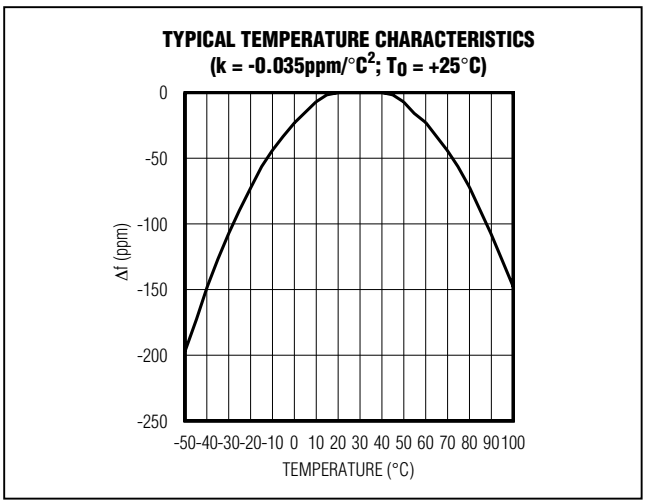

Figure 3. Frequency Stability and Temperature

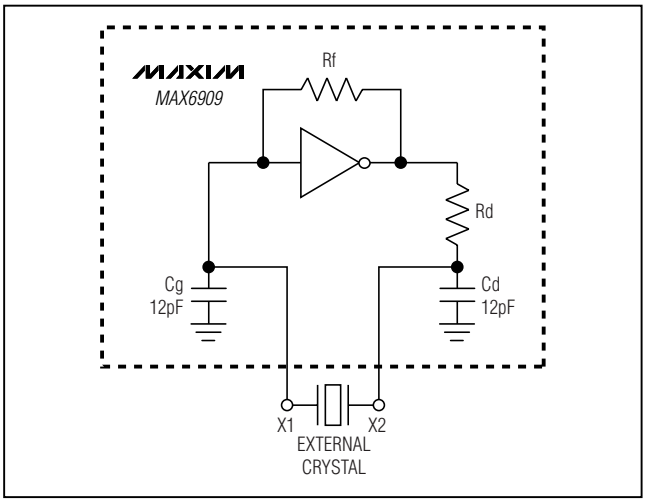

Figure 4. Oscillator Functional Schematic

Table 2. Acceptable Quartz Crystal Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Frequency	f		32.768		kHz
Equivalent series resistance (ESR)	R_S			60	kΩ
Parallel load capacitance	C_L		6		pF
Q factor	Q	40,000			

After 1 month that translates to:

$$\Delta t = (31\text{day}) \times \left(24\frac{\text{hr}}{\text{day}}\right) \times \left(60\frac{\text{min}}{\text{hr}}\right) \times \left(60\frac{\text{s}}{\text{min}}\right) \times \left(0.000045\text{s/s}\right) = 120.158\text{s}$$

Total worst-case timekeeping error at the end of 1 month at +45°C is approximately 120s or 2min (assumes negligible parasitic layout capacitance). Figure 5 shows the register address definition. Table 3 is the hex register address/description.

Control Register (Write Protect Bit)

Bit 7 of the control register is the write protect bit. The lower 7 bits (bits 0–6) are forced to zero and always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

Hours Register (AM-PM/12-24 Mode)

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20h–23h).

Clock Burst

Addressing the clock burst register specifies burst mode operation. In this mode, the first seven clock/calendar registers and the control register can be consecutively read or written starting with bit 7 of address BEh for a write and BFh for a read. If the write protect bit is set high when a write clock/calendar burst mode is specified, no data transfer occurs to any of the seven clock/calendar registers or the control register. When writing to the clock registers in the burst mode, all eight registers must be written in order for the data to be transferred. In addition, the WP bit in the control register must be set to zero prior to a clock burst write.

RAM

The static RAM is 31 bytes addressed consecutively in the RAM address space. Even address/commands (C0h–FCh) are used for writes, and odd address/commands (C1h–FDh) are used for reads. The contents of the RAM are static and remain valid for V_{OUT} down to 1.5V (typ).

RAM Burst

Addressing the RAM burst register specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written starting with bit 7 of address FEh for a write and FFh for a read. When writing to RAM in burst mode, it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to is transferred to RAM regardless of whether all 31 bytes are written.

Trickle Charge Register (MAX6910)

The trickle charge register controls the trickle charger characteristics of the MAX6910. The trickle charger functional schematic (Figure 6) shows the basic components of the trickle charger. Table 4 details the bit settings for trickle charger control. Trickle charge selection (TCS) bits D7–D4 control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 enables the trickle charger. All other patterns disable the trickle charger. The MAX6910 powers up with the trickle charger disabled. The diode select (DS) bits (D3–D2) select whether two diodes or no diodes are connected between V_{CC} and BATT. If DS is 10, no diode is selected; if DS is 01, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independent of the state of the TCS bits. The RS bits (D1–D0) select the resistor that is connected between V_{CC} and BATT. If both RS bits are set to zero, the trickle charger is disabled, regardless of any other bit states in the trickle charger register. RS bits set to 10 select a 1.7K, 01 selects 2.9K, and 11 select 5K.

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REGISTER ADDRESS

FUNCTION	A7	A6	A5	A4	A3	A2	A1	A0
SEC	1	0	0	0	0	0	0	RD /W
MIN	1	0	0	0	0	0	1	RD /W
HR	1	0	0	0	0	1	0	RD /W
DATE	1	0	0	0	0	1	1	RD /W
MONTH	1	0	0	0	1	0	0	RD /W
DAY	1	0	0	0	1	0	1	RD /W
YEAR	1	0	0	0	1	1	0	RD /W
CONTROL	1	0	0	0	1	1	1	RD /W
TRICKLE CHARGER	1	0	0	1	0	0	0	RD /W
CENTURY	1	0	0	1	0	0	1	RD /W
ALARM CONFIG	1	0	0	1	0	1	0	RD /W
TEST CONFIG	1	0	0	1	0	1	1	RD

REGISTER DEFINITION

VALUE	D7	D6	D5	D4	D3	D2	D1	D0
00-59	0	10 SEC			1 SEC			
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
00-59	ALM OUT	10 MIN			1 MIN			
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
00-23	12/24	0	10 HR	10 HR	1 HR			
01-12	1/0		A/P 0/1					
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
01-12	0	0	0	10 M	1 MONTH			
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
01-07	0	0	0	0	0	WEEKDAY		
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
00-99	10 YEAR				1 YEAR			
***POR STATE**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
	WP	0	0	0	0	0	0	0
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	TCS	TCS	TCS	TCS	DS	DS	RS	RS
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
00-99	1000 YEAR				100 YEAR			
***POR STATE**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**
	OSC FAIL EN	YEAR	DAY	MONTH	DATE	HOUR	MIN	SEC
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	0	0	0	0	0	1	1	1
***POR STATE**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**

NOTE: *POR STATE DEFINES POWER-ON RESET STATE OF REGISTER CONTENTS. THE TEST CONFIG REGISTER IS A READ-ONLY REGISTER.

Figure 5. Register Address Definition (Sheet 1 of 2)

REGISTER ADDRESS

FUNCTION	A7	A6	A5	A4	A3	A2	A1	A0
CX STATUS	1	0	0	1	1	0	0	RD/W
CONFIG	1	0	0	1	1	0	1	RD/W
ALARM THRESHOLDS:								
SEC	1	0	0	1	1	1	0	RD/W
MIN	1	0	0	1	1	1	1	RD/W
HR	1	0	1	0	0	0	0	RD/W
DATE	1	0	1	0	0	0	1	RD/W
MONTH	1	0	1	0	0	1	0	RD/W
DAY	1	0	1	0	0	1	1	RD/W
YEAR	1	0	1	0	1	0	0	RD/W
CLOCK BURST	1	0	1	1	1	1	1	RD/W
RAM								
RAM 0	1	1	0	0	0	0	0	RD/W
⋮								⋮
RAM 30	1	1	1	1	1	1	1	RD/W
RAM BURST	1	1	1	1	1	1	1	RD/W

REGISTER DEFINITION

VALUE	D7	D6	D5	D4	D3	D2	D1	D0
	CX FAIL	0	0	0	0	0	0	0
*POR STATE	0	0	0	0	0	0	0	0
	WD EN	0	0	WD TIME	PZT SEL	PZT CNTL	PZT REFQ	PZT FREQ
*POR STATE	0	0	0	0	0	0	0	0
00-59	0	10 SEC			1 SEC			
*POR STATE	0	1	1	1	1	1	1	1
00-59	0	10 MIN			1 MIN			
*POR STATE	0	1	1	1	1	1	1	1
00-23	12/24	0	10 HR	10 HR	1 HR			
01-12	1/0		A/P 0/1					
*POR STATE	1	0	1	1	1	1	1	1
01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
*POR STATE	0	0	1	1	1	1	1	1
01-12	0	0	0	10 M	1 MONTH			
*POR STATE	0	0	0	1	1	1	1	1
01-07	0	0	0	0	0	WEEKDAY		
*POR STATE	0	0	0	0	0	0	0	0
00-99	10 YEAR				1 YEAR			
*POR STATE	1	1	1	1	1	1	1	1
RAM DATA 0	X	X	X	X	X	X	X	X
⋮								⋮
RAM DATA 30	X	X	X	X	X	X	X	X

NOTE: *POR STATE DEFINES POWER-ON RESET STATE OF REGISTER CONTENTS.

Figure 5. Register Address Definition (Sheet 2 of 2)

Table 3. Hex Register Address/Description

WRITE (HEX)	READ (HEX)	DESCRIPTION	POR CONTENTS (HEX)	POR CONTENTS (BCD)
80	81	Seconds	00	00
82	83	Minutes	00	00
84	85	Hours	00	00
86	87	Date	01	01
88	89	Month	01	01
8A	8B	Day	01	01
8C	8D	Year	70	70
8E	8F	Control	00	00
90	91	Trickle charger	00	00
92	93	Century	19	19
94	95	Alarm configuration	00	00
—	97	Test configuration*	07	07
98	99	CX status	00	00
9A	9B	Configuration	00	00
9C	9D	Seconds alarm threshold	7F	7F
9E	9F	Minutes alarm threshold	7F	7F
A0	A1	Hours alarm threshold	BF	BF
A2	A3	Date alarm threshold	3F	3F
A4	A5	Month alarm threshold	1F	1F
A6	A7	Day alarm threshold	00	00
A8	A9	Year alarm threshold	FF	FF
BE	BF	Clock burst	N/A	N/A
C0	C1	RAM 0	Indeterminate	Indeterminate
C2	C3	RAM 1	Indeterminate	Indeterminate
C4	C5	RAM 2	Indeterminate	Indeterminate
C6	C7	RAM 3	Indeterminate	Indeterminate
C8	C9	RAM 4	Indeterminate	Indeterminate
CA	CB	RAM 5	Indeterminate	Indeterminate
CC	CD	RAM 6	Indeterminate	Indeterminate
CE	CF	RAM 7	Indeterminate	Indeterminate
D0	D1	RAM 8	Indeterminate	Indeterminate
D2	D3	RAM 9	Indeterminate	Indeterminate
D4	D5	RAM 10	Indeterminate	Indeterminate
D6	D7	RAM 11	Indeterminate	Indeterminate
D8	D9	RAM 12	Indeterminate	Indeterminate
DA	DB	RAM 13	Indeterminate	Indeterminate
DC	DD	RAM 14	Indeterminate	Indeterminate
DE	DF	RAM 15	Indeterminate	Indeterminate
E0	E1	RAM 16	Indeterminate	Indeterminate
E2	E3	RAM 17	Indeterminate	Indeterminate

**This is a read-only register.*

Table 3. Hex Register Address/Description (continued)

WRITE (HEX)	READ (HEX)	DESCRIPTION	POR CONTENTS (HEX)	POR CONTENTS (BCD)
E4	E5	RAM 18	Indeterminate	Indeterminate
E6	E7	RAM 19	Indeterminate	Indeterminate
E8	E9	RAM 20	Indeterminate	Indeterminate
EA	EB	RAM 21	Indeterminate	Indeterminate
EC	ED	RAM 22	Indeterminate	Indeterminate
EE	EF	RAM 23	Indeterminate	Indeterminate
F0	F1	RAM 24	Indeterminate	Indeterminate
F2	F3	RAM 25	Indeterminate	Indeterminate
F4	F5	RAM 26	Indeterminate	Indeterminate
F6	F7	RAM 27	Indeterminate	Indeterminate
F8	F9	RAM 28	Indeterminate	Indeterminate
FA	FB	RAM 29	Indeterminate	Indeterminate
FC	FD	RAM 30	Indeterminate	Indeterminate
FE	FF	RAM Burst	N/A	N/A

Diode and resistor selection is determined by the user, according to the maximum current desired for the battery or SuperCap charging. The maximum charging current can be calculated as shown in the following example. Assume that a system power supply of 3V is applied to V_{CC} and a SuperCap is connected to BATT. Also assume that the trickle charger has been enabled with no diode and resistor R1 between V_{CC} and BATT. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = \frac{3.0V}{R1} \approx \frac{3.0V}{1.7k\Omega} \approx 1.76mA$$

As the SuperCap charges, the voltage difference between V_{CC} and V_{BATT} decreases, and therefore the charge current decreases. The MAX6909 does not feature a trickle charger.

Power Control, Trickle Charger, and Battery Switchover

BATT provides power as a battery backup. V_{CC} provides the primary power in dual-supply systems where BATT is connected as a backup source to maintain the timekeeping function and RAM + register contents. When V_{CC} rises above the reset threshold, V_{RST}, V_{CC} powers the MAX6909/MAX6910. When V_{CC} falls below the reset threshold, VRST, and is less than V_{TPD}, BATT powers the MAX6909/MAX6910. If V_{CC} falls below the reset threshold, V_{RST}, and is more than V_{TPD}, V_{CC} powers the MAX6909/MAX6910. When RESET and $\overline{RESET}$ are active, all inputs ($\overline{MR}$, WDI, $\overline{CE\ IN}$, and the 2-wire interface) are disabled. In addition, when operating from BATT, the outputs RESET, $\overline{RESET}$, and $\overline{PFO}$ remain in the active state, PZT is high impedance and $\overline{CE\ OUT}$ is pulled to OUT. The timekeeping function remains active, together with the alarm function and crystal fail function if enabled. To minimize power consumption when operating from BATT, some functions are disabled; see Table 5. MAX6909/MAX6910 functional blocks remain active when powered from V_{CC} or BATT.

A battery can be connected prior to application of V_{CC} with no current being drawn from the battery and the MAX6909/MAX6910 remaining inactive. This is the freshness seal mode of operation. On the very first application of V_{CC} to the MAX6909/MAX6910, V_{CC} must rise above the reset threshold. The battery should only be changed with V_{CC} applied in order to maintain timekeeping functions.

The trickle charger can be enabled and disabled through software control but is automatically disabled whenever V_{CC} falls below V_{BATT}.

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Table 4. Trickle-Charger Register Control

D7	D6	D5	D4	D3	D2	D1	D0	ACTION
TCS	TCS	TCS	TCS	DS	DS	RS	RS	
X	X	X	X	0	0	X	X	Trickle charger disabled
X	X	X	X	1	1	X	X	Trickle charger disabled
X	X	X	X	X	X	0	0	Trickle charger disabled
1	0	1	0	1	0	1	0	No diode selected; 1.7K selected
1	0	1	0	1	0	0	1	No diode selected; 2.9K selected
1	0	1	0	1	0	1	1	No diode selected; 5K selected
1	0	1	0	0	1	1	0	Two diodes selected; 1.7K selected
1	0	1	0	0	1	0	1	Two diodes selected; 2.9K selected
1	0	1	0	0	1	1	1	Two diodes selected; 5K selected

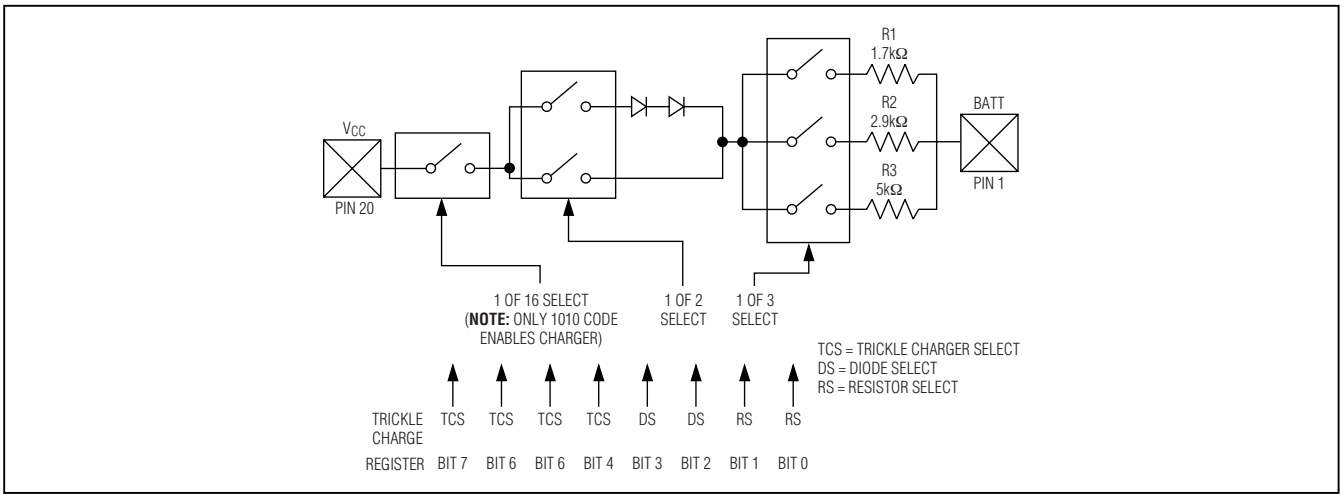

Figure 6. Trickle-Charger Functional Schematic

OUT Function

OUT is an output supply voltage for external devices. When V_{CC} rises above the reset threshold or is greater than V_{BATT}, OUT connects to V_{CC}. When V_{CC} falls below V_{RST} and V_{BATT}, OUT connects to BATT. There is a typical V_{TRU} - V_{TRD} hysteresis associated with the switching between V_{CC} and BATT if BATT < V_{RST} and typically V_{HYST} of hysteresis if BATT > V_{RST}. Connect at least a 0.1µF capacitor from OUT to ground (GND). Switching from V_{CC} to BATT uses a break-before-make switch; a capacitor from OUT to GND prevents loss of power needed for clock data and RAM during switchover.

Oscillator Start Time

The MAX6909/MAX6910 oscillator typically takes 100ms to settle to its optimum operating power level after start-up. To ensure the oscillator is operating, the system software should validate this by reading the seconds register. Any reading with more than 0s, from the POR value of 0s, is a validation that the oscillator is operating.

Power-On Reset (POR)

The MAX6909/MAX6910 contain an integral POR circuit that ensures all registers are reset to a known state on power-up. On initial power-up, once V_{OUT} rises above 0.75V (typ), the POR circuit releases the registers for normal operation. Should V_{OUT} dip to less than 1.5V (typ), the contents of the MAX6909/MAX6910 registers can no longer be guaranteed.

Table 5. MAX6910 I/O and IC Sections Powered from V_{CC} and BATT

DESCRIPTION	PIN	PIN NAME	POWER = V_{CC}	V_{CC} < V_{RST}	V_{CC} < V_{RST} COMMENTS	COMMENTS
Crystal Oscillator I/O	9	X1	Enabled	Enabled		
Crystal Oscillator I/O	10	X2	Enabled	Enabled		
Backup Power-Supply Input	1	BATT	N/A	N/A		Power pin
OUT (> of V_{CC} or BATT if V_{CC} < V_{RESET})	2	OUT	N/A	N/A		Power output pin
Manual Reset Input	6	$\overline{MR}$	Enabled	Disabled	Input ignored	
Battery-On Output	3	$\overline{BATT\ ON}$	Enabled	Enabled		
Watchdog Input	7	WDI	Enabled	Disabled	Input ignored	
Chip-Enable Input	4	$\overline{CE\ IN}$	Enabled	Disabled	Input ignored	
Power-Fail Input	5	PFI	Enabled	Disabled	Input ignored	
Ground	8	GND	N/A	N/A		Power pin
Active Low, Open-Drain Reset Output (-OD)	18	$\overline{RESET}$	Enabled	Enabled	Pulled low	
Active High, Push/Pull Reset Output	19	RESET	Enabled	Enabled	Pulled to V_{CC}	
Chip-Enable Output	17	$\overline{CE\ OUT}$	Enabled	Disabled	Pulled to OUT	
Power-Fail Output	16	$\overline{PFO}$	Enabled	Enabled	Pulled low	
Alarm Output	14	$\overline{ALM}$	Enabled	Enabled		
Piezo Output	15	PZT	Enabled	Disabled	High impedance	
Crystal-Fail Output	11	$\overline{CX\ FAIL}$	Enabled	Enabled		
2-Wire Bus Data I/O	12	SDA	Enabled	Disabled		
2-Wire Bus Clock	13	SCL	Enabled	Disabled		
Main Power-Supply Input	20	V_{CC}	N/A	N/A		Power pin
Trickle Charge	1 to 20		Enabled	Disabled		
FEATURES						
Crystal Oscillator			Enabled	Enabled		Supply = OUT
RAM			Enabled	Enabled		Supply = OUT
Timekeeping Registers			Enabled	Enabled		Supply = OUT
Control Registers			Enabled	Enabled		Supply = OUT
Crystal Fail Detect			Enabled	Enabled		Supply = OUT
Alarm Registers			Enabled	Enabled		Supply = OUT
Power-Fail Comparator			Enabled	Enabled	Disabled in BATT	Supply = OUT
RESET Comparator			Enabled	Enabled		Supply = V_{CC}
Watchdog Timer			Enabled	Disabled		Supply = OUT
Internal Reference			Enabled	Enabled		Supply = V_{CC}
Power Switchover			Enabled	Enabled		Supply = V_{CC}
CE Circuitry			Enabled	Disabled		Supply = OUT
Piezo Dividers/Select Register			Enabled	Enabled		Supply = OUT
Trickle Charge			Enabled	Disabled		Supply = OUT

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Alarm Generation Registers

The alarm function generates an ALARM when the contents of the SEC, MIN, HR, DATE, MONTH, DAY, or YEAR registers match the respective alarm threshold registers. Also, the generation of the ALARM is programmable through the alarm configuration register. The alarm configuration register can be written to with an address of 94H or it can be read with an address of 95H. The alarm configuration register definition is shown in Figure 5 (register address definition). Placing a 1 in the appropriate bit enables the $\overline{ALM}$ and the alarm out status bit when the selected alarm threshold register contents match the respective timekeeping register contents. For example, writing 0000 0001 to the alarm configuration register causes the alarm pin to get triggered every minute (each time the contents of the seconds timekeeping register match the contents of the seconds alarm threshold register). Writing 0000 0010 causes the alarm to go on every hour (each time the contents of the minutes timekeeping register match the contents of the minutes alarm threshold register). Writing a 0100 1111 to the alarm configuration register, therefore, causes the alarm to be triggered on a specific second, of a specific minute, of a specific hour, of a specific date, of a specific year. The alarm output stays low until it is "cleared" by reading or writing to the alarm configuration register or by reading or writing to any of the alarm threshold registers.

Minutes Register (Alarm Out Status)

An alarm out status bit is available if it is desired to use the alarm function as a polled alarm instead of connecting directly to the $\overline{ALM}$ output pin. Bit D7 in the minutes timekeeping register contains the status of the $\overline{ALM}$ output with a 1 indicating the alarm function has triggered and zero indicating no triggered alarm.

Manual Reset Input

Many microprocessor-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. With the MAX6909/MAX6910, a logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{RP} (Figure 7) after it returns high. $\overline{MR}$ has an internal pullup resistor of typically 50kΩ, so it can be left open if it is not used. Internal debounce circuitry requires a minimum low time on the $\overline{MR}$ input of 1µs with 100ns (typ) minimum glitch immunity.

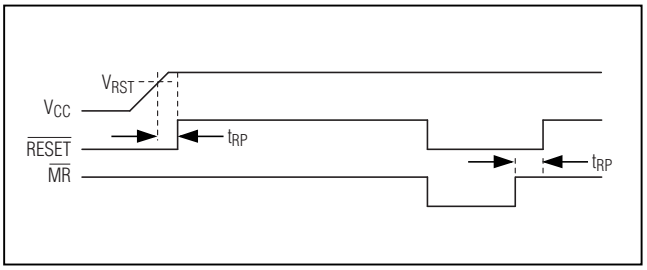

Figure 7. Manual Reset Timing

Reset Outputs

A µP's reset input starts the µP in a known state. When RESET and $\overline{RESET}$ are active, all control inputs ($\overline{MR}$, WDI, $\overline{CE\ IN}$, and the 2-wire interface) are disabled. The MAX6909/MAX6910 µP supervisory circuit asserts a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. $\overline{RESET}$, open-drain active low, and RESET (push-pull active high) are guaranteed to be active for $0V < V_{CC} < V_{RST}$, provided V_{OUT} is greater than 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps RESET and $\overline{RESET}$ active for the reset timeout period (t_{RP}); after this interval, $\overline{RESET}$ becomes inactive (high) and RESET becomes inactive (low). If a brownout condition occurs (V_{CC} dips below the reset threshold), RESET and $\overline{RESET}$ become active. Each time RESET and $\overline{RESET}$ are asserted, they are held active for the reset timeout period.

The MAX69_ _EO30 is optimized to monitor 3.0V ±10% power supplies. Except when $\overline{MR}$ is asserted, reset does not occur until V_{CC} falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the power supply falls below +2.5V.

The MAX69_ _EO33 is optimized to monitor 3.3V ±10% power supplies. Except when $\overline{MR}$ is asserted, reset does not occur until V_{CC} falls below 3.0V (3.0V is just above 3.3V - 10%), but is guaranteed to occur before the power supply falls below 2.8V.

See the Maximum Transient Duration vs. Reset Comparator Overdrive graph in the *Typical Operating Characteristics.*

Negative-Going V_{CC} Transients

The MAX6909/MAX6910 are relatively immune to short-duration negative transients (glitches) while issuing resets to the µP during power-up, power-down, and brownout conditions. Therefore, resetting the µP when V_{CC} experiences only small glitches is usually not recommended.

Maximum transient duration vs. reset comparator overdrive (see the *Typical Operating Characteristics*) shows the maximum pulse period that can occur on V_{CC} for which reset pulses are NOT generated. The graph was produced using negative-going V_{CC} pulses, starting at 3.6V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the typical maximum pulse width a negative-going V_{CC} transient can have without causing a reset. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 60mV below the reset threshold and lasts for 60µs or less does not cause a reset pulse to be issued. A capacitor of at least 0.1µF mounted close to the V_{CC} pin provides additional transient immunity.

Interfacing to Microprocessors with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX6909/MAX6910 $\overline{\text{RESET}}$ or RESET outputs. If, for example, the RESET output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the RESET output and the µP reset I/O as shown in Figure 8. Buffer the RESET output to other system components. The positive voltage supply for the RESET pin is V_{CC}. If V_{CC} drops, then so does the V_{OH} of this pin.

Battery-On Output

The battery-on output, $\overline{\text{BATT ON}}$, is an open-drain output indicator of when the MAX6909/MAX6910 are powered from the backup battery input, BATT. When V_{CC} falls below the reset threshold, V_{RST}, and below V_{BATT}, OUT switches from V_{CC} to BATT and $\overline{\text{BATT ON}}$ is asserted. When V_{CC} rises above V_{BATT} or the reset threshold, V_{RST}, OUT reconnects to V_{CC} and $\overline{\text{BATT ON}}$ is deasserted.

Watchdog Input

In the MAX6909/MAX6910, the watchdog circuit monitors the µP's activity. Data bit D4 in the configuration register controls the selection of the watchdog timeout period. The power-up default is 1.6s (D4 = 0). If D4 is set to 1, then the watchdog timeout period is changed to 200ms. Data bit D7 in the configuration register is the watchdog enable function. A logic 0 disables the watchdog function and a logic 1 enables the watchdog function. The power-on reset state of WD EN is logic 0, meaning the watchdog function is disabled. When D4 is set to 1, the first watchdog timeout period following a reset cycle is always 1.6s and reverts to 200ms after the first WDI transition. This is to allow the µP to recover after a RESET interrupt. If the µP does not toggle the WDI within the register-selectable watchdog timeout period, RESET and $\overline{\text{RESET}}$ are asserted for 200ms. At the same time, bits D4 and D7 in the configuration register are reset. These bits have to be rewritten to enable the watchdog and short timeout function again. While RESET and $\overline{\text{RESET}}$ are asserted, all control inputs to the MAX6909/MAX6910 are disabled ($\overline{\text{MR}}$, $\overline{\text{CE IN}}$, WDI, and the 2-wire interface). Figure 9 shows the watchdog timing relationship.

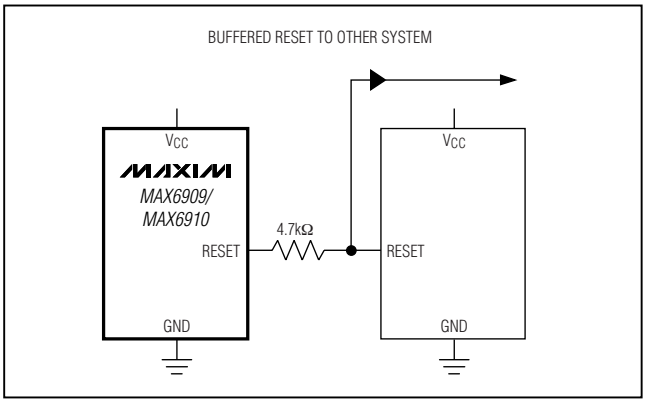

Figure 8. Interfacing to Microprocessors with Bidirectional Reset I/O

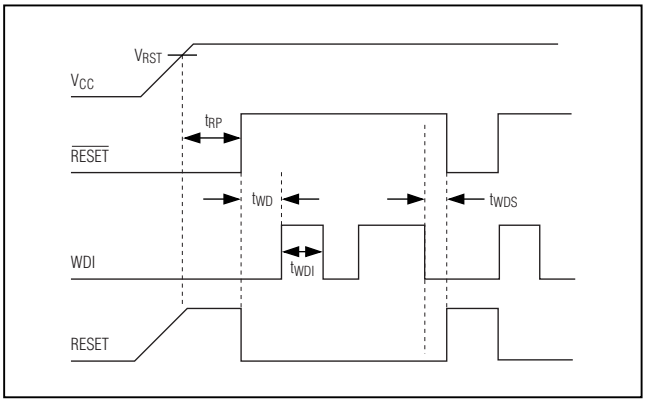

Figure 9. Watchdog Timing Relationship

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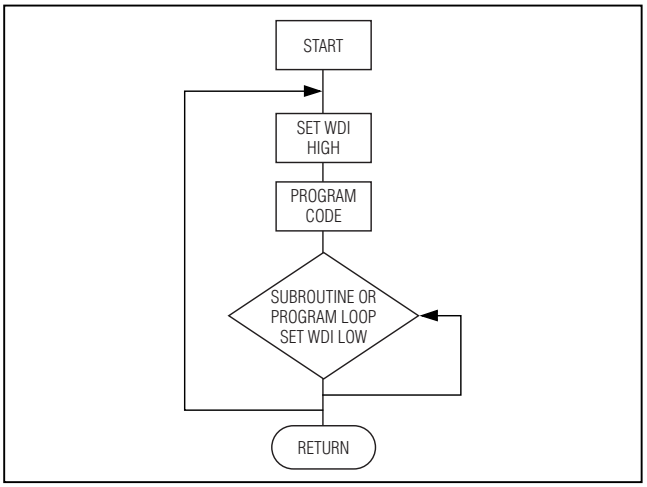

Figure 10. Watchdog Flow Diagram

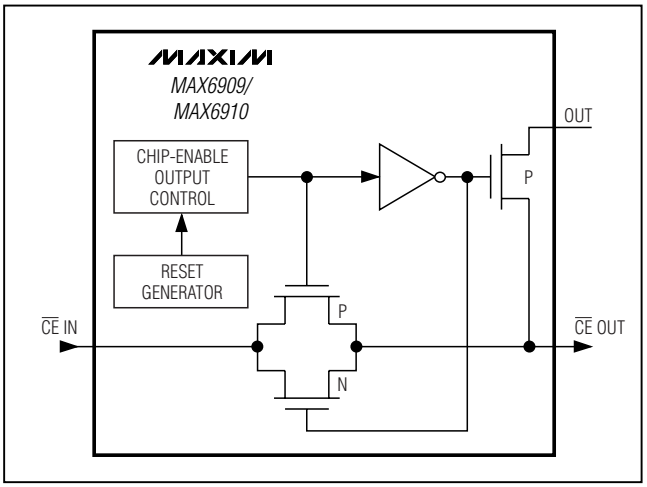

Figure 11. Chip-Enable Transmission Gate

Watchdog Software Considerations

There is a way to help the watchdog-timer monitor software execution more closely, which involves setting and resetting the watchdog input at different points in the program rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop, in which the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 10 shows an example of how the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would quickly be corrected since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset to be issued.

Chip-Enable Signal Gating

Internal gating of chip-enable (CE) signals prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX6909/MAX6910 use a transmission gate from $\overline{CE\ IN}$ to $\overline{CE\ OUT}$. During normal operation (reset not asserted), the transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{CE\ IN}$ to $\overline{CE\ OUT}$ enables the MAX6909/MAX6910 to be used with most microprocessors. If $\overline{CE\ IN}$ is low when reset asserts, $\overline{CE\ OUT}$ remains low for typically t_{RCE} to permit completion of the current write cycle. Figure 11 shows the chip-enable transmission gate.

Chip-Enable Input

The CE transmission gate is disabled and $\overline{CE\ IN}$ is high impedance (disabled mode) while reset is asserted. During a power-down sequence when V_{CC} goes below the reset threshold, the CE transmission gate disables, and $\overline{CE\ IN}$ immediately becomes high impedance if the voltage at $\overline{CE\ IN}$ is a logic high. If $\overline{CE\ IN}$ is logic low when reset asserts, the CE transmission gate disables at the moment $\overline{CE\ IN}$ goes high or t_{RCE} after reset asserts (t_{RCE}), whichever occurs first (Figure 12). This permits the current write cycle to complete during power-down. The CE transmission gate remains disabled and $\overline{CE\ IN}$ remains high impedance (regardless of $\overline{CE\ IN}$ activity) for (t_{RP}), the reset timeout period any time a reset is generated. While disabled, $\overline{CE\ IN}$ is high impedance. When the CE transmission gate is enabled, the impedance of $\overline{CE\ IN}$ appears as a load in series with the load at $\overline{CE\ OUT}$.

The propagation delay through the CE transmission gate depends on V_{CC}, the source impedance of the driver connected to $\overline{CE\ IN}$, and the loading on $\overline{CE\ OUT}$. The CE propagation delay is measured from the 50% point on $\overline{CE\ IN}$ to the 50% point on $\overline{CE\ OUT}$ using a 50Ω driver and 10pF of load capacitance (Figure 14), and is typically 5ns. For minimum propagation delay, minimize the capacitive load at $\overline{CE\ OUT}$, and use a low-output-impedance driver.

Chip-Enable Output

When the CE transmission gate is enabled, the impedance of $\overline{CE\ OUT}$ is equivalent to a resistor in series with the source driving $\overline{CE\ IN}$. In the disabled mode, the transmission gate is off and an active pullup connects $\overline{CE\ OUT}$ to OUT (Figure 12). This pullup turns off when the transmission gate is enabled.

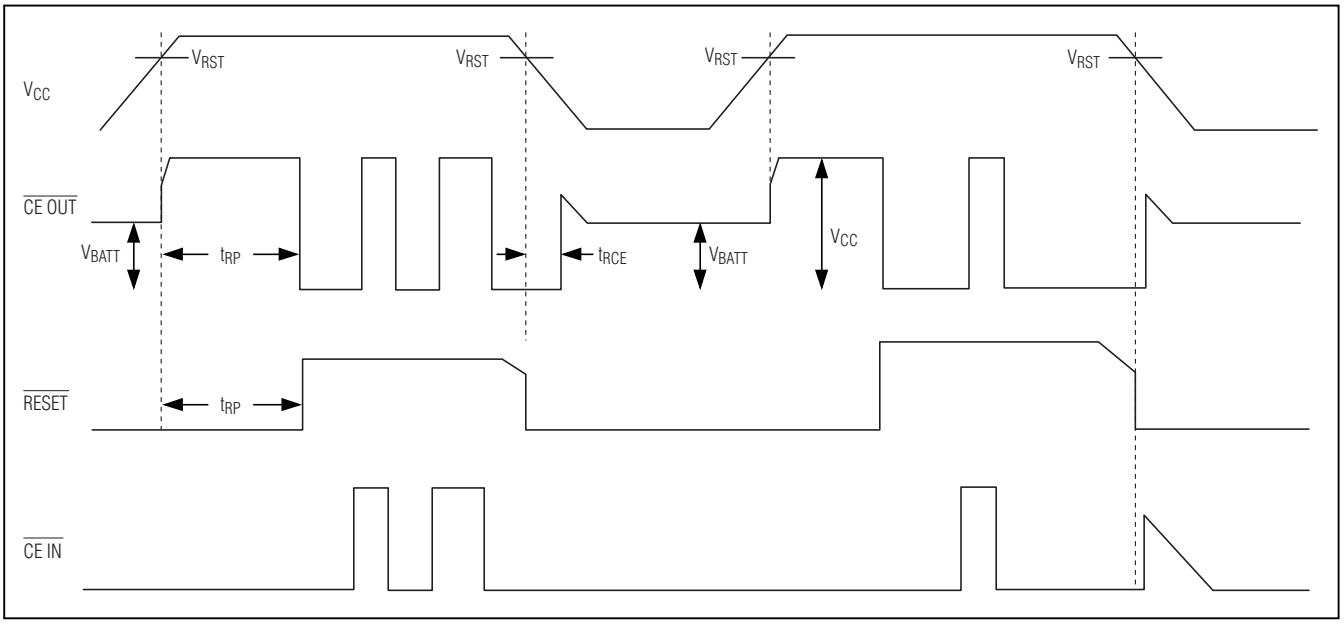

Figure 12. Chip-Enable Timing

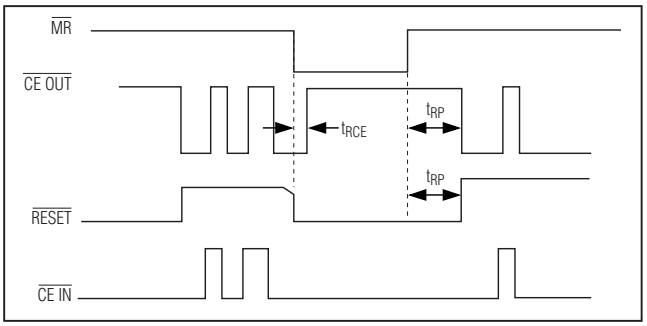

Figure 13. Chip-Enable Timing Including MR

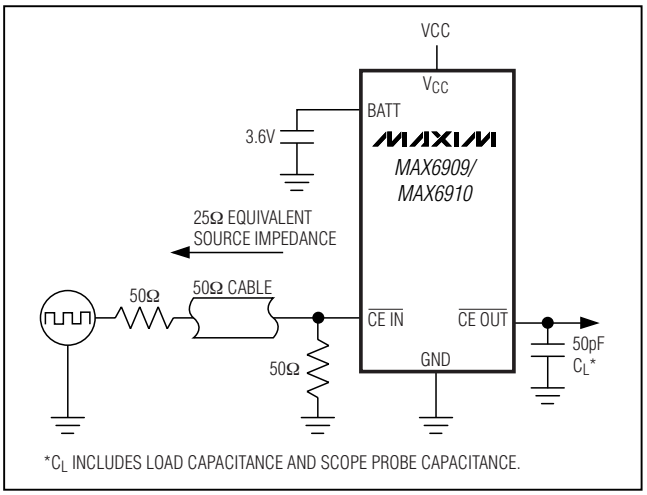

Figure 14. CE Propagation-Delay Test Circuit

Power-Fail Comparator

The MAX6909/MAX6910 PFI is compared to an internal reference. If the PFI voltage is less than the power-fail threshold (V_{PFT}), $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply and can monitor either positive or negative supplies using a voltage-divider to PFI (Figure 26). However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

Any time $V_{CC} < V_{RST}$, $\overline{PFO}$ is forced low, regardless of the state of PFI. Any time $V_{CC} > V_{RST}$ and $\overline{RESET}$ is active low (during the reset timeout period), $\overline{PFO}$ is forced high, regardless of the state of PFI. If the comparator is unused, connect PFI to V_{CC} and leave $\overline{PFO}$ floating. Figure 15 shows PFI and $\overline{PFO}$ timing.

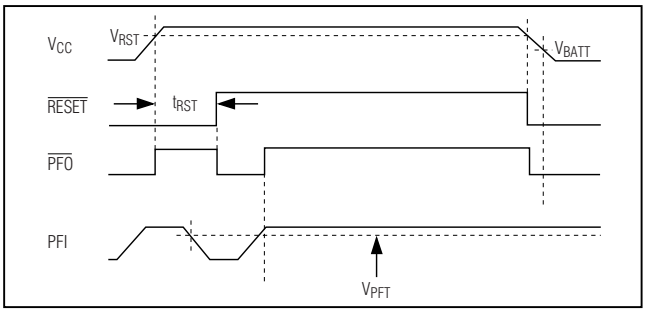

Figure 15. PFI and PFO Timing

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Piezo Transducer Output Drive

The push-pull, piezo transducer drive output, PZT, is selectable through the configuration register for frequencies of 1.024kHz, 2.048kHz, 4.096kHz, or 8.192kHz (Table 6). Bits D0 and D1 control which frequency outputs to PZT. If in battery backup mode (when V_{CC} falls below the reset threshold and below V_{BATT}), the PZT output is disabled to high impedance to prevent battery drain from the backup battery on the BATT pin.

Table 7 lists the piezo transducer control bits.

Bit D3, the PZT SEL bit, selects whether the $\overline{ALM}$, alarm output, controls when the selected PZT frequency is gated to PZT or whether control is given to the PZT CNTL bit, bit D2. If D3 = 1, then the $\overline{ALM}$ controls gating of the selected PZT frequency to PZT. When the alarm is triggered, the selected frequency stays on PZT until the alarm is cleared by writing to or reading from the alarm configuration register. If D3 = 0, then the PZT CNTL bit, D2, determines when and for how long the selected frequency appears at PZT. Bit D2, the PZT CNTL bit, controls whether the selected frequency is gated to PZT, provided D3 = 0. D2 = 1 gates the selected frequency to PZT and D2 = 0 inhibits the selected frequency (PZT remains low).

Anytime a frequency is selected to be gated through to the PZT output, it is modulated by a 1Hz square wave. The PZT output then turns on for 0.5s and off for 0.5s. Since the human ear is particularly sensitive to changes in condition, switching a sound on and off makes it more noticeable than a continuous sound of the same frequency.

The PZT output swings between V_{CC} and GND through the output stage's on-resistance, R_{OUT_PZT}. To allow flexibility of the PZT output to work with many different types of piezo buzzers, R_{OUT_PZT} is designed to be as low as practical. To minimize peak currents into the piezo buzzer, an external current-limiting resistor Rs may be required. Ipeak is now equal to V_{CC} / (Rs + R_{OUT_PZT}). Rs can be adjusted to reduce the sound amplitude from the external piezo buzzer. The value of Rs varies for each application and should be chosen at the prototype design stage with the piezo buzzer installed in a cavity approximating its final housing. The typical value of R_{OUT_PZT} is calculated from V_{OUT} / I_{PZT}, where I_{PZT} is the average of the sink and source currents. Figure 16 is the piezo transducer functional diagram.

Table 6. Piezo Transducer Selectable Frequencies

D1 (PZT FREQ)	D0 (PZT FREQ)	PZT TYPICAL FREQUENCY (kHz)
0	0	1.024
0	1	2.048
1	0	4.096
1	1	8.19

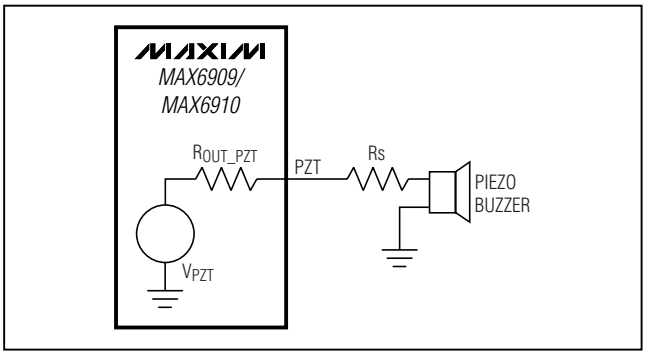

Figure 16. Piezo Transducer Functional Diagram

Table 7. Piezo Transducer Control Bits

D3 (PZT SEL)	D2 (PZT CNTL)	CONDITION	PZT
0	0	PZT CNTL bit, D2, has control	Low
0	1	PZT CNTL bit, D2, has control	Selected frequency
1	0	$\overline{ALM}$ has control, D2 is ignored; assume alarm triggered	Selected frequency
1	1	$\overline{ALM}$ has control, D2 is ignored; assume alarm cleared by reading the alarm configuration register	Low

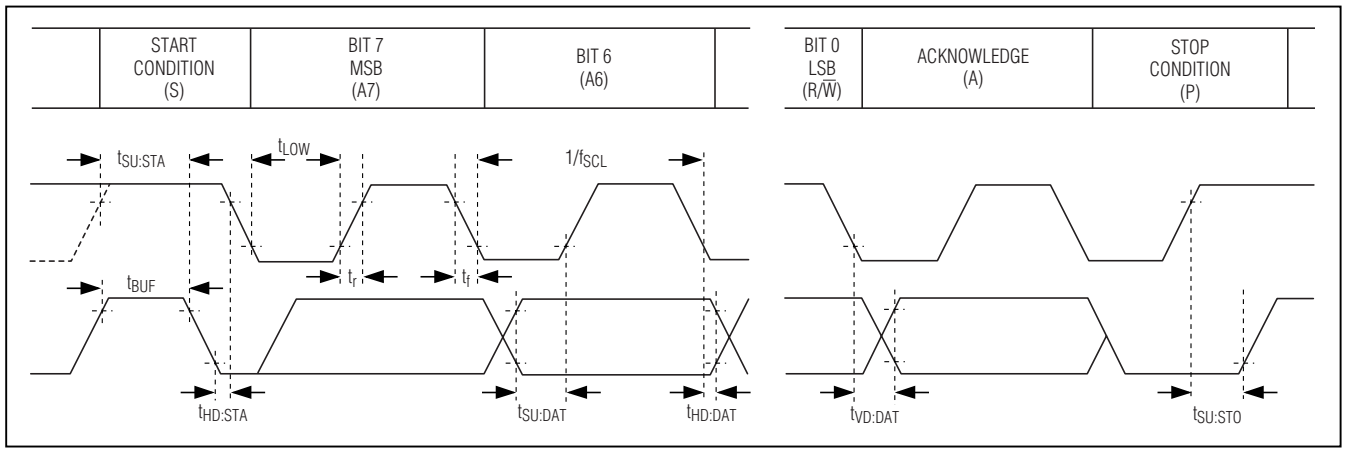

Figure 17. 2-Wire Bus Timing Diagram

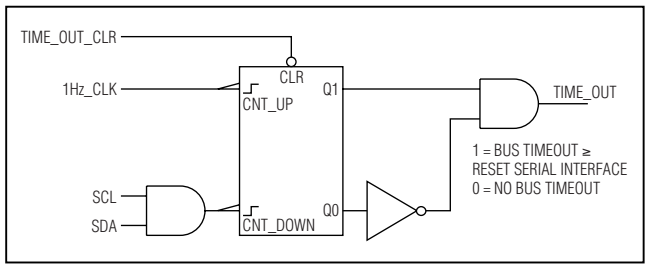

Figure 18. Timeout Simplified Functional Diagram

Crystal-Fail Output

The open-drain, crystal-fail output, $\overline{\text{CX FAIL}}$, alerts the user when the 32.768kHz crystal has failed due to a loss of 30 contiguous cycles, typical, of the 32.768kHz clock. If $\overline{\text{CX FAIL}}$ enable (D7) in the alarm configuration register is set to 1, then the crystal-fail detect circuit is enabled; if D7 = 0, the crystal-fail detect circuit is disabled.

When $\overline{\text{CX FAIL}}$, D7 in the CX status register is 1, a crystal failure has been detected and $\overline{\text{CX FAIL}}$, open-drain output, goes low. The $\overline{\text{CX FAIL}}$ output and the $\overline{\text{CX FAIL}}$ bit in the CX status register are both cleared by reading to the CX status register.

Test Configuration Register

This is a read-only register.

2-Wire Interface

The MAX6909/MAX6910 use a bidirectional 2-wire serial interface. The two lines are SDA and SCL. Both lines must be connected to a positive supply through individual pullup resistors. Data transfers can only be initiated when the bus is not busy (both SDA and SCL are high). When V_{CC} is less than V_{RST}, communication with the serial bus is terminated and inactive to prevent erroneous communication from the microprocessor. Figure 17 is the 2-wire bus timing diagram.

Timeout Feature

The purpose of the bus timeout is to reset the serial bus interface and change the SDA line from an output to an input, which releases the SDA line from being held low. This is necessary when the MAX6909/MAX6910 are transmitting data and become stuck at logic low. If the SDA line is stuck low, any other device on the bus is not able to communicate. The logic above, shown in Figure 18, is intended to illustrate the timeout feature. If an I²C transaction takes more than 1s (minimum timout period), a timeout condition occurs. When a timeout condition is observed, the I²C interface resets to the IDLE state and waits for a new I²C transaction. In order to complete the 31-byte burst read/write from the RAM before an I²C timeout, the minimum SCL frequency must be 0.32kHz. A valid start condition sets Time_Out_CLR = 1 and the counting begins. A valid stop condition returns Time_Out_CLR = 0 and disables the up/down counter.

Figure 19 shows the normal 2-wire bus operation.

Figure 20 illustrates what happens when the SDA line is stuck low for two clock cycles of 1Hz_CLK during a valid bus transaction. Depending on when the actual valid bus transaction begins relative to the 1Hz CLK, the timeout period is either t1 = 2s or t2 = 1s.

Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as control signals (Figure 21).

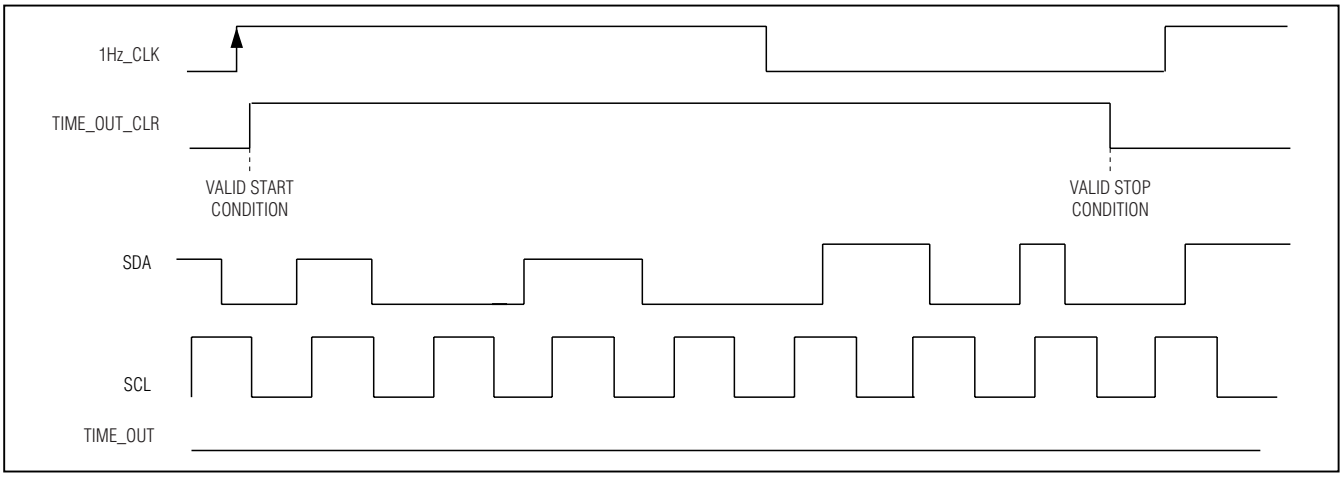

Figure 19. Normal 2-Wire Bus Operation

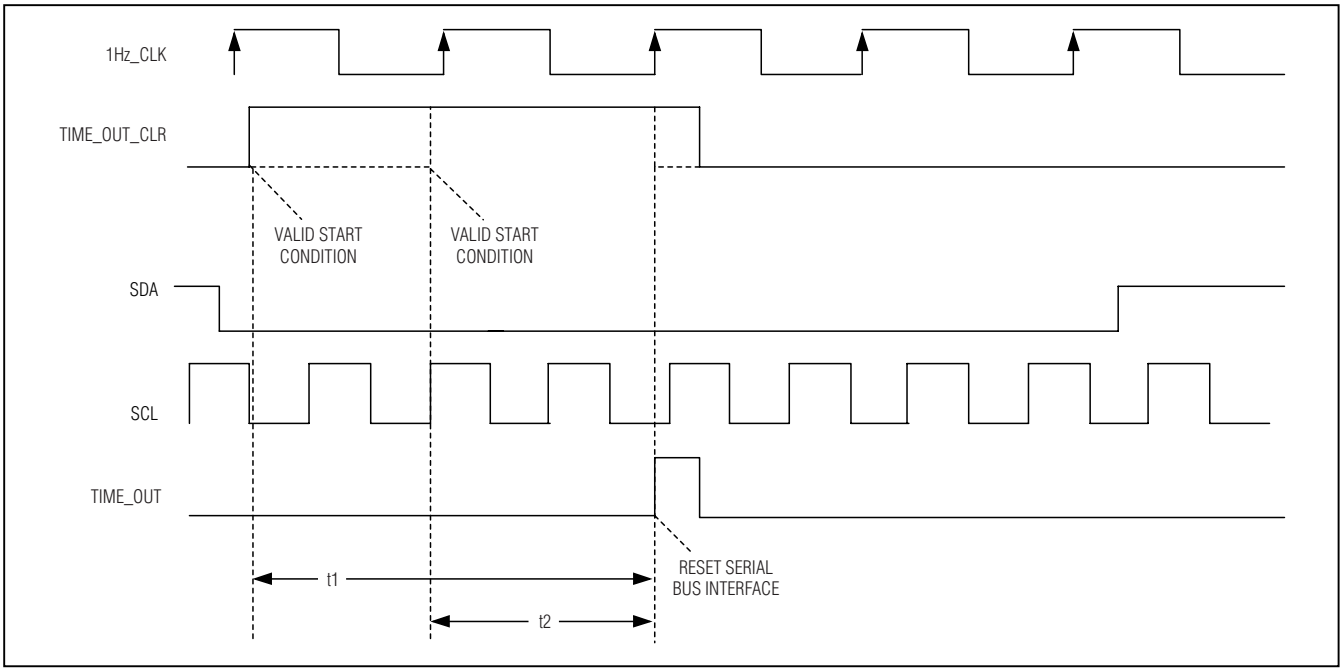

Figure 20. Timeout 2-Wire Bus Operation

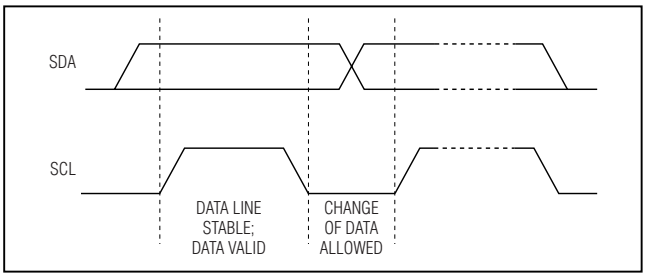

Figure 21. Bit Transfer

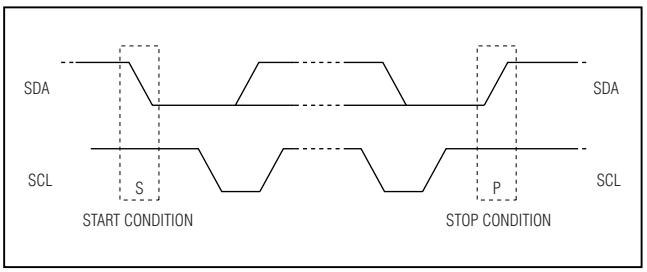

Figure 22. START and STOP Conditions

START and STOP Conditions

Both SDA and SCL remain high when the bus is not busy. A high-to-low transition of SDA, while SCL is high, is defined as the START (S) condition. A low-to-high transition of the data line while SCL is high is defined as the STOP (P) condition (Figure 22).

Acknowledge

The number of data bytes between the START and STOP conditions for the transmitter and receiver are unlimited. Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on SDA by the transmitter, during which time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge clock pulse (setup and hold times must also be met). A master receiver must signal an end of the data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a STOP condition.

Slave Address Byte

Before any data is transmitted on the bus, the device that should respond is addressed first. The first byte sent after the start (S) procedure is the address byte. The MAX6909/MAX6910 act as a slave transmitter/receiver. Therefore, SCL is only an input clock signal and SDA is a bidirectional data line. The slave address for the MAX6909/MAX6910 is shown in Figure 23.

1	1	0	1	0	0	0	RD/W
BIT 7							BIT 0

Figure 23. MAX6909/MAX6910 2-Wire Slave Address Byte

7	6	5	4	3	2	1	0
1	RAM /CLK	A5	A4	A3	A2	A1	RD /W

Figure 24. Address/Command Byte

Address/Command Byte

The command byte is shown in Figure 24. The MSB (bit 7) must be a logic 1. If it is zero, writes to the MAX6909/MAX6910 are disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 through 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or a read operation (output) if logic 1. The command byte is always input starting with the MSB (bit 7).

Reading from the Timekeeping Registers

The timekeeping registers (seconds, minutes, hours, date, month, day, and year) can be read either with a single read or a burst read. The century register can only be read with a single read. Since the real-time clock runs continuously and a read takes a finite amount of time, there is the possibility that the clock counters could change during a read operation, thereby reporting inaccurate timekeeping data. In the MAX6909/MAX6910, each clock register's data is buffered by a latch. Clock register data is latched by the 2-wire bus read command (on the falling edge of SCL when the slave acknowledge bit is sent after the address/command byte has been sent by the master to read a timekeeping register). Collision-detection circuitry ensures that this does not happen coincident with a seconds counter update to ensure accurate time data is being read. This avoids time data changes during a read operation. The clock counters continue to count and keep accurate time during the read operation.

If single reads are to be used to read each of the timekeeping registers individually, then it is necessary to do some error checking on the receiving end. The potential for error is the case when the seconds counter increments before all the other registers are read out. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during single read operations of the timekeeping registers. Then, the net data could become 14:59:59, which is erroneous real-time data. To prevent this with single-read operations, read the seconds register first (initial seconds) and store this value for future comparison. When the remaining timekeeping registers have been read out, read the seconds register again (final seconds). If the initial seconds value is 59, check that the final seconds value is still 59; if not, repeat the entire single-read process for the timekeeping registers. A comparison of the initial seconds value with the final seconds value can indicate if there was a bus delay problem in reading the timekeeping data (difference should always be 1s or less). Using a 100kHz bus speed, sequential single reads would take under 2.5ms to read all seven of the timekeeping registers, plus a second read of the seconds register.

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The most accurate way to read the timekeeping registers is to do a burst read. In the burst read, the main timekeeping registers (seconds, minutes, hours, date, month, day, year) and the control register are read sequentially, in the order listed with the seconds register first. They must be all read out as a group of eight registers, with 8 bits each, for proper execution of the burst read function. All seven timekeeping registers are latched upon the receipt of the burst read command. Worst-case errors that can occur between the actual time and the read time is 1s, assuming the entire burst read is done in less than 1s.

Writing to the Timekeeping Registers

The time and date can be set by writing to the timekeeping registers (seconds, minutes, hours, date, month, day, year, and century). To avoid changing the current time by an incomplete write operation, the current time value is buffered from being written directly to the timekeeping registers. The timekeeping registers continue to count, and on the next rising edge of the 1Hz seconds clock, the new data is loaded into the timekeeping registers. The new value will be incremented on the next rising of the 1Hz seconds clock. Collision-detection circuitry ensures that this does not happen coincident with a seconds register update to ensure accurate time data is being written. This avoids time data changes during a write operation. An incomplete write operation aborts the time update procedure and the contents of the input buffer are discarded.

If single write operations are to be used to write to each of the timekeeping registers, then error checking is needed. If the seconds register is to be updated, update it first and then read it back and store its value as the initial seconds. Update the remaining timekeeping registers and then read the seconds register again (final seconds). If initial seconds were 59, ensure they are still 59. If initial seconds were not 59, ensure that final seconds are within 1s of initial seconds. If the seconds register is not to be written to, then read the seconds register first and save it as initial seconds. Write to the required timekeeping registers and then read the seconds register again (final seconds). If initial seconds were 59, ensure they are still 59. If initial seconds were not 59, ensure that final seconds are within 1s of initial seconds.

Although both single writes and burst writes are possible, the most accurate way to write to the timekeeping registers is to do a burst write. In the burst write, the main timekeeping registers (seconds, minutes, hours, date, month, day, year) and the control register are written to sequentially. They must be all written to as a group of eight registers, with 8 bytes each, for proper execution of the burst write function. All seven timekeeping registers are simultaneously loaded into the input buffer at the end of the 2-wire bus write operation. The worst-case error that can occur between the actual time and the write time update is 1s. Figure 25 shows MAX6909/MAX6910 data transfer.

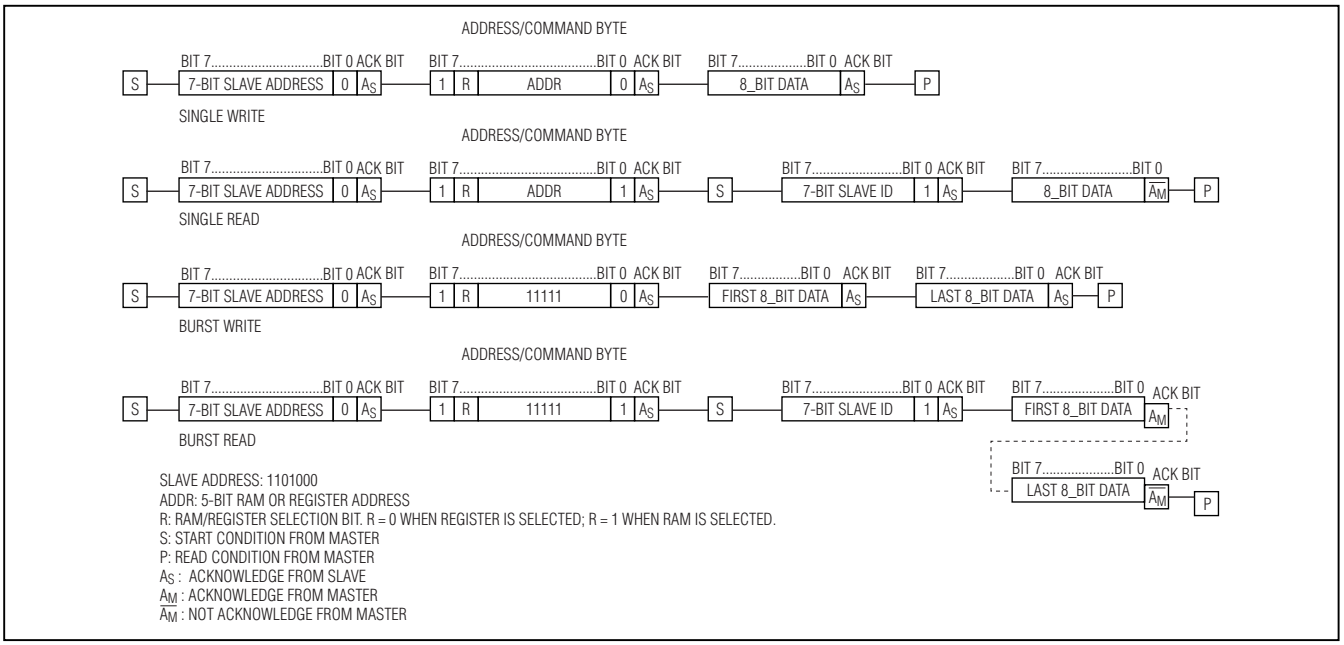

Figure 25. MAX6909/MAX6910 Data Transfer

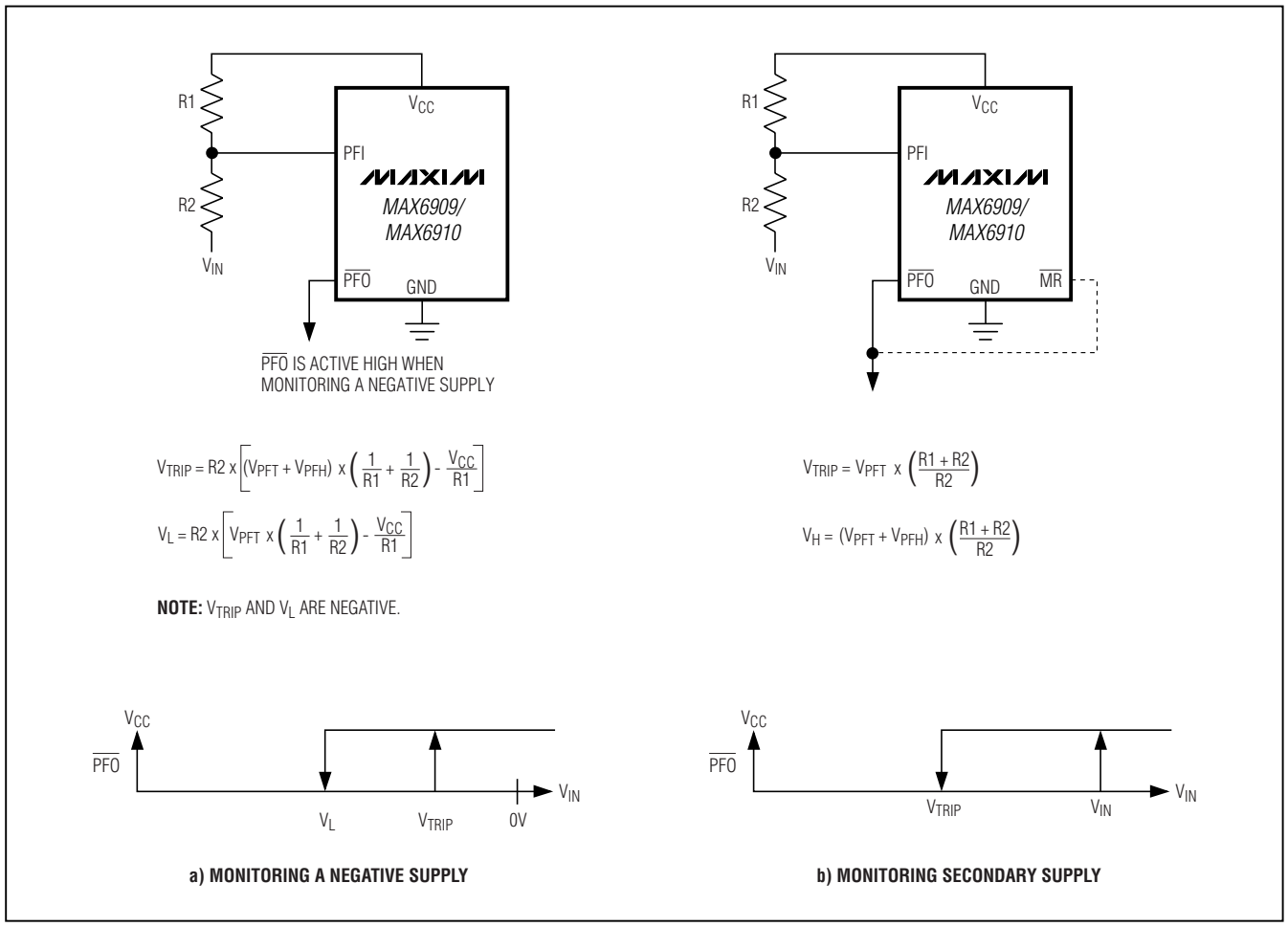

Figure 26. Using the Power-Fail Comparator to Monitor Additional Power Supplies

Applications Information

Monitoring Additional Power Supplies

PFO can be connected to MR so that a low voltage on PFI activates RESET and RESET (Figure 26). In this configuration, when the monitored voltage causes PFI to fall below V_{PFT}, PFO pulls MR low, causing a reset to be asserted. A 200ms reset is generated, during which PFO is forced high and MR is released. At the end of the 200ms reset, the power-fail comparator reflects the state of PFI, which if below V_{PFT}, causes another reset.

Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 30mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage-divider supply (Figure 27).

If additional noise margin is desired, connect a resistor between PFO and PFI (Figure 27(a)). Select the ratio of R1 and R2 such that PFI sees V_{PFT} when V_{IN} falls to its trip point (V_{TRIP}). R3 adds the additional hysteresis and should typically be more than 10 times the value of R1 or R2. The hysteresis window extends both above (V_H) and below (V_L) the original trip point (V_{TRIP}).

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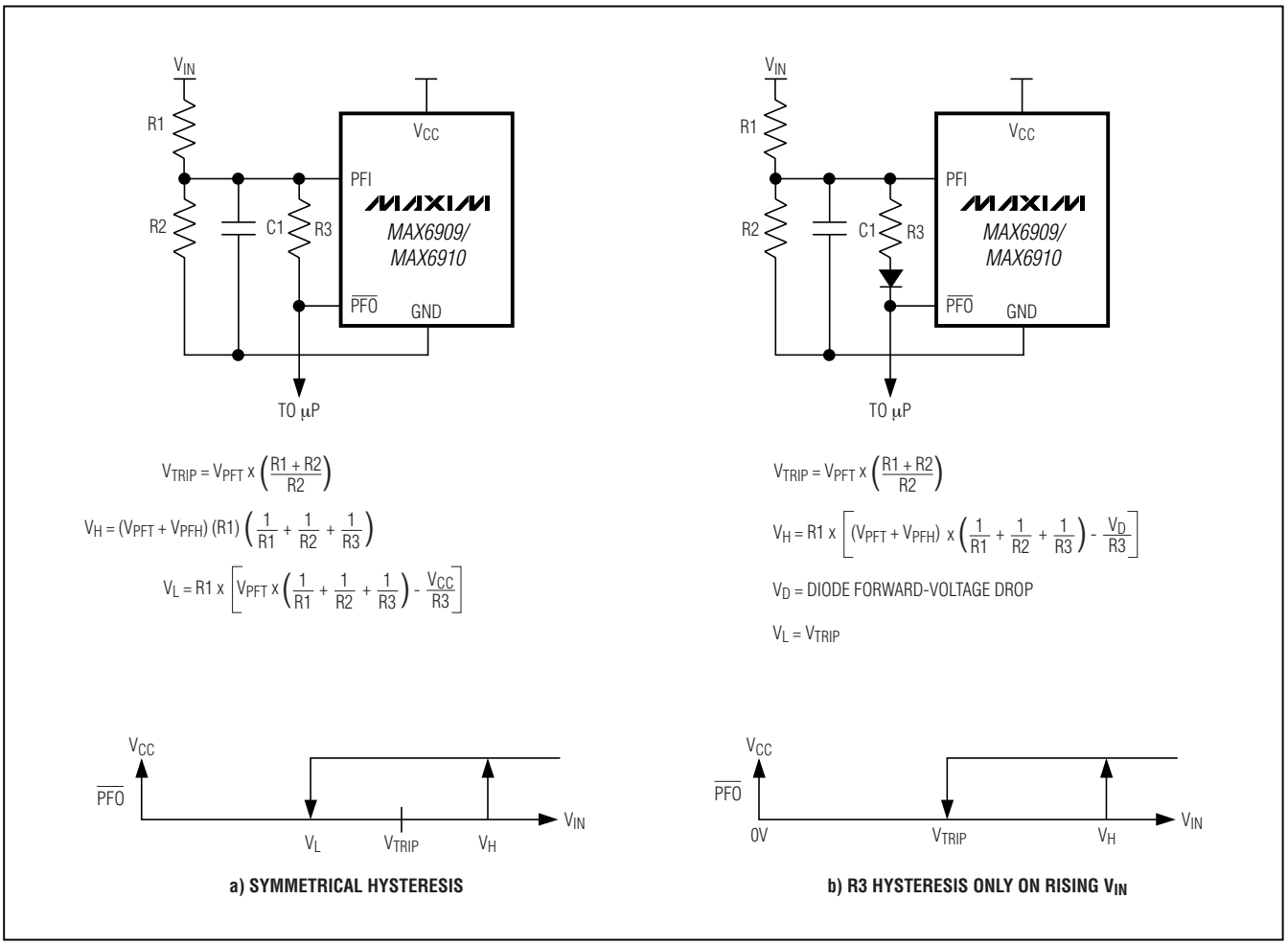


Figure 27. Adding Hysteresis to the Power-Fail Comparator

Connecting an ordinary signal diode in series with R3 (Figure 27(b)) causes the lower trip point (V_L) to coincide with the trip point without hysteresis (V_{TRIP}), so that the entire hysteresis window occurs above V_{TRIP}. This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. It is useful for accurately detecting when a voltage falls past a threshold. The current through R1 and R2 should be at least 1µA to ensure that the 100nA (max over temperature) PFI input current does not shift the trip point. R3 should be larger than 82kΩ so it does not load down the $\overline{PFO}$ pin. Capacitor C1 is optional and adds noise rejection.

Early Power-Fail Warning Using the PFI Input

Critical systems often require an early warning indicating that power is failing. This warning provides time for the µP to store vital data and take care of any additional "housekeeping" functions before the power supply gets too far out of tolerance for the µP to operate reliably. If access to the unregulated supply is feasible, the power-fail comparator input (PFI) can be connected to the unregulated supply through a voltage-divider, with the power-fail comparator output ($\overline{PFO}$) providing the nonmaskable interrupt (NMI) to the µP (Figure 28).

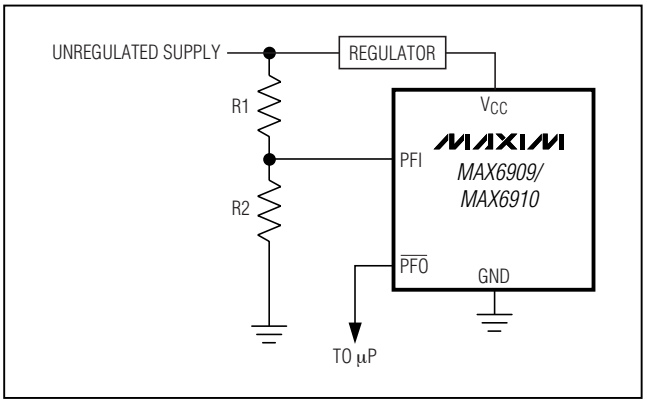
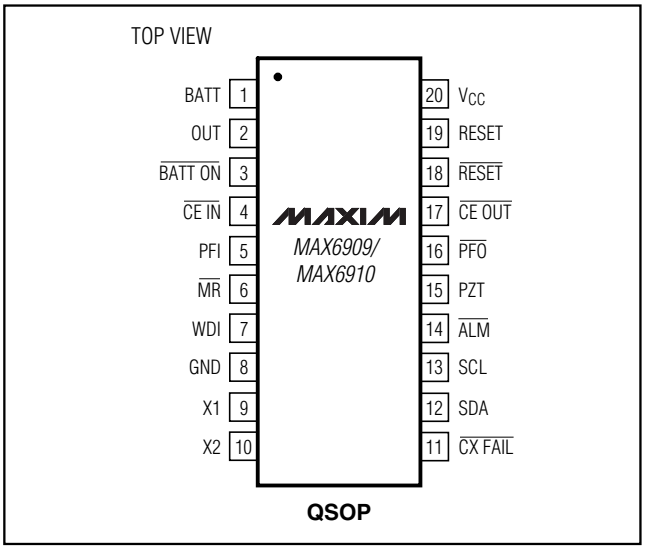


Figure 28. Using the Power-Fail Comparator to Generate a Power-Fail Warning

Selector Guide

PART	RESET THRESHOLD (TYP)	TRICKLE CHARGER
MAX6909EO30	2.63	No
MAX6909EO33	2.93	No
MAX6910EO30	2.63	Yes
MAX6910EO33	2.93	Yes

Pin Configuration



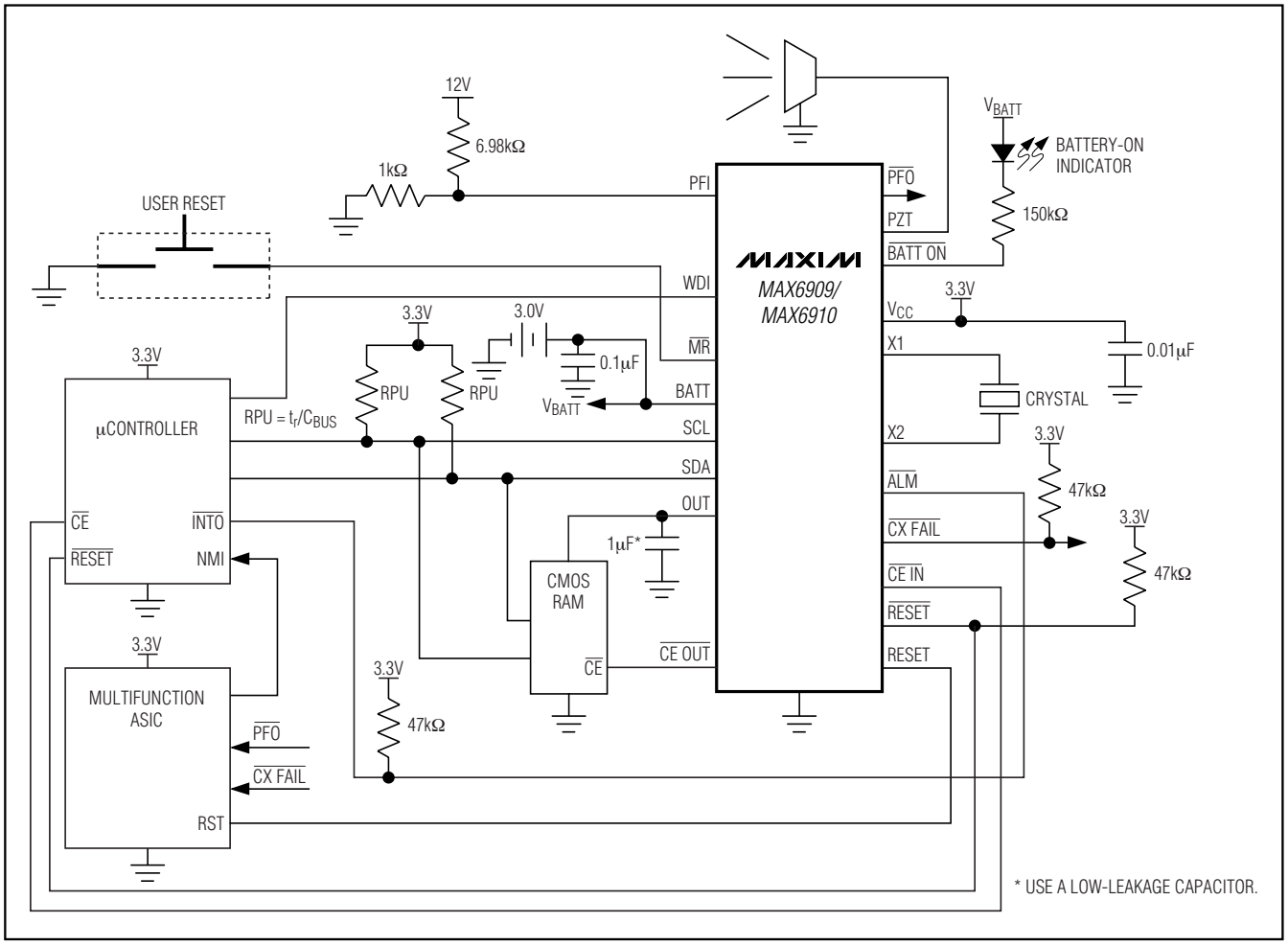
Chip Information

TRANSISTOR COUNT: 35,267

PROCESS: BiCMOS

I²C-Compatible Real-Time Clocks with µP Supervisor and NV RAM Controller

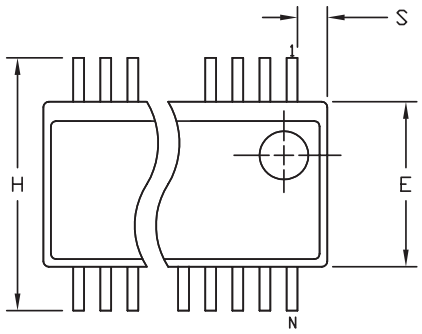
Typical Operating Circuit



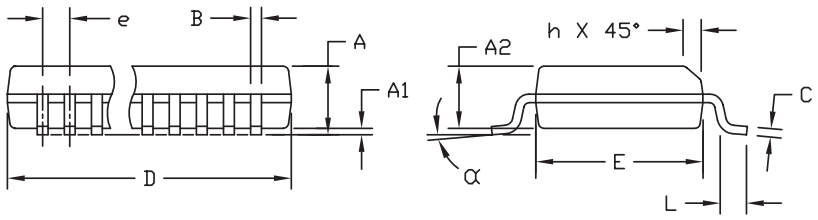
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1