TLV705xxxEVM-596 Evaluation Module

This user's guide describes the characteristics, operation, and use of the TLV705xxxEVM-596 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the Texas Instruments' TLV705 and TLV705P low-dropout linear regulators (LDOs). This user's guide includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials (BOM), and printed circuit board (PCB) layout drawings for the evaluation module. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the TLV705xxxEVM-596 unless otherwise noted.

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1 Introduction

The TLV705xxxEVM-596 EVM helps design engineers to evaluate the operation and performance of the TLV705xx family of linear regulators for possible use in their own circuit applications. This particular EVM configuration contains a single linear regulator with internal thermal and current limit shutdowns, and enable (disable) circuitry in an extremely small, 0.8-mm × 0.8-mm package. The regulator, including external components, is capable of delivering up to 200 mA to the load depending on the input-output power dissipation across the device. The TLV705xx does not require an input capacitor and the output capacitor must only be 1 µF (effective minimum) for stability; however, for conservative design practice that accounts for a wide variety of noisy environments and dynamic line/load conditions, a 1-µF capacitor is installed at the input and output ports.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TLV705xxxEVM-596.

2.1 Input / Output Connectors and Jumper Descriptions

J1: VIN

This connector is the input power-supply voltage connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize electromagnetic interference (EMI) transmission. Additional bulk capacitance should be added between J1 and J2 if the supply leads are greater than 6 in (15.24 cm) in length. For example, an additional 47-μF electrolytic capacitor connected from J1 to ground can improve the transient response of the TLV70528 while eliminating unwanted ringing on the input as a result of long wire connections.

J2: GND

This is the ground-return connection for the input power supply.

J3: VOUT

This is the regulated output voltage connector.

J4: GND

This is the output ground-return connector.

JP1: EN

This jumper is the output enable. To enable the output, connect a jumper to short the VIN pin (pin 1) to the EN center pin (pin 2). To disable the output, connect a jumper to short the EN pin to GND (pin 3).

2.2 Soldering Guidelines

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit (IC).

2.3 Equipment Setup

Follow these procedures to set up the test equipment properly.

- Turn off the input power supply after verifying that the output voltage is set to less than 5.5 V. Connect the positive voltage lead from the input power supply to VIN, at the J1 connector of the EVM. Connect the ground lead from the input power supply to GND at the J2 connector of the EVM.
- Connect a 0-mA to 200-mA load between the output (VOUT) at connector J3 and ground (GND) at connector J4.
- Disable the output by jumpering JP1, the EN pin, to the GND pin.

3 Operation

Follow these guidelines to correctly operate the TLV705xxxEVM-596.

- Turn on the input power supply. For initial operation, it is recommended that the input power supply, VIN – J1, be set to 3.8 V.
- Enable the output by reconnecting the jumper on JP1 from the EN pin to the VIN pin.
- Vary the respective loads and VIN voltages as necessary for test purposes.

4 Test Results

This section provides typical performance waveforms for the TLV70528EVM (with the 2.8-V version of the TLV705xx device installed).

4.1 Turn-On Sequence

Figure 1 shows the turn-on/-off characteristic where VIN is pre-set to 5.0 V, the output drives a full load, and the EN turn-on is stepped to 3.2 V (C2, white). The output soft start (C1, yellow) shows a monotonic rise time of approximately 50 μs after a built-in delay of approximately 70 μs. The output voltage startup ramp does not depend on the load.

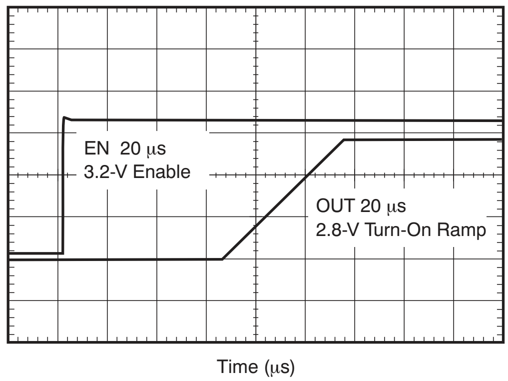


Figure 1. Turn-On Sequence

4.2 Output Load Transient

Figure 2 illustrates the load transient responsefor a full load step transient from 1 mA to 200 mA. VIN is set at 5 V.

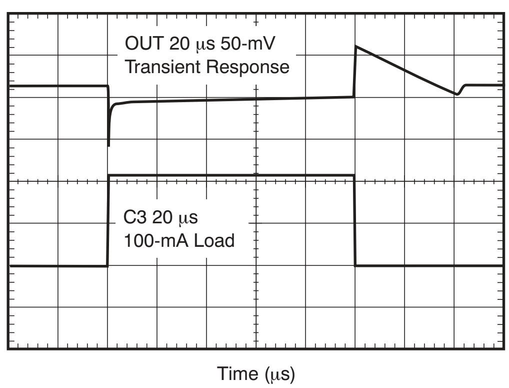


Figure 2. Load Step and Transient Response, Output Voltage Transient Response

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key design component of any power converter, and is especially important when the power dissipation in the LDO is high. Use Equation 1 to approximate the maximum power dissipation for the particular ambient temperature.

$$T_J = T_A + P_D \bullet \theta_{JA} \quad (1)$$

Where:

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation in the IC (in watts)
θ_{JA} = thermal resistance from junction to ambient

All temperatures are in degrees Celsius (°C).

The maximum silicon junction temperature, T_J, must not be allowed to exceed +150°C. The layout design must use copper trace and plane areas effectively as thermal sinks, in order not to allow T_J to exceed the absolute maximum ratings under all temperature conditions and voltage conditions across the application.

Designers should carefully consider the thermal design of the PCB for optimal performance over temperature. For this EVM, Figure 4 shows that the PCB top ground plane has six, 6-mil (0,1524-mm) thermal via connections to the bottom side copper ground plane to dissipate heat. The PCB is a two-layer board with 2-oz copper on top and bottom layers. The YFF package drawing can be found at the Texas Instruments web site in the TLV70528 LDO product folder.

Table 1 shows the Dissipation Ratings table of the TLV70528 data sheet for comparison with the thermal resistance, θ_{JA}, calculated for this EVM layout to show the wide variation in thermal resistances for given copper areas. The High-K value is determined using a standard JEDEC High-K (2s2p) board having dimensions of 3-inch x 3-inch with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

Table 1. Thermal Resistance (θ_{JA}) and Maximum Power Dissipation

Board	Package	θ_{JA}	Max Dissipation without Derating (T_A = +25°C)	Max Dissipation without Derating (T_A = +70°C)
High-K	YFF	268°C/W	370 mW	205 mW
TLV70528EVM	YFF	107°C/W	1.16 W	747 mW

The thermal resistance for the TLV705xxxEVM-596, θ_{JA}, is the measured value for this particular layout scheme. The maximum power dissipation is proportional to the volume of copper volume connected to the package.

6 Board Layout

This section provides the TLV705xxxEVM-596 board layout and schematic.

6.1 Layout

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TLV705xxxEVM-596 PCBs.

Figure 3 through Figure 5 show the PCB layouts.

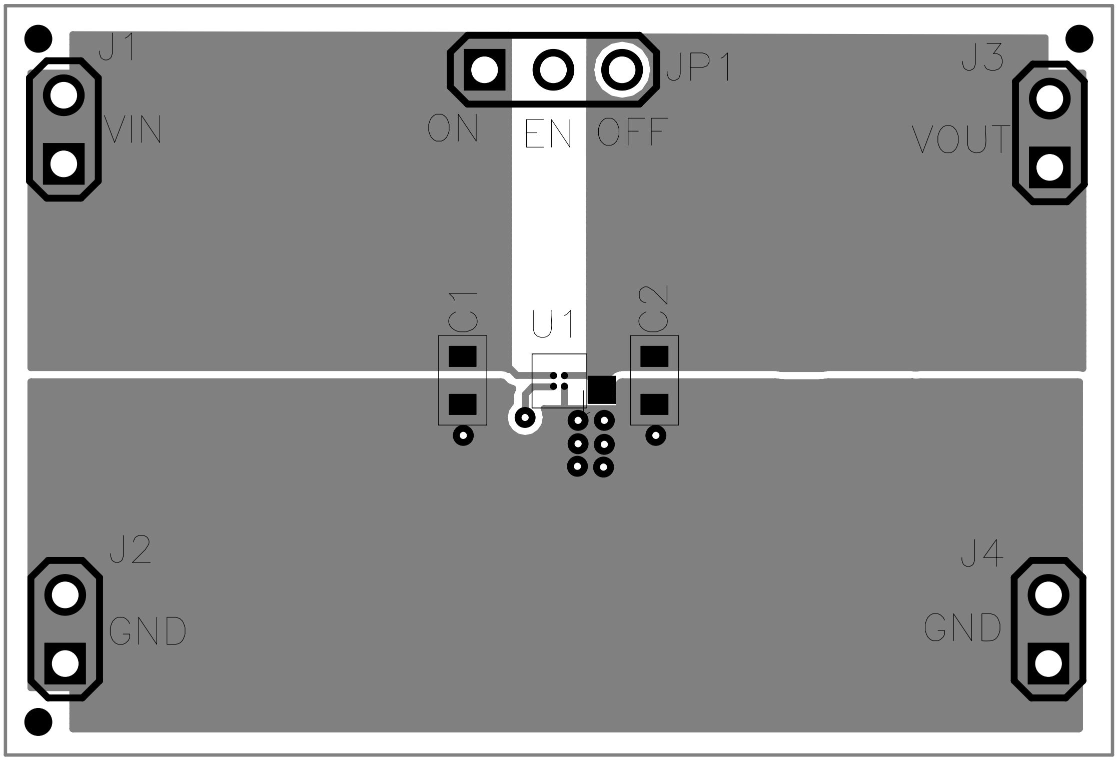


Figure 3. Assembly Layer

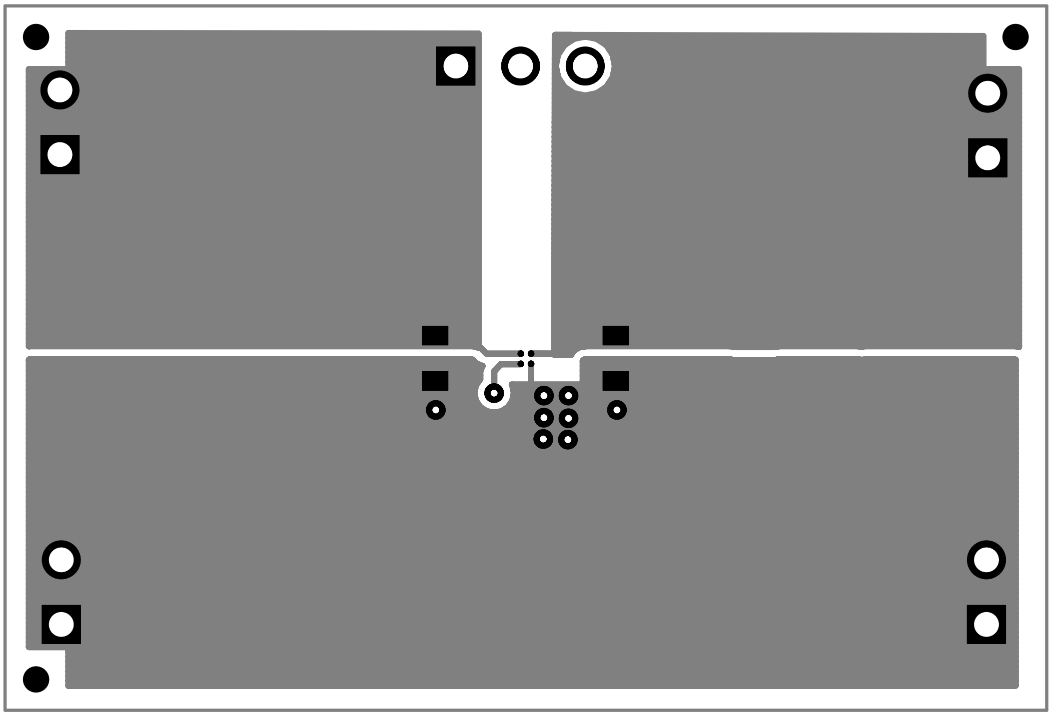


Figure 4. Top Layer Routing

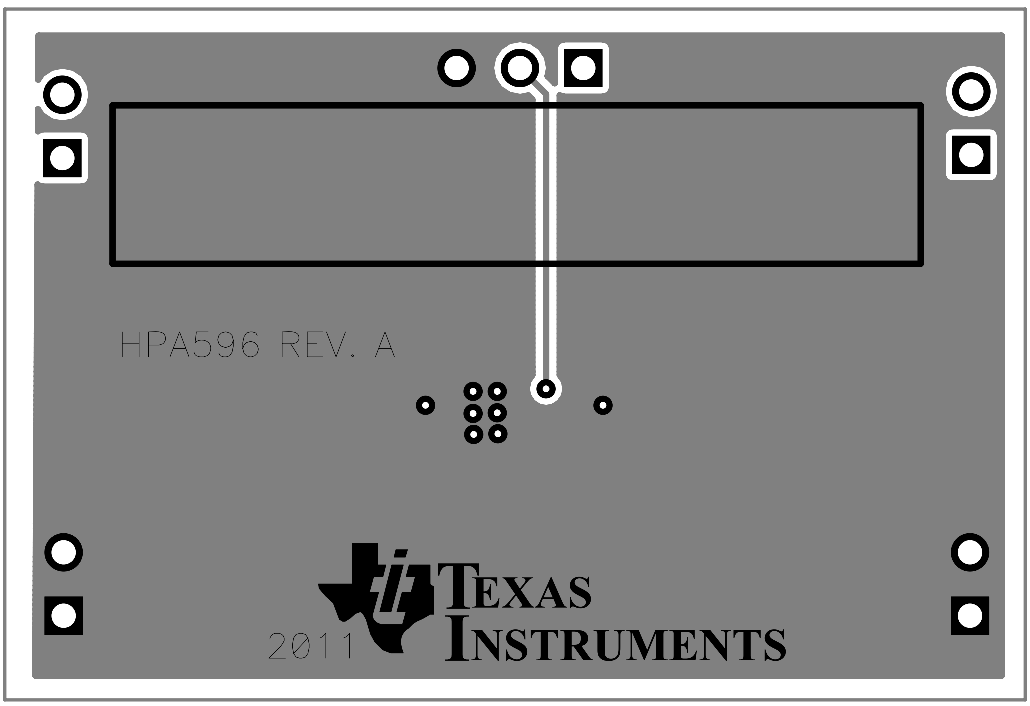
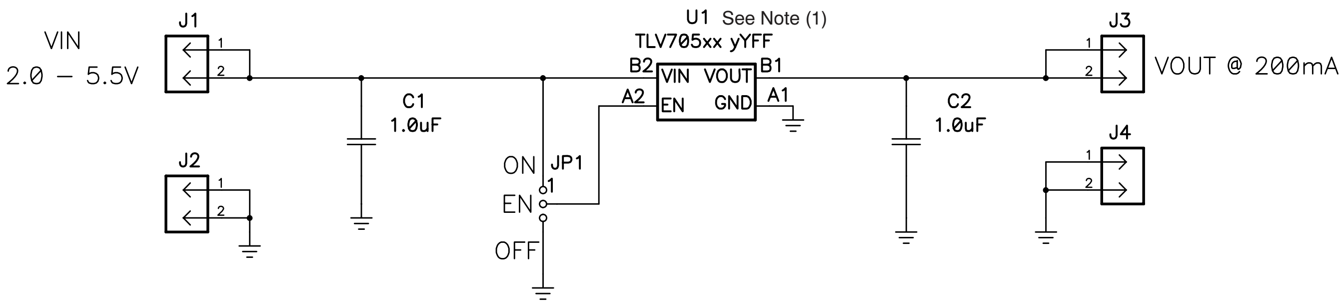


Figure 5. Bottom Layer Routing

6.2 Schematic

Figure 6 illustrates the schematic for this EVM.



(1) Refer to Table 2 for component values.

Figure 6. TLV705xxxEVM-596 Schematic

7 Bill of Materials

Table 2 lists the bill of materials for the TLV705xxxEVM-596.

Table 2. TLV705xxxEVM-596 Bill of Materials[(1)(2)(3)(4)(5)]

EVM Device Option: Count						RefDes	Value	Description	Size	Part Number, MFR
-001	-002	-003	-004	-005	-006					
2	2	2	2	2	2	C1, C2	1.0 µF	Capacitor, Ceramic, Low Inductance, 6.3V, X7R, 10%	0603	STD
4	4	4	4	4	4	J1, J2, J3, J4	PEC02SAAN	Header, 2-pin, 100-mil spacing	0.100 inch x 2	PEC02SAAN, Sullins
1	1	1	1	1	1	JP1	PEC03SAAN	Header, 3-pin, 100-mil spacing	0.100 inch x 3	PEC03SAAN, Sullins
1	0	0	0	0	0	U1	TLV70518YFF	IC, 200mA, Low IQ, LDO Regulator	WCSP	TLV70518YFF, TI
0	1	0	0	0	0	U1	TLV70518PYFF	IC, 200mA, Low IQ, LDO Regulator	WCSP	TLV70518PYFF, TI
0	0	1	0	0	0	U1	TLV70528YFF	IC, 200mA, Low IQ, LDO Regulator	WCSP	TLV70528YFF, TI
0	0	0	1	0	0	U1	TLV70528PYFF	IC, 200mA, Low IQ, LDO Regulator	WCSP	TLV70528PYFF, TI
0	0	0	0	1	0	U1	TLV70533YFF	IC, 200mA, Low IQ, LDO Regulator	WCSP	TLV70533YFF, TI
0	0	0	0	0	1	U1	TLV70533PYFF	IC, 200mA, Low IQ, LDO Regulator	WCSP	TLV70533PYFF, TI
1	1	1	1	1	1	—	Shunt	Shunt, 100-mil, Black	0.100	929950-00, 3M
1	1	1	1	1	1	—	HPA596	PCB, 1.090 In x1.610 In x 0.062 In	--	HPA596, Any
1	1	1	1	1	1	—	—	Label	1.25 x 0.25 inch	THT-13-457-10, Brady

(1) These assemblies are ESD sensitive; ESD precautions must be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of *no clean* flux is not acceptable.
(3) These assemblies must comply with IPC-A-610 Class 2 workmanship standards.
(4) All components may be substituted with equivalent manufacturer's components.
(5) Install label after final wash. Text must be 8-point font. Mark in accordance with assembly numbers shown in Table 3.

7.1 Marking Information

Table 3 provides the marking information for this EVM.

Table 3. Marking Information

Assembly Number	Marking Text
HPA596-001	TLV70518EVM-596
HPA596-002	TLV70518PEVM-596
HPA596-003	TLV70528EVM-596
HPA596-004	TLV70528PEVM-596
HPA596-005	TLV70533EVM-596
HPA596-006	TLV70533PEVM-596

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of –0.3 V to 6.0 V and the output voltage range of +0.7 V to +4.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +125°C. The EVM is designed to operate properly with certain components above +125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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