TPS78601/TPS79501/TPS79601DRB Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPS78601DRBEVM, TPS79501DRBEVM and TPS7960DRBEVM (or TPS7xx01DRBEVM). These EVMs demonstrate the operation and use of Texas Instruments' TPS78601, TPS79501 and TPS79601 low dropout linear regulators (LDOs), all in 3.00 mm x 3.00 mm SON-8 packages, which are capable of 1.5 A, 500 mA, and 1 A of output current, respectively. This user's guide includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials (BOM), and printed circuit board (PCB) layout drawings for the evaluation module. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the TPS7xx01DRBEVM, unless otherwise noted.

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1 Introduction

The TPS7xx01DRBEVM helps designers evaluate the operation and performance of the LDOs

Table 1 shows related devices.

Table 1. Related Devices

DEVICE	PACKAGE SIZE	ASSEMBLY	DESCRIPTION
TPS78601DRB	3.00 mm × 3.00 mm SON	HPA497-001	Ultra-Low Noise, High-PSRR, Fast-RF, 1.5 A, Low-Dropout Linear Regulator
TPS79501DRB	3.00 mm × 3.00 mm SON	HPA497-002	Ultra-Low Noise, High-PSRR, Fast-RF, 500 mA, Low-Dropout Linear Regulator
TPS79601DRB	3.00 mm × 3.00 mm SON	HPA497-003	Ultra-Low Noise, High-PSRR, Fast-RF, 1.0 A, Low-Dropout Linear Regulator

2 Setup

!~ *Section 2* describes the jumpers and connectors on the EVM and how to properly connect, set up, and use the TPS7xx01DRBEVM.

2.1 Input / Output Connector Descriptions

J1: VIN

This connector is the positive input supply voltage. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added between J1 and J2 if the supply leads are greater than six inches. A capacitor with a value of 47 µF or greater improves the transient response of the TPS7xx01DRB device and helps to reduce ringing on the input when long supply wires are used.

J2: GND

This is the return connection for the output.

J3: GND

This is the return connection for the input power supply of the regulator.

J4: VOUT

This is the positive connection from the output. Connect this pin to the positive input of the load.

J5: EN

This jumper is used to enable or disable the output of the TPS7xx01DRB device. Placing a shorting jumper between pins 1 and 2 (ON position) enables the TPS7xx01DRB device. Placing the shorting jumper between pins 2 and 3 (OFF position) disables the TPS7xx01DRB device.

J6: Output Voltage Select

This jumper sets the desired output voltage from the TPS7xx01DRB device. Placing a shorting jumper between the appropriate pins gives the outputs shown in Table 2.

Table 2. Output Voltage Settings

SHORT PINS:	V_{OUT}
1 and 2	3.3V
3 and 4	2.8V
5 and 6	2.5V
7 and 8	1.8V

3 Operation

Section 3 provides information about the operation of the TPS7xx01DRBEVM.

3.1 General Operation

Connect the positive input power supply to J1. Connect the input power return (ground) to J3. The TPS7xx01DRB device has an absolute maximum input voltage of 6 V. TI recommends a maximum output voltage of 6 V. The highest input voltage may be less than 5.5 V because of thermal conditions. See the *Thermal Considerations* section of this manual to determine the highest input voltage.

Connect the desired load between J4 (positive lead) and J2 (negative or return lead). Configure jumper J6 for the desired output voltage.

4 Thermal Guidelines

Section 4 provides guidelines for the thermal management of the TPS7xx01DRBEVM board.

4.1 Thermal Considerations

Thermal management is a key design component of any power converter and is especially important when the power dissipation in the LDO is high. To better help you design the TPS7xx01DRB family into your application, the following formula should be used to approximate the maximum power dissipation at a particular ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA} \quad (1)$$

Where:

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation in the IC
θ_{JA} = thermal resistance from junction to ambient

All temperatures are in degrees Celsius (°C).

The measured thermal resistance from junction to ambient for the TPS7xx01DRBEVM has a typical value of 32°C/W. The recommended maximum operating junction temperature specified in the product data sheets for the TPS7xx01 family is +125°C. With these two pieces of information, the maximum power dissipation can be found by using Equation 1.

Table 3 shows the maximum input voltage that can be applied to the input of the TPS7xx01DRBEVM by device type and selected output voltage. The maximum input voltage shown provides the rated output current while keeping the junction temperature at or below the recommended +125°C. Values for two different ambient temperatures (+25°C and +85°C) are shown.

Table 3. Maximum Input Voltage versus Ambient Temperature and Output Voltage

DEVICE	I_{OUT} (A)	SELECTED OUTPUT VOLTAGE (V) FOR T_A = +25°C				SELECTED OUTPUT VOLTAGE (V) FOR T_A = +85°C			
		1.80	2.50	2.80	3.30	1.80	2.50	2.80	3.30
TPS78601DRB	1.50	3.88	4.58	4.88	5.38	2.63	3.33	3.63	4.13
TPS79501DRB	0.50	5.5(1)	5.5(1)	5.5(1)	5.5(1)	4.30	5.00	5.30	5.5(1)
TPS79601DRB	1.00	4.93	5.5(1)	5.5(1)	5.5(1)	3.05	3.75	4.05	4.55

(1) Not limited by thermals; limited by recommended input voltage.

5 Board Layout

!~ *Section 5* provides the TPS7xx01DRBEVM board layout and illustrations.

5.1 Layout

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out, and are not intended to be used for manufacturing TPS7xx01DRBEVM PCBs.

Figure 1 through Figure 3 show the PCB layouts.

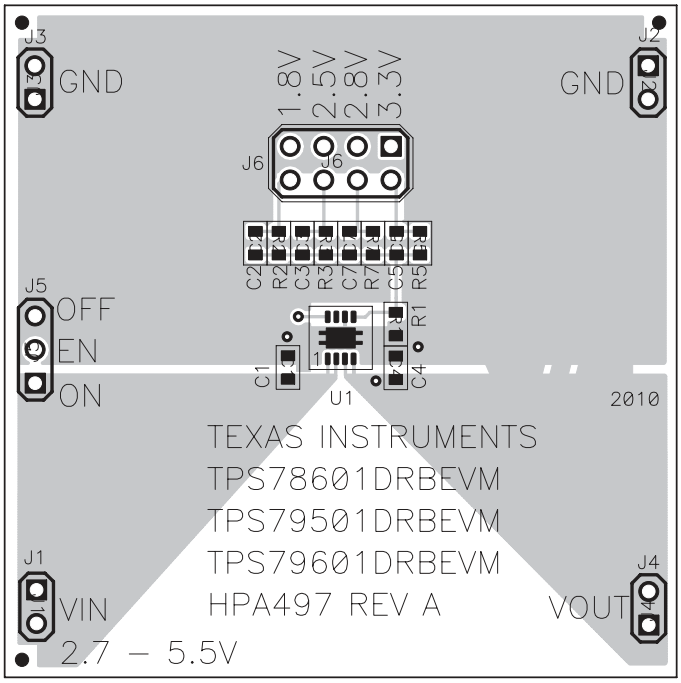

Figure 1. Top Layer Assembly

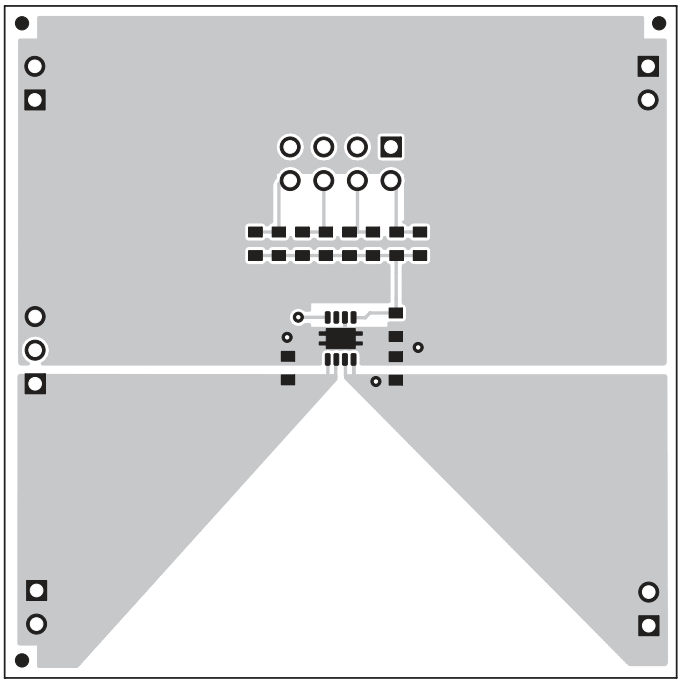

Figure 2. Top Layer Routing

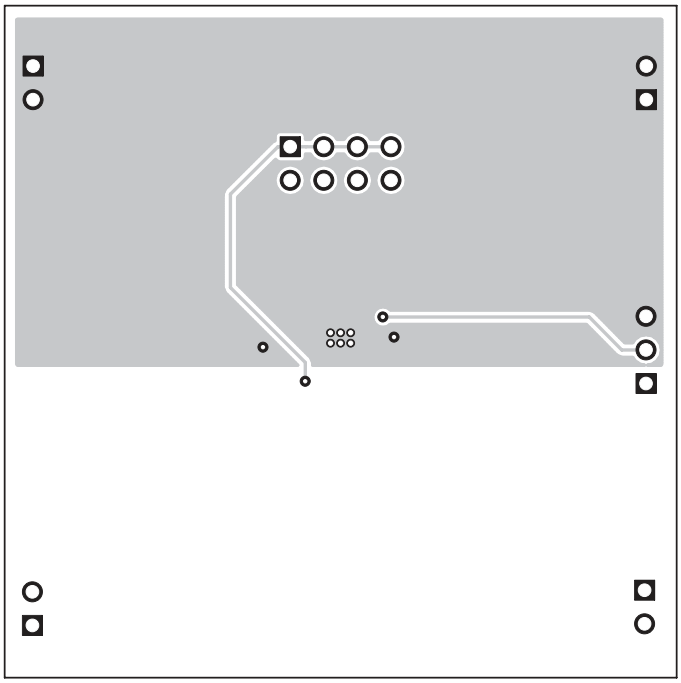

Figure 3. Bottom Layer Routing

6 Schematic and Bill of Materials

This section provides the TPS7xx01DRBEVM schematic and bill of materials.

6.1 Schematic

Figure 4 shows the TPS7xx01DRBEVM schematic.

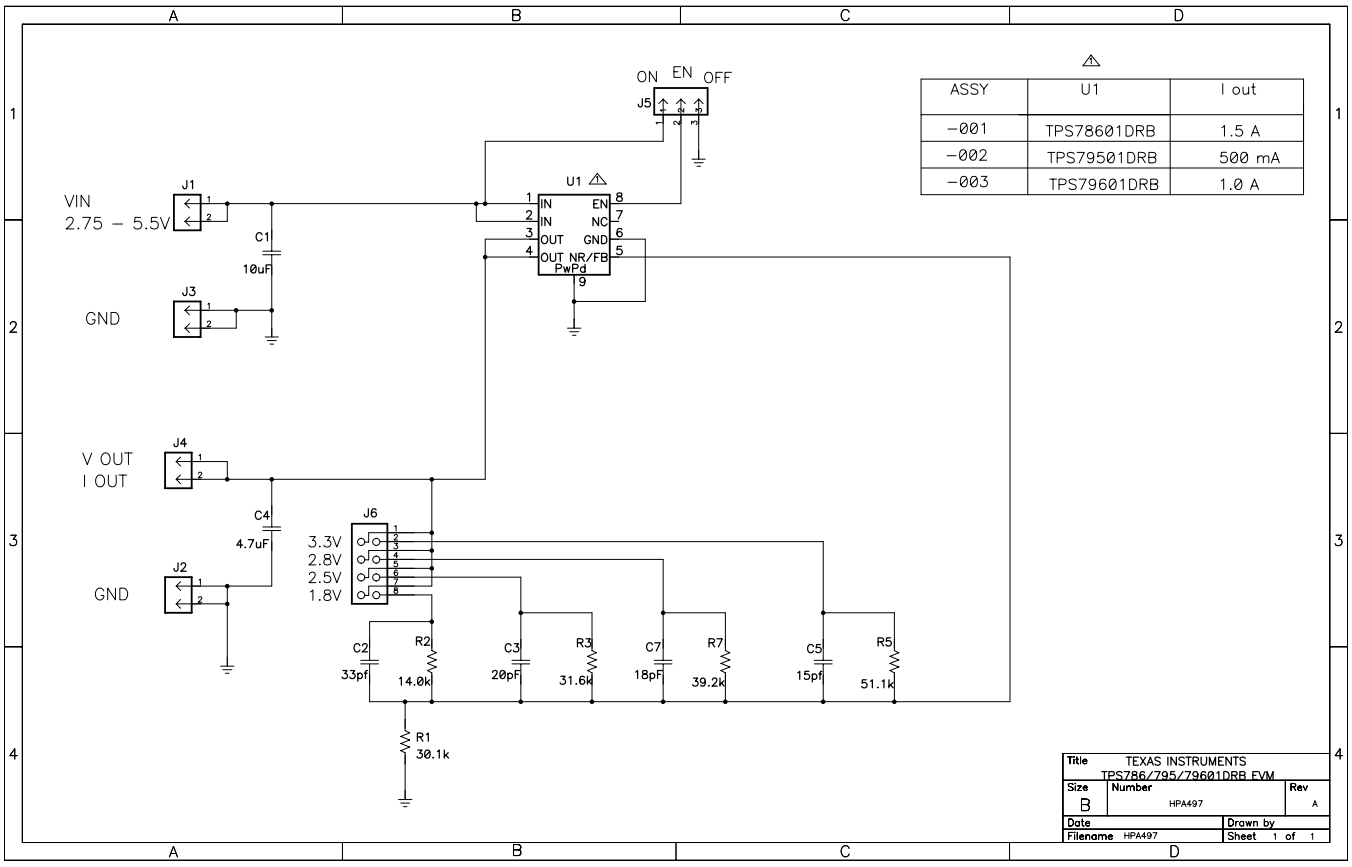

Figure 4. TPS7xx01DRBEVM Schematic

6.2 Bill of Materials

Table 4 lists the bill of materials for the TPS7xx01DRBEVM.

Table 4. TPS7xx01DRBEVM Bill of Materials[1][2][3]

001	002	003	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
1	1	1	C1	10 µF	Capacitor, Ceramic, Low Inductance, 6.3 V, X5R, 20%	0603	STD	STD
1	1	1	C2	33 pF	Capacitor, Ceramic, Low Inductance, 50 V, COG, 5%	0603	STD	STD
1	1	1	C3	20 pF	Capacitor, Ceramic, Low Inductance, 50 V, COG, 5%	0603	STD	STD
1	1	1	C4	4.7 µF	Capacitor, Ceramic, Low Inductance, 6.3 V, X5R, 20%	0603	STD	STD
1	1	1	C5	15 pF	Capacitor, Ceramic, Low Inductance, 50 V, COG, 5%	0603	STD	STD
1	1	1	C7	18 pF	Capacitor, Ceramic, Low Inductance, 50 V, COG, 5%	0603	STD	STD
4	4	4	J1, J2, J3, J4	PEC02SAAN	Header, Male 2-pin, 100-mil spacing	0.100"	PEC02SAAN	Sullins
1	1	1	J5	PEC03SAAN	Header, Male 3-pin, 100-mil spacing	0.100"	PEC03SAAN	Sullins
1	1	1	J6	PEC04DAAN	Header, Male 2 × 4-pin, 100-mil spacing	0.100"	PEC04DAAN	Sullins
1	1	1	R1	30.1 kΩ	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	1	1	R2	14.0 kΩ	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	1	1	R3	31.6 kΩ	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	1	1	R5	51.1 kΩ	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	1	1	R7	39.2 kΩ	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	—	—	U1	TPS78601DRB	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF	SON-8	TPS78601DRB	TI
—	1	—	U1	TPS79501DRB	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF	SON-8	TPS79501DRB	TI
—	—	1	U1	TPS79601DRB	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF	SON-8	TPS79601DRB	TI
1	1	1	—	—	PCB, 2.00 in × 2.00 in × 0.062 in	—	HPS497	Any
2	2	2	—	—	Shunt, 100-mil, Black	—	929950-00	3M

(1) These assemblies are ESD sensitive. ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of *no-clean flux* is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.7V to 5.5V and the output voltage range of 1.2V to 5.5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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