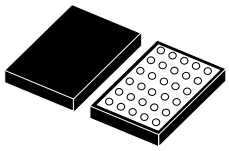
STG3820

Low voltage high bandwidth quad DPDT switch

Datasheet - production data



Flip Chip 30
(2.0 x 2.4 mm)

Features

- Ultralow power dissipation
  - I_{CC} = 1 µA (max.) at T_A = 85 °C
- Low “ON” resistance
  - R_{ON} = 5.4 Ω (T_A = 25 °C) at V_{CC} = 4.3 V
  - R_{ON} = 6.6 Ω (T_A = 25 °C) at V_{CC} = 3.0 V
- Wide operating voltage range
  - V_{CC} (OPR.) = 1.65 V to 4.3 V
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 V to 3.0 V
- 4 select pins controlling 2 switches each
- Typical bandwidth (-3 dB) at 800 MHz on all channels
- USB (2.0) high speed (480 Mbps) signal switching compliant
- Integrated fail safe function
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance exceeds JESD22 2000-V human body model (A114-A)

Applications

- Mobile phones

Description

The STG3820 device is a high-speed CMOS low voltage quad analog DPDT (dual pole dual throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65 V to 4.3 V, making this device ideal for portable applications.

The SELm-n input is provided to control the switches. The switches nS1 and mS1 are ON (connected to common ports Dn and Dm respectively) when the SELm-n input is held high and OFF (high impedance state exists between the two ports) when the SELm-n is held low. The switches nS2 and mS2 are ON (connected to common port Dn and Dm respectively) when the SELm-n input is held low and OFF (high impedance state exists between the two ports) when the SELm-n is held high.

The STG3820 device has an integrated fail safe function to withstand overvoltage condition when the device is powered off. Additional key features are fast switching speed, break-before-make-delay time and ultralow power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packing
STG3820BJR	Flip Chip 30 (2.0 x 2.4 mm)	Tape and reel

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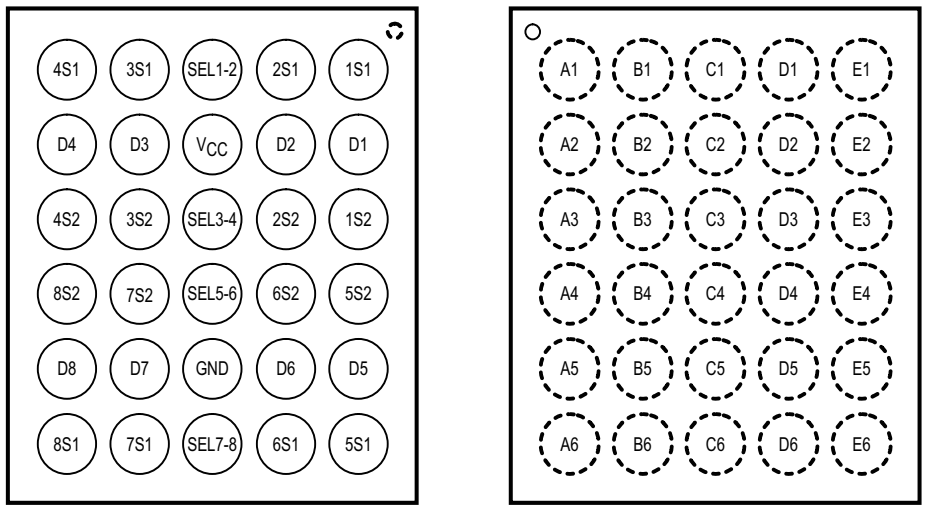
1 Pin settings

1.1 Pin connection

Figure 1. Pin connection



1.2 Pin description

Table 2. Pin assignment

Pin number	Symbol	Name and function
A1	1S1	Independent channel for switch 1
A2	D1	Common channel for switch 1
A3	1S2	Independent channel for switch 1
A4	5S2	Independent channel for switch 5
A5	D5	Common channel for switch 5
A6	5S1	Independent channel for switch 5
B1	2S1	Independent channel for switch 2
B2	D2	Common channel for switch 2
B3	2S2	Independent channel for switch 2
B4	6S2	Independent channel for switch 6
B5	D6	Common channel for switch 6
B6	6S1	Independent channel for switch 6

Table 2. Pin assignment (continued)

Pin number	Symbol	Name and function
C1	SEL1-2	Switch 1-2 selection control
C2	VCC	Positive supply voltage
C3	SEL3-4	Switch 3-4 selection control
C4	SEL5-6	Switch 5-6 selection control
C5	GND	Ground (0 V)
C6	SEL7-8	Switch 7-8 selection control
D1	3S1	Independent channel for switch 3
D2	D3	Common channel for switch 3
D3	3S2	Independent channel for switch 3
D4	7S2	Independent channel for switch 7
D5	D7	Common channel for switch 7
D6	7S1	Independent channel for switch 7
E1	4S1	Independent channel for switch 4
E2	D4	Common channel for switch 4
E3	4S2	Independent channel for switch 4
E4	8S2	Independent channel for switch 8
E5	D8	Common channel for switch 8
E6	8S1	Independent channel for switch 8

2 Logic diagram

Figure 2. Logic equivalent circuit

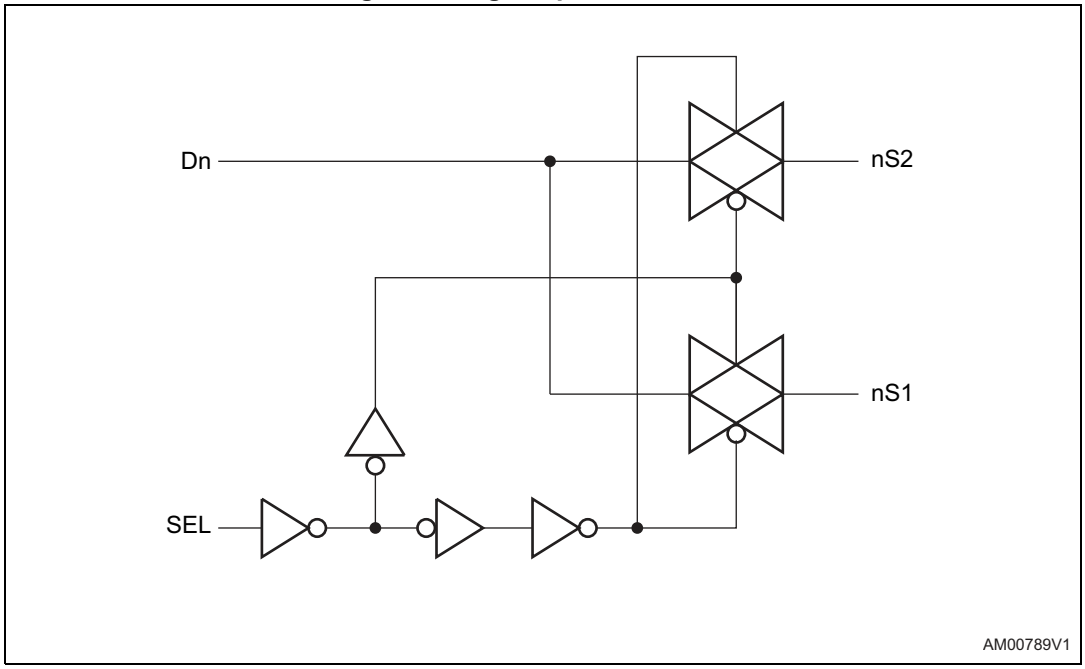


Table 3. Truth table

SEL	Switch nS1	Switch nS2
H	ON	OFF(1)
L	OFF(1)	ON

1. High impedance.

3 Maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 6.0	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL} < 0 V)	-50	mA
I_{IK}	DC input diode current (V_{SEL} < 0 V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±128	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±300	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70 °C	1120	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec.)	300	°C

Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_L = 1.65 V to 2.7 V	0 to 20	ns/V
		V_L = 3.0 V to 4.3 V	0 to 10	

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High level input voltage	1.65 – 1.95		0.65 V_{CC}	–	–	0.65 V_{CC}	–	V
		2.3 – 2.5		1.2	–	–	1.2	–	
		2.7 – 3.0		1.3	–	–	1.3	–	
		3.3 – 3.6		1.4	–	–	1.4	–	
		4.3		1.6	–	–	1.6	–	
V_{IL}	Low level input voltage	1.65 – 1.95		–	–	0.25	–	0.25	V
		2.3 – 2.5		–	–	0.25	–	0.25	
		2.7 – 3.0		–	–	0.25	–	0.25	
		3.3 – 3.6		–	–	0.30	–	0.30	
		4.3		–	–	0.40	–	0.40	
R_{PEAK}	Switch ON peak resistance	1.8	V_S = 0 V to V_{CC} I_S = 8 mA	–	17.0	19.6	–	–	Ω
		2.7		–	7.5	8.7	–	–	
		3.0		–	6.6	7.6	–	–	
		3.7		–	5.8	6.7	–	–	
		4.3		–	5.4	6.2	–	–	
R_{ON}	Switch ON resistance	3.0	V_S = 3 V I_S = 8 mA	–	5.1	5.8	–	–	Ω
		3.0	V_S = 0.4 V I_S = 8 mA	–	6.3	7.3	–	–	
ΔR_{ON}	ON resistance match between channels(1)	1.8	V_S at R_{ON} MAX I_S = 8 mA	–	–	–	–	–	Ω
		2.7		–	–	–	–	–	
		3.0		–	0.3	–	–	–	
		3.7		–	–	–	–	–	
		4.3		–	–	–	–	–	

Table 6. DC specifications (continued)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
R_{FLAT}	ON resistance flatness(2)	1.8	V_S = 0 V to 0.4 V I_S = 8 mA	–	4.5	–	–	–	Ω
		1.8	V_S = 0 V to V_{CC} I_S = 8 mA	–	9.5	–	–	–	
		2.7		–	2.2	–	–	–	
		3.0		–	1.8	–	–	–	
		3.7		–	1.6	–	–	–	
		4.3		–	1.6	–	–	–	
I_{OFF}	OFF state leakage current (Sn), (D)	4.3	V_S = 0.3 or 4 V	-20	–	20	-100	100	nA
I_{IN}	Input leakage current	0 to 4.3	V_{SEL} = 0 to 4.3 V	-0.2	–	0.2	-1.0	1.0	µA
I_{CC}	Quiescent supply current	1.65 to 4.3	V_{SEL} = V_{CC} or GND	-0.2	–	0.2	-1.0	1.0	µA
I_{CCLV}	Quiescent supply current for low voltage driving(3)	4.3	V_{SEL} = 1.65 V	–	±37	±50	–	±100	µA
			V_{SEL} = 1.80 V	–	±33	±40	–	±50	
			V_{SEL} = 2.60 V	–	±11	±20	–	±30	

1. ΔR_{ON} = max. |mSN - nSN|, where m = 1 to 8 and n = 1 to 8, N = 1, 2.
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
3. Measurement is for one SEL pin.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq$ 5 ns)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation delay	1.65 - 1.95		–	0.21	–	–	–	ns
		2.3 - 2.7		–	0.15	–	–	–	
		3.0 - 3.3		–	0.14	–	–	–	
		3.6 - 4.3		–	0.13	–	–	–	
t_{ON}	Turn-on time	1.65 - 1.95	V_S = 0.8 V	–	36	–	–	–	ns
		2.3 - 2.7	V_S = 1.5 V	–	20	23	–	26	
		3.0 - 3.3		–	15	17	–	20	
		3.6 - 4.3		–	13	15	–	17	
t_{OFF}	Turn-off time	1.65 - 1.95	V_S = 0.8 V	–	29	–	–	–	ns
		2.3 - 2.7	V_S = 1.5 V	–	19	22	–	25	
		3.0 - 3.3		–	14	16	–	18	
		3.6 - 4.3		–	11	13	–	14	
t_D	Break-before-make time delay	1.65 - 1.95	C_L = 35 pF R_L = 50 Ω V_S = 1.5 V	–	10	–	–	–	ns
		2.3 - 2.7		–	7	–	–	–	
		3.0 - 3.3		–	6	–	–	–	
		3.6 - 4.3		–	4	–	–	–	
Q	Charge injection	1.65	C_L = 100 pF V_{GEN} = 0 V R_{GEN} = 0 Ω	–	3.9	–	–	–	pC
		2.3		–	4.8	–	–	–	
		3.0		–	5.2	–	–	–	
		4.3		–	6.4	–	–	–	

Table 8. AC electrical characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
OIRR	OFF isolation(1)	1.65 – 4.3	V_S = 1 V_{RMS}, f = 1 MHz signal = 0 dBm	–	-78	–	–	–	dB
			V_S = 1 V_{RMS}, f = 10 MHz signal = 0 dBm	–	-57	–	–	–	
Xtalk	Crosstalk	1.65 – 4.3	V_S = 1 V_{RMS}, f = 1 MHz signal = 0 dBm	–	-78	–	–	–	dB
			V_S = 1 V_{RMS}, f = 10 MHz signal = 0 dBm	–	-58	–	–	–	
BW	-3dB bandwidth	3.0 – 4.3	R_L = 50 Ω signal = 0 dBm	–	800	–	–	–	MHz
C_{IN}	Control pin input capacitance		V_{CC} = 0 V	–	2	–	–	–	pF
C_{Sn}	Sn port capacitance	3.3	F = 240 MHz, switch is enabled	–	6	–	–	–	pF
			F = 240 MHz, switch is disabled	–	2	–	–	–	
C_D	D port capacitance	3.3	F = 240 MHz	–	8	–	–	–	pF

1. Off isolation = 20 Log10 (V_D/V_S), V_D = output, V_S = input to off switch.

Table 9. USB related AC electrical characteristics

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
$t_{SK(0)}$	Channel-to-channel skew	3.0 - 3.6	C_L = 10 pF	–	26	–	–	–	ps
$t_{SK(P)}$	Skew of opposite transition of the same output	3.0 - 3.6	C_L = 10 pF	–	60	–	–	–	ps
T_J	Total jitter	3.0 - 3.6	R_L = 50 Ω C_L = 10 pF $t_R = t_F$ = 750 ps at 480 Mbps	–	130	–	–	–	ps

5 Test circuits

Figure 3. On-resistance

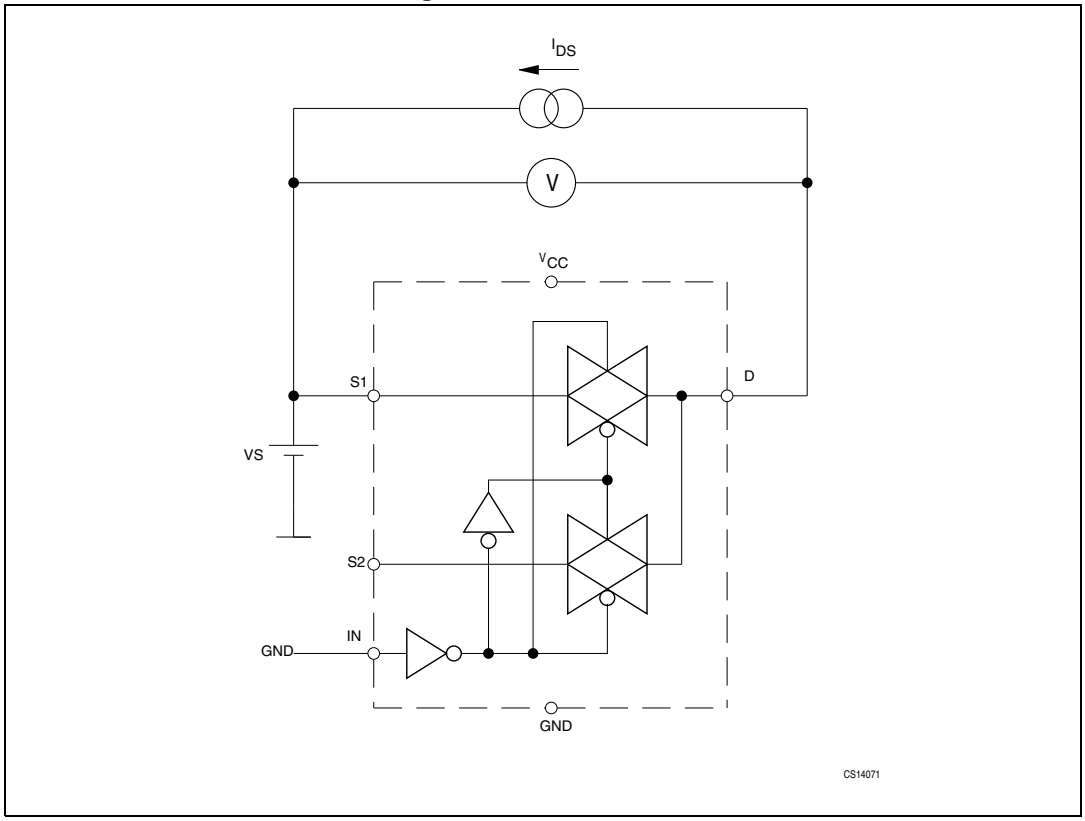


Figure 4. Bandwidth

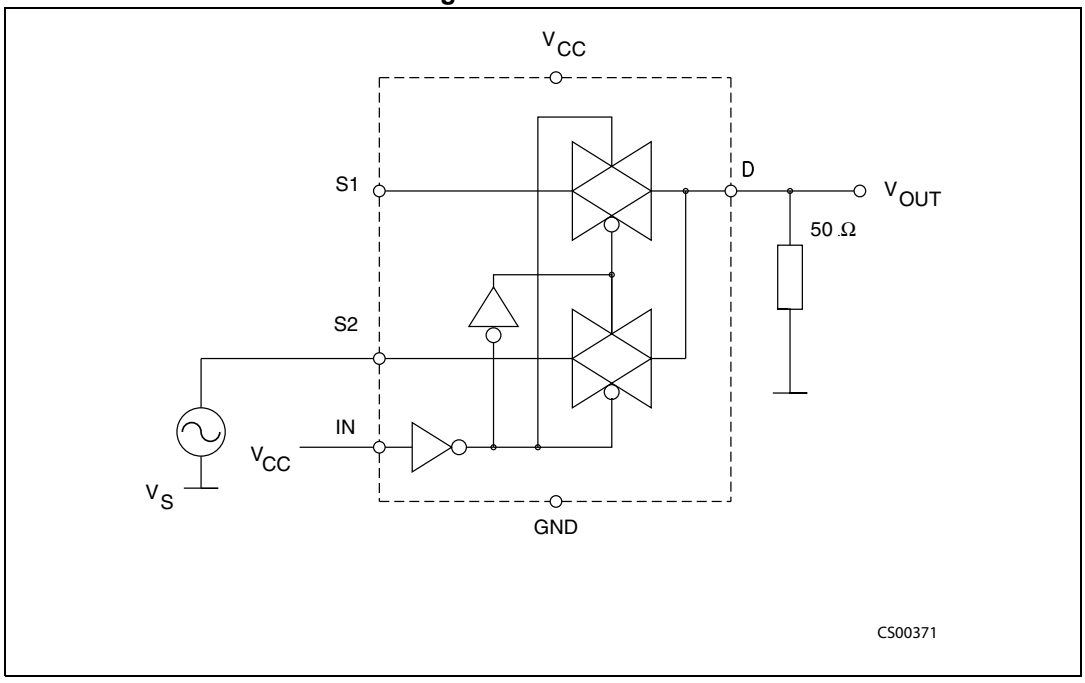


Figure 5. Off leakage

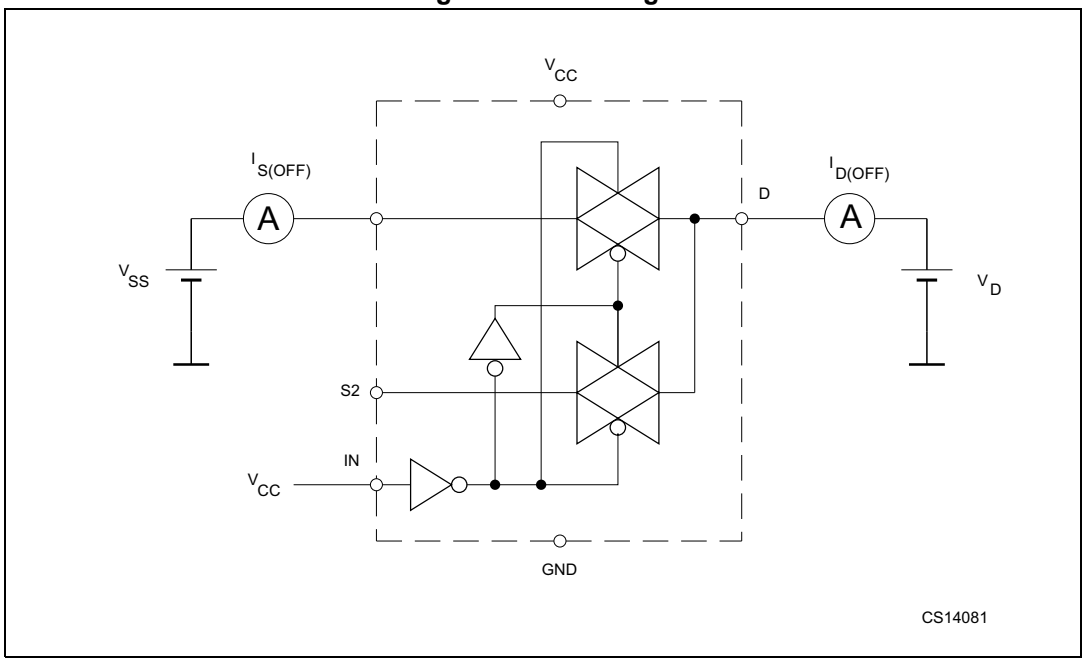


Figure 6. Channel to channel crosstalk

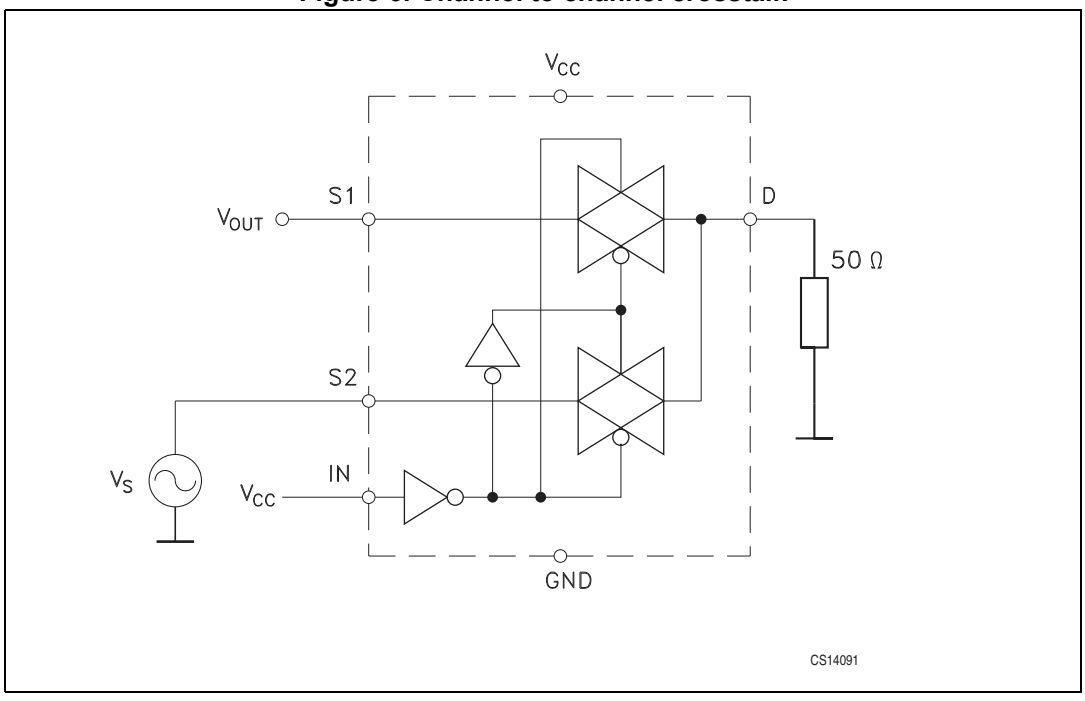


Figure 7. Off isolation

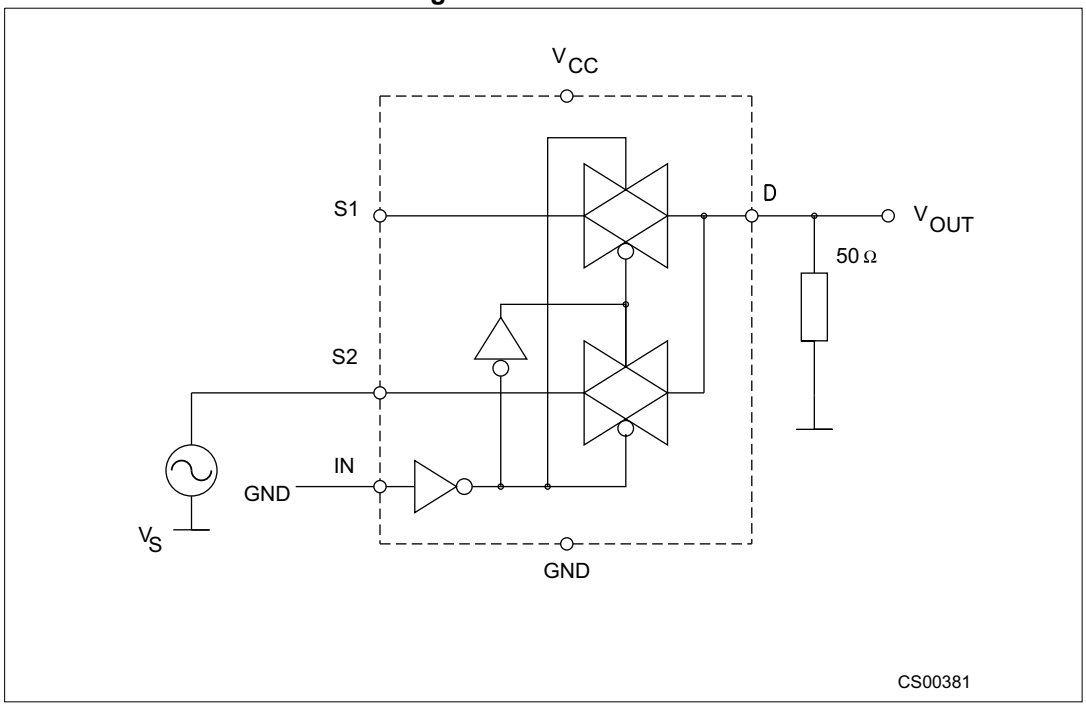
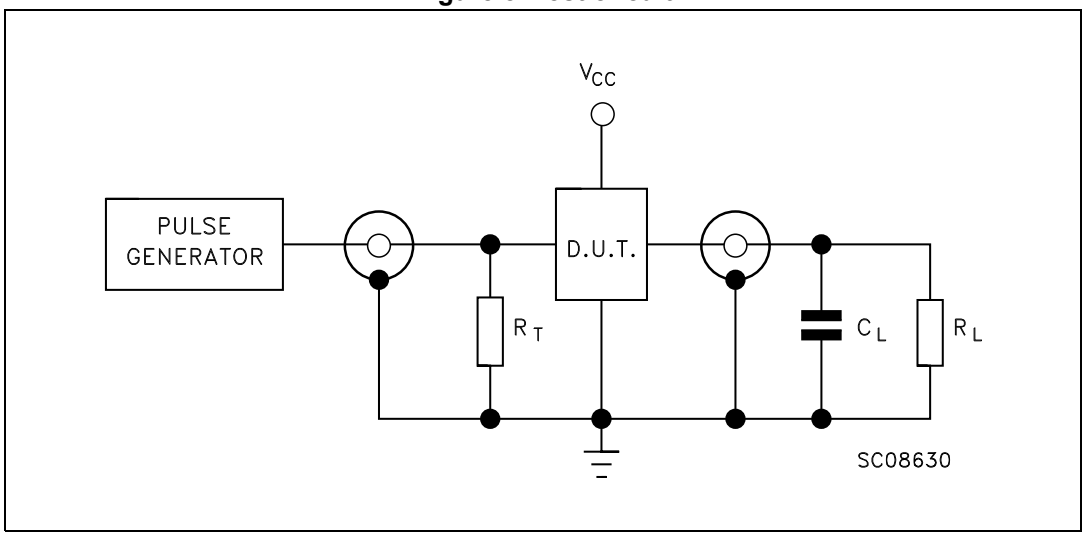


Figure 8. Test circuit



Note: *C_L = 5/35 pF or equivalent: (includes jig capacitance).*

R_L = 50 Ω or equivalent.

R_T = Z_{OUT} of pulse generator (typically 50 Ω).

Figure 9. Break-before-make time delay

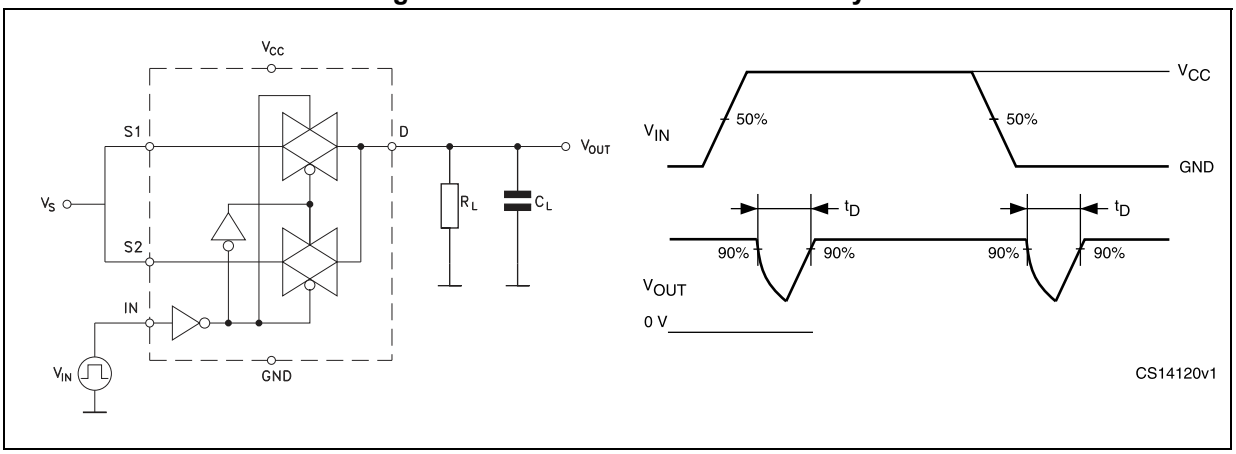


Figure 10. Switching time and charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF)

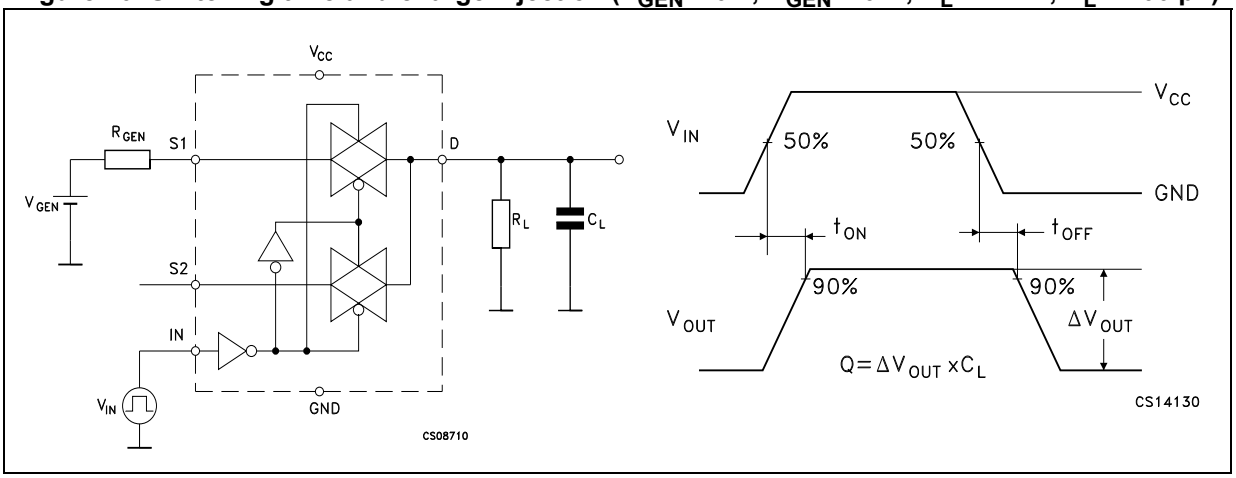
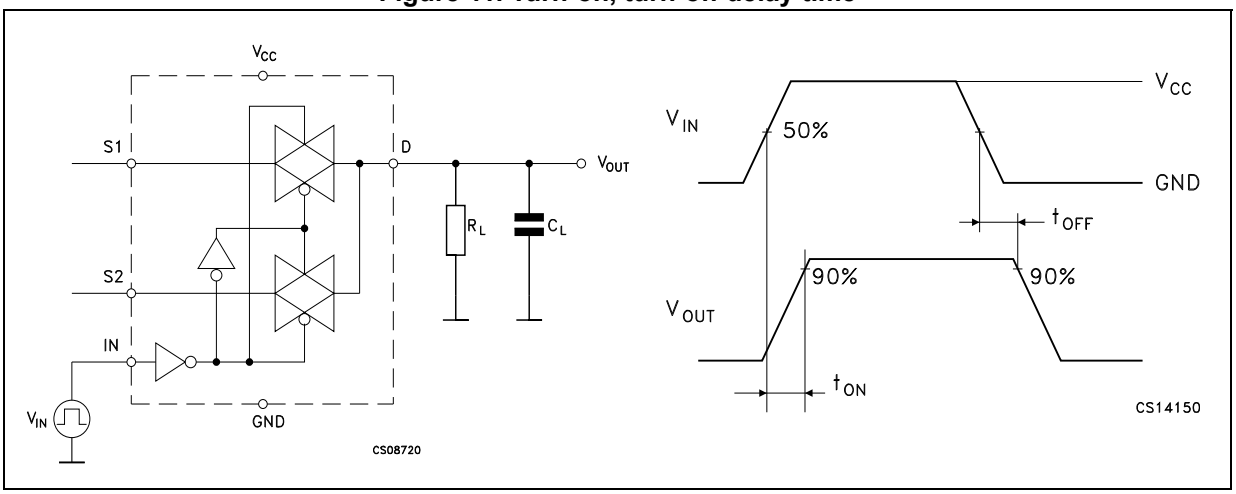


Figure 11. Turn-on, turn-off delay time



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 12. Package outline for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch

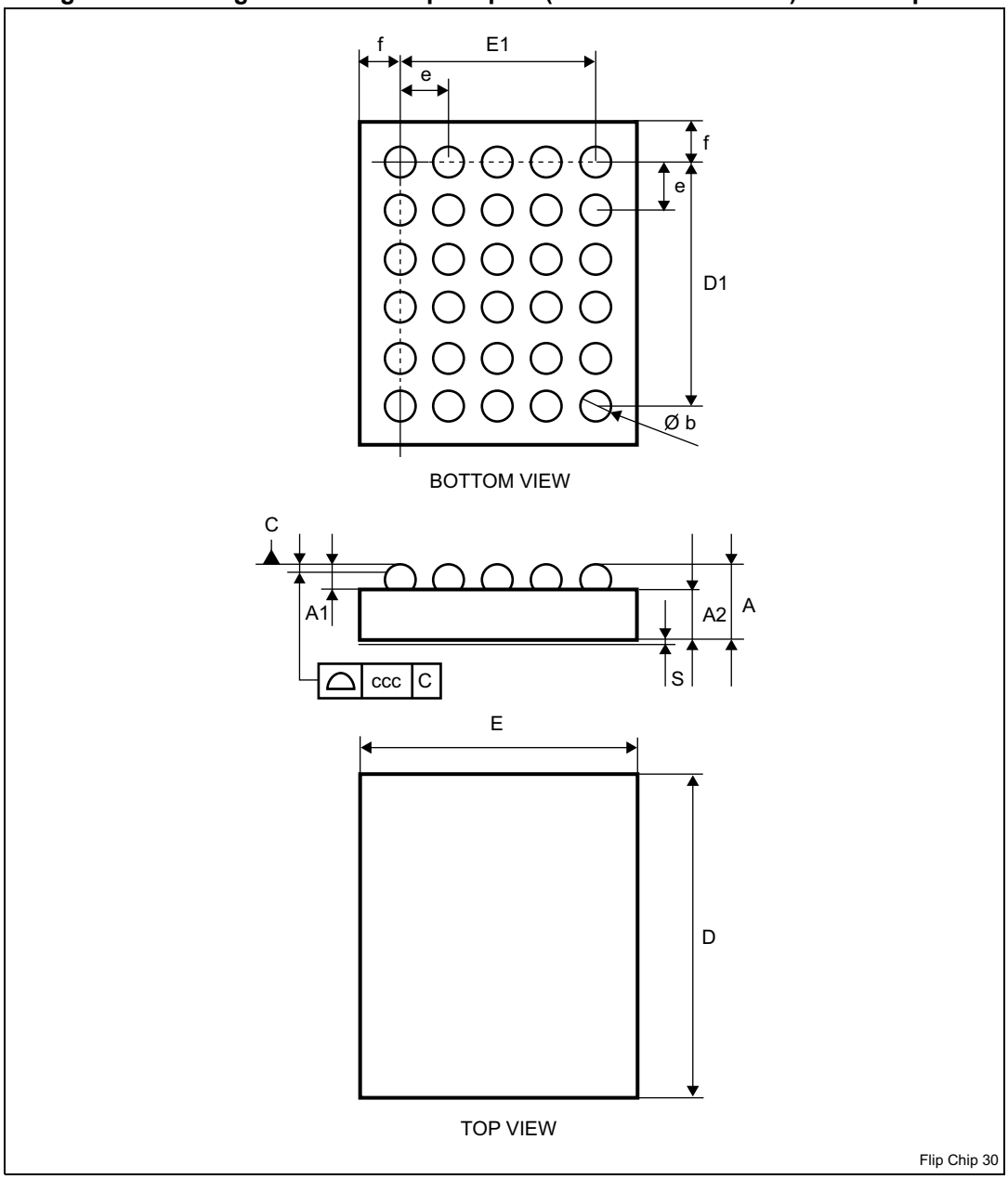


Table 10. Mechanical data for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.565	0.625	0.685
A1	0.17	0.205	0.24
A2	0.355	0.375	0.395
b	0.215	0.255	0.295
D	2.1	2.4	2.43
D1	–	2.0	–
E	1.97	2.0	2.03
E1	–	1.6	–
e	0.36	0.4	0.44
f	0.19	0.2	0.21
ccc	–	0.05	–
$	0.040	0.045	0.05

Figure 13. Footprint recommendations for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch

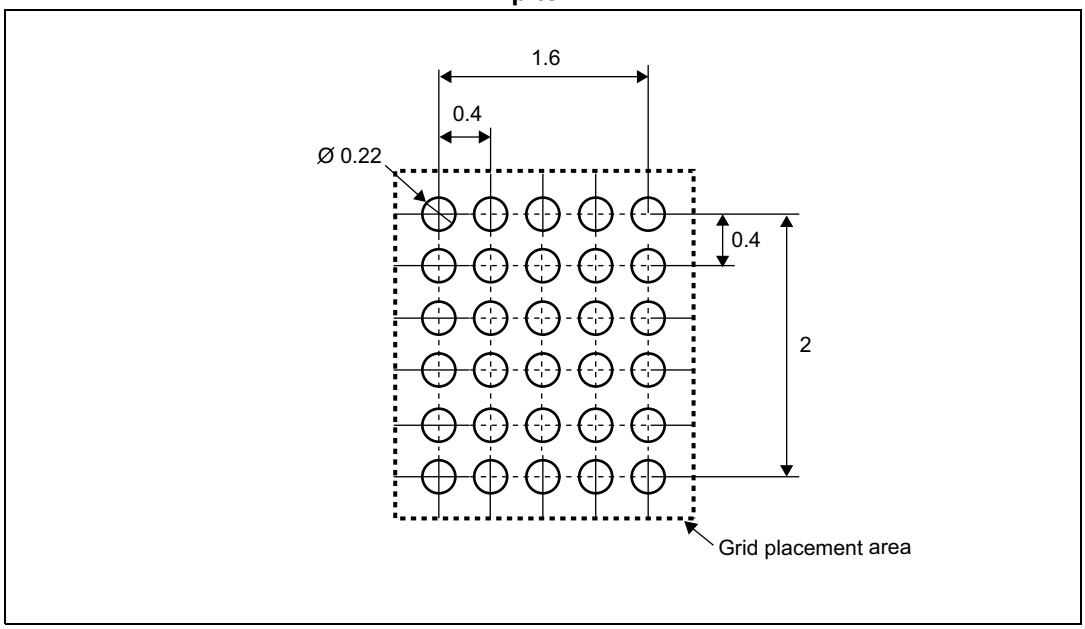


Figure 14. Tape information for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch

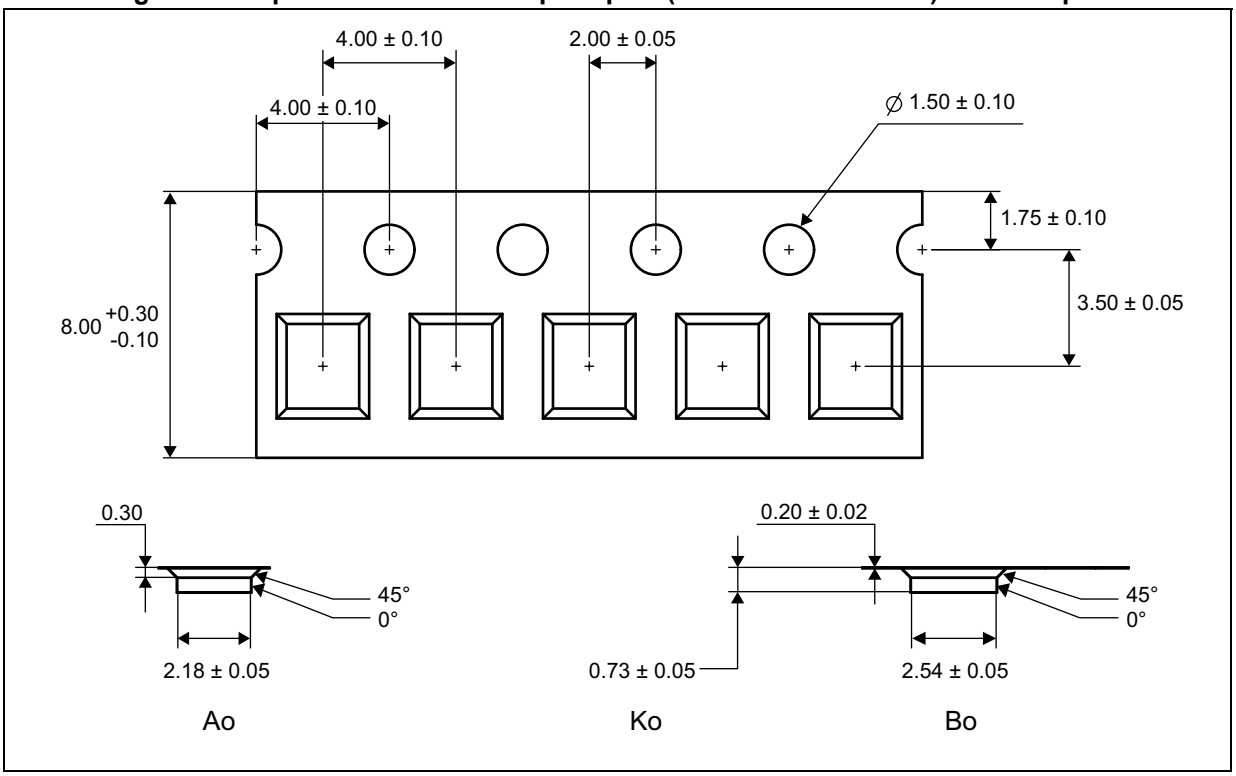
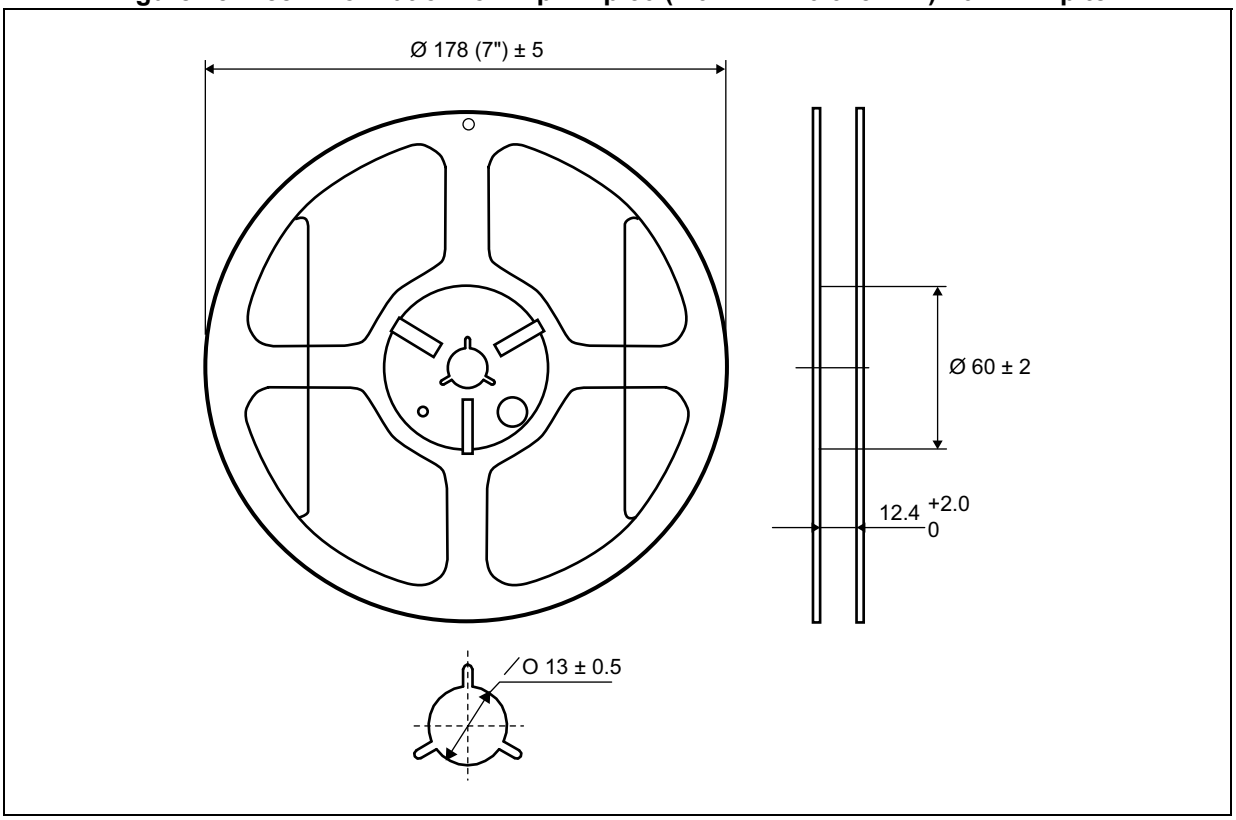


Figure 15. Reel information for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch



7 Revision history

Table 11. Document revision history

Date	Revision	Changes
18-Dec-2009	1	Initial release.
19-Jan-2011	2	Document reformatted, added *Contents*, updated *Figure 12* and *Figure 13*, corrected typo in *Features*, *Table 1*, *Section 1: Pin settings*, *Table 2*, *Table 7*, *Table 8*, notes below *Figure 8*, title of *Figure 11*, *Figure 12*, *Table 10*, and *Figure 13*, corrected name of “Table 11” to *Figure 13*.
23-Apr-2013	3	Moved *Description* to page 1. Redrawn *Figure 1*. Updated *Section 3* (added/updated cross-references, updated V_{CC} value in *Table 4*). Redrawn *Figure 12* to *Figure 15*. Updated *Figure 12* (removed superfluous reference to note). Updated title of *Figure 14* and *Figure 15* (added “Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch”). Minor corrections throughout document.
06-Aug-2013	4	Updated *Table 8 on page 10* (replaced C_{ON} and C_{OFF} symbol by C_{sn} and C_D symbol).

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