ANALOG DEVICES

EVAL-AD7177-2SDZ User Guide
UG-849

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Evaluating the AD7177-2 32-Bit, 10 kSPS, Sigma-Delta ADC with 100 µs Settling and Integrated Analog Input Buffers

FEATURES

Full featured evaluation board for the AD7177-2
PC control in conjunction with the system demonstration platform (SDP), see the EVAL-SDP-CB1Z data sheet for additional information
PC software for control and data analysis (time domain)
Standalone capability

EVALUATION KIT CONTENTS

EVAL-AD7177-2SDZ evaluation board
AD7177-2
AD717x Eval+ evaluation software (CD)
7 V to 9 V ac-to-dc adapter
Plastic screw and washer set

EQUIPMENT NEEDED

DC signal source
PC running Windows® XP, Windows 8, or Windows 10

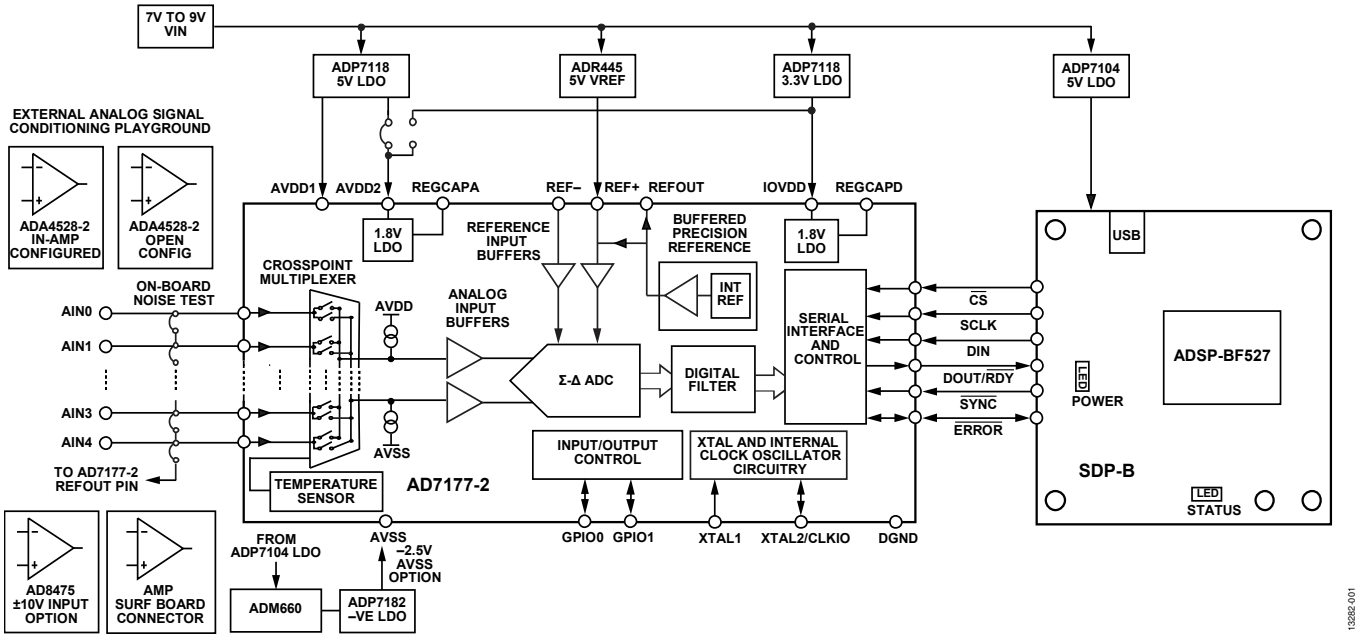
GENERAL DESCRIPTION

The EVAL-AD7177-2SDZ evaluation kit features the AD7177-2, a 32-bit, 10 kSPS analog-to-digital converter (ADC) with integrated rail to rail analog input buffers, on-board power supply regulation, and an external amplifier section for amplifier evaluation. A 7 V to 9 V ac-to-dc adapter is regulated to 5 V and 3.3 V that supplies the AD7177-2 and supports its components. The EVAL-AD7177-2SDZ evaluation board connects to the USB port of a PC via the EVAL-SDP-CB1Z (SDP-B) controller board.

The AD717x Eval+ software fully configures the AD7177-2 device functionality via an interactive block diagram and a user accessible register interface, and provides dc time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

For full specifications, see AD7177-2 data sheet, which must be consulted in conjunction with this user guide when using the evaluation board.

EVAL-AD7177-2SDZ FUNCTIONAL BLOCK DIAGRAM



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REVISION HISTORY

8/2018—Rev. 0 to Rev. A

Reorganized Layout ... Universal
Changes to Evaluation Kit Contents Section, Equipment Needed Section, and General Description Section ... 1
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Added Figure 10, Installing the .NET Framework 3.5 for Windows 8/Windows 10 Section, Figure 11, and Setting Up the System for Data Capture Section ... 11
Added Figure 13, Figure 14, and Figure 15 ... 12
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Deleted ADC Reset Section, Functional Block Diagram Section, Pop-Up Button Section, and Channel Configuration Overview Section ... 13
Added Select Product/Evaluation Mode Pane Section, Tutorial Icon Section, Functional Block Diagram and Configuration Pop-Up Buttons Section, and Analog and Digital Supply Voltage Section ... 13
Changed Software Operation Section Heading to Evaluation Board Software Operation Section ... 13
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6/2015—Revision 0: Initial Version

EVAL-AD7177-2SDZ QUICK START GUIDE

RECOMMENDED QUICK START GUIDE

To set up the evaluation board, take the following steps:

1. Disconnect the SDP-B board from the USB port of the PC.
2. Install the AD717x Eval+ software from the enclosed CD.
3. Restart the PC after installation.
4. Connect the SDP-B board to the EVAL-AD7177-2SDZ evaluation board, as shown in Figure 2.
5. Fasten the two boards together with the enclosed plastic screw and washer set.
6. Connect the external 9 V power supply to the J5 connector of the evaluation board as shown in Figure 2. Set Link LK2 to Position B.
7. Connect the SDP-B board to the PC via the USB cable. For Windows® XP, search for the SDP-B drivers. If prompted by the Windows operating system, choose to automatically search for the SDP-B drivers.
8. Launch the AD717x Eval+ software from the **Analog Devices** subfolder in the **Programs** menu.

QUICK START NOISE TEST

To test the noise performance, take the following steps:

1. Insert Link LK8 to Link LK12 to initiate the noise performance test mode. In this mode, the analog input channels short to the REFOUT pin.
2. Click **Sample** to acquire samples from the ADC (see Figure 16).

The **Samples** text field in the top right corner of the main window sets the number of samples collected in each batch (see Figure 16).

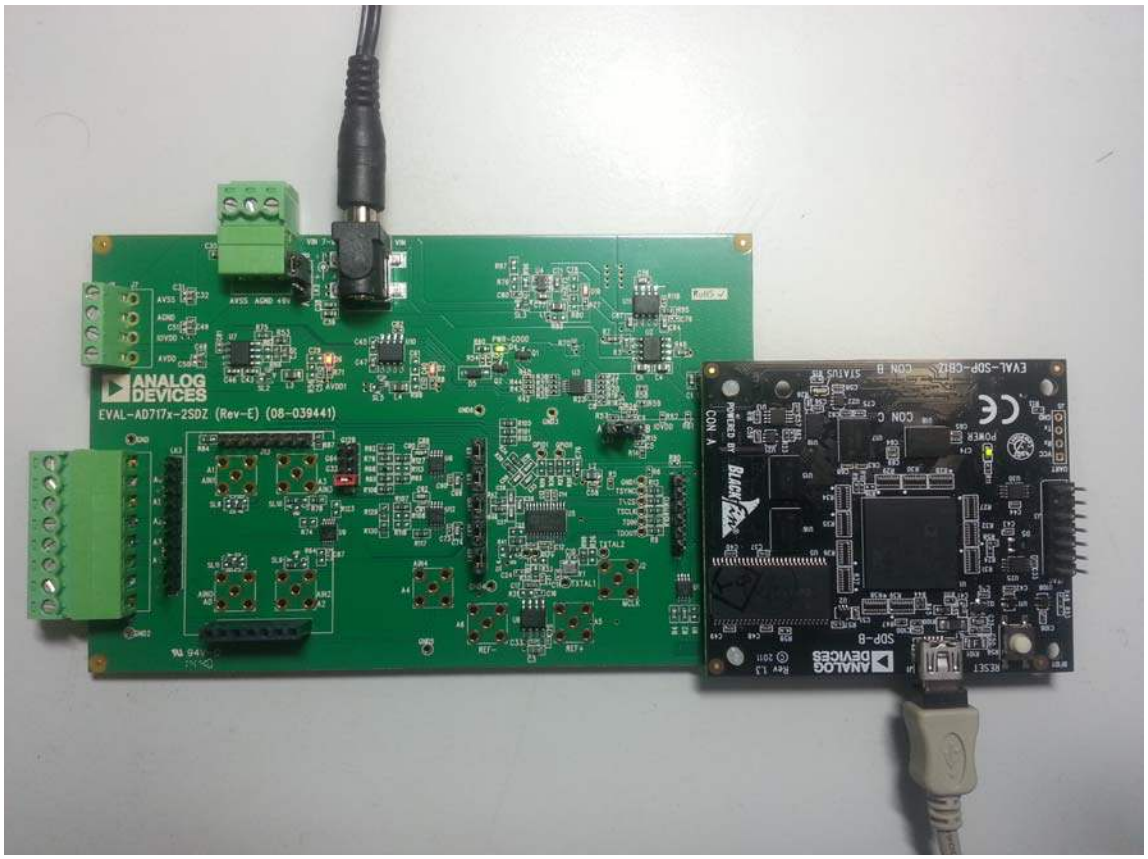

Figure 2. Hardware Configuration, Setting Up the EVAL-AD7177-2SDZ Evaluation Board

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7177-2 is a highly accurate, high resolution, multiplexed, 2-/4-channel (fully differential/single-ended) Σ-Δ ADC. The AD7177-2 has a maximum channel-to-channel scan rate of 10 kSPS (100 µs) for fully settled data. The output data rates range from 5 SPS to 10 kSPS. The device includes integrated rail-to-rail analog input and reference input buffers, an integrated precision 2.5 V reference, and an integrated oscillator.

See the AD7177-2 data sheet for complete specifications. Full details for the SDP-B board are available on the SDP-B product page on the Analog Devices website.

HARDWARE LINK OPTIONS

See Table 1 for default link options. By default, the EVAL-AD7177-2SDZ is configured to operate from the supplied 9 V ac-to-dc adapter connected to the J5 connector. The 5 V supply required for the AD7177-2 comes from the ADP7118 on-board, low dropout (LDO) regulator. The ADP7118, with a 5 V output voltage, receives its input voltage from the J3 connector or the J5 connector, depending on the position of LK2, and generates a 5 V output.

Table 1. Default Link and Solder Link Options

Link	Default Option	Description
LK1	A	Selects the voltage applied to the power supply sequencer circuit (U3); dependent on AVDD1. Place in Position A if using 5 V supply for AVDD1, or Position B if using 2.5 V supply for AVDD1.
LK2	B	Selects the external power supply from Connector J3 (Position A) or Connector J5 (Position B).
LK3 to LK7	Not inserted	Prior to inserting SL8 to SL11, inserting these links sets up the on-board noise test to short the on-board amplifiers, U8 and U9. In this mode, all inputs short to REFOUT.
LK8 to LK12	Inserted	Inserting these links sets up the on-board noise test close to the ADC analog inputs. In this mode, all inputs short to REFOUT.
SL1	A	Sets the voltage applied to the AVDD2 pin. Operates using the AVDD1 supply (default). Position B sets the AVDD2 voltage to the 3.3 V supply from the ADP7118 (3.3 V) (U10) regulator.
SL2	A	Selects between an external (Position B) or on-board (Position A) AVDD1 source. Supplies AVDD1 from the ADP7118 (5 V) (U7) (default).
SL3	A	Selects between an external ((Position B) or on-board (Position A) AVSS source. Supplies AVSS from the ADP7182 (−2.5 V) (U4) (default).
SL4	C	Connects AIN4 to: A4/J6 (Position A), REFOUT pin on the AD7177-2 (Position B), or AVSS (Position C). Position B and Position C are used to simplify the input using a single-ended input source.
SL5	B	Selects between an external or on-board IOVDD source. Supplies IOVDD from the ADP7118 (3.3 V) (U10) (default). The evaluation board operates with a 3.3 V logic.
SL8	A	Routes A0 to: AIN0 pin on the AD7177-2 (Position A), Buffer/In-Amp U8 (Position B), Funnel Amp U9 with gain of 0.8× (Position C), or J10-1 (Position D).
SL9	A	Routes A2 to: AIN2 pin on the AD7177-2 (Position A), Buffer U12 (Position B), or Funnel Amp U9 with gain of 0.4× (Position C).
SL10	A	Routes A3 to: AIN3 pin on the AD7177-2 (Position A), Buffer U12 (Position B), or Funnel Amp U9 with gain of 0.4× (Position C).
SL11	A	Routes A1 to: AIN1 pin on the AD7177-2 (Position A), Buffer/In-amp U8 (Position B), Funnel Amp U9 with gain of 0.8× (Position C), or J10-7 (Position D).
G16	Inserted	Sets the on-board in-amp (U8) to a gain of 16. Insert only one of the G16, G32, G64, or G128 links at a time.
G32	Not inserted	Sets the on-board in-amp (U8) to a gain of 32. Insert only one of the G16, G32, G64, or G128 links at a time.
G64	Not inserted	Sets the on-board in-amp (U8) to a gain of 64. Insert only one of the G16, G32, G64, or G128 links at a time.
G128	Not inserted	Sets the on-board in-amp (U8) to a gain of 128. Insert only one of the G16, G32, G64, or G128 links at a time.
R49 to R51	Inserted	Connects AVSS and AGND for single-supply operation. To operate in split supply mode, remove these links.

SOCKETS AND CONNECTORS

Table 2. Connector Details

Connector	Function	Connector Type	Manufacturer	Manufacturer Number	Stock Code[1]
J1	Connector to the SDP-B	120-way connector, 0.6 mm pitch	Hirose	FX8-120S-SV(21)	FEC1324660
J2	External MCLK input	Straight PCB mount SMB/SMA jack	TE Connectivity	1-1337482-0	Not applicable
J3	External bench top voltage supply for the EVAL-AD7177-2SDZ	Power socket block, 3-pin, 3.81 mm pitch	Phoenix Contact	MC 1.5/3-G-3.81	FEC3704737
J5	External ac-to-dc adapter input for the EVAL-AD7177-2SDZ, 7 V to 9 V	DC power connectors, 2 mm SMT power jack	Lumberg	161314	FEC1243245
J6	Analog input terminal block; wired connection to external source or sensor	Power socket block, 8-pin, 3.81 mm pitch	Phoenix Contact	MC 1.5/8-G-3.81	FEC3704774
J9	External bench top voltage supply option for AVDD1/AVDD2, IOVDD, and AVSS inputs on the AD7177-2	Screw terminal block, 3.81 mm pitch	Phoenix Contact	1727036	FEC3704592
J10	Optional header	7-way, 2.54 mm pin header	Samtec	SSW-107-01-T-S	FEC1803478
J13	Optional header	7-way, 2.54 mm socket	Samtec	TLW-107-05-G-S	FEC1668499
A0 to A4	Analog inputs to ADC	Straight PCB mount SMB/SMA jack	TE Connectivity	1-1337482-0	Not applicable
A7	PMOD-compatible header	6-Pin single inline (SIL) header (0.1 inch pitch)	Harwin	20-9990646	FEC 1022255

[1] FEC stands for Farnell Electronic Component Distributors.

SERIAL INTERFACE

The EVAL-AD7177-2SDZ evaluation board connects to the Blackfin® ADSP-BF527 on the SDP-B via the serial peripheral interface (SPI). The SPI has four primary signals: the $\overline{CS}$, SCLK, and DIN input signals, and the DOUT/$\overline{RDY}$ output signal.

To operate the evaluation board in standalone mode, disconnect the evaluation board from the SDP-B controller board. Use the test points to connect the signals to an alternative digital capture setup or the PMOD-compatible header (A7).

POWER SUPPLIES

Power the evaluation board from the ac-to-dc adapter connected to J5, or from an external bench top supply applied to J3 or J9. Linear LDOs generate the required voltages from the applied input voltage (V_{IN}) rail when using J3 or J5. Use J9 to bypass the on-board regulators. An ADP7118 regulator generates the 5 V (single supply) and 2.5 V (split supply) supplies for the AVDD1 and AVDD2 rails to the ADC; a second ADP7118 generates 3.3 V for the IOVDD rail. The ADP7104 supplies +5 V for the SDP-B controller board, as well as +5 V for the ADM660 voltage converter to generate −5 V to supply the ADP7182. The ADP7182 generates the −2.5 V supply for AVSS when operating in split supply mode. Each supply is decoupled where it enters the board and at each device in accordance with the schematics shown in Figure 24 to Figure 28. Table 3 shows the various power supply configurations available, including split supply operation.

Table 3. Power Supply Configurations[1]

Configuration	Input Voltage Range	Description
Single Supply (Regulated)	7 V to 9 V	The 7 V to 9 V input is regulated to 5 V for AVDD1/AVDD2 and 3.3 V for IOVDD. This input also powers the external 5 V reference. See the Single Supply (Regulated) section in the Power Supply Configurations section.
Single Supply (Unregulated)	7 V to 9 V, 5 V, and 3.3 V	The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Single Supply (Unregulated) section in the Power Supply Configurations section.
Split Supply (Regulated)	7 V to 9 V	The 7 V to 9 V input is regulated to +2.5 V for AVDD1/AVDD2, −2.5 V for AVSS and +3.3 V for IOVDD. The 7 V to 9 V input powers the external 5 V reference. See the Split Supply (Regulated) section in the Power Supply Configurations section.
Split Supply (Unregulated)	+7 V to +9 V, ±2.5 V, and +3.3 V	The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Split Supply (Unregulated) section in the Power Supply Configurations section.

[1] Only one configuration can be used at a time.

POWER SUPPLY CONFIGURATIONS

Single Supply (Regulated)

There are two available power supply options for the single supply (regulated) configuration.

- An ac-to-dc adapter (included) connected to J5. Set LK2 to Position B.
- A bench top power supply connected to J3. Set LK2 to Position A, and ensure that AVSS = AGND = 0 V.

Set all other links and solder links to the default settings as outlined in Table 1.

Single Supply (Unregulated)

To set up the evaluation board, use the following procedure:

1. Move SL2 to Position B and move SL5 to Position A.
2. Connect the two terminals of J9 labeled AGND and AVSS.
3. Connect 0 V (GND) to J9 at the terminal labeled AGND.
4. Connect 5 V to J9 at the terminal labeled AVDD.
5. Connect 3.3 V to J9 at the terminal labeled IOVDD.
6. Connect the 7 V to 9 V input to J5.

Set all other links and solder links to the default settings as outlined in Table 1.

Split Supply (Regulated)

To set up the evaluation board, use the following procedure:

1. Remove R49 to R52. These links connect AVSS to AGND.
2. Insert a 0 Ω resistor at R67 and R85.
3. Set LK1 to Position B, which sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.
4. Connect a bench top power supply to J5 and set LK2 to Position B.
5. Set LK1 to Position B, which sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.

Set all other links and solder links to the default settings as outlined in Table 1.

Split Supply (Unregulated)

To set up the EVAL-AD7177-2SDZ evaluation board, use the following procedure:

1. Move SL2 and SL3 to Position B and move SL5 to Position A.
2. Remove R49 to R52.
3. Insert a 0 Ω resistor at R67 and R85.
4. Connect 0 V (GND) to J9 at the terminal labeled AGND.
5. Connect 2.5 V to J9 at the terminal labeled AVDD.
6. Connect −2.5 V to J9 at the terminal labeled AVSS.
7. Connect 3.3 V to J9 at the terminal labeled IOVDD.
8. Connect 7 V to 9 V to J5.
9. Set LK1 to Position B. This sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.

Set all other links and solder links set to the default settings as outlined in Table 1.

ANALOG INPUTS

The primary analog inputs of the EVAL-AD7177-2SDZ evaluation board can be applied in two separate ways.

- J6 connector on the left side of the board
- A0 to A4 SMB/SMA footprints on the evaluation board

The analog inputs route directly to the associated analog input pins on the AD7177-2, provided that the LK5 to LK9 links (on-board noise test) are removed. The AD717x Eval+ software is set up to analyze dc inputs to the ADC. The AD7177-2 input buffers work for dc input signals.

REFERENCE OPTIONS

The EVAL-AD7177-2SDZ evaluation board includes an external 5 V reference, the ADR445. The AD7177-2 includes an internal 2.5 V reference. The default operation is to use the external reference input, which is set to accept the 5 V ADR445 on the evaluation board.

EVALUATION BOARD SOFTWARE INSTALLATION

Install the AD717x Eval+ software before connecting the evaluation board and the SDP-B board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts to the software installation, noted by the following:

1. AD717x Eval+ software installation
2. AD717x Eval+ Dependencies installation
   a. SDP-B board drivers
   b. Ssrc SVG plug-in
   c. Microsoft .NET Framework 3.5

INSTALLING THE AD717x Eval+ SOFTWARE

To install the AD717x Eval+ software, take the following steps:

1. Ensure that the SDP-B board is disconnected from the USB port of the PC and insert the CD into the CD-ROM drive.
2. Double click the **setup.exe** file to begin the evaluation board software installation. The default installation location for the software is **C:\Program Files\Analog Devices\ AD717x Eval+\.**
3. A dialogue box appears asking for permission to allow the program to make changes to the PC (See Figure 3). Click **Yes**.

*Figure 3. **User Account Control** Dialog Box*

4. Select a location to install the software and click **Next>>**. Figure 4 shows the default locations displayed when the dialogue box opens. To select another location click **Browse**.

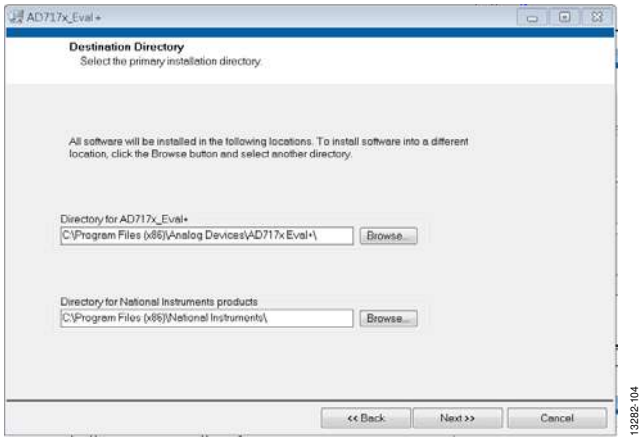

Figure 4. Selecting the Location for Software Installation

5. A license agreement appears. Read the agreement, select **I accept the License Agreement**, and click **Next>>** (see Figure 5).

Figure 5. Accepting the License Agreement

6. A summary of the installation displays. Click **Next>>** to continue (see Figure 6).

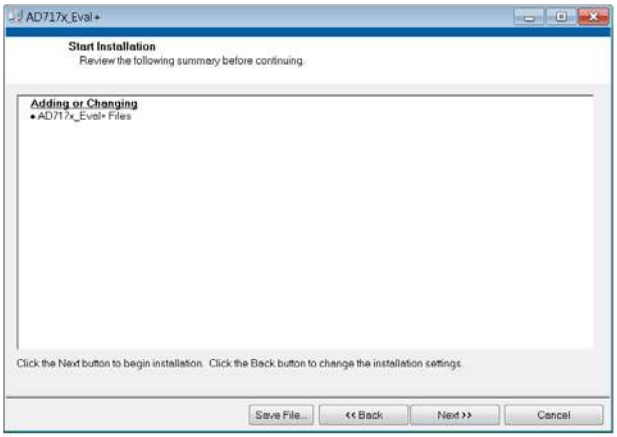

Figure 6. Reviewing a Summary of the Installation

7. The message shown in Figure 7 appears when the installation is complete.

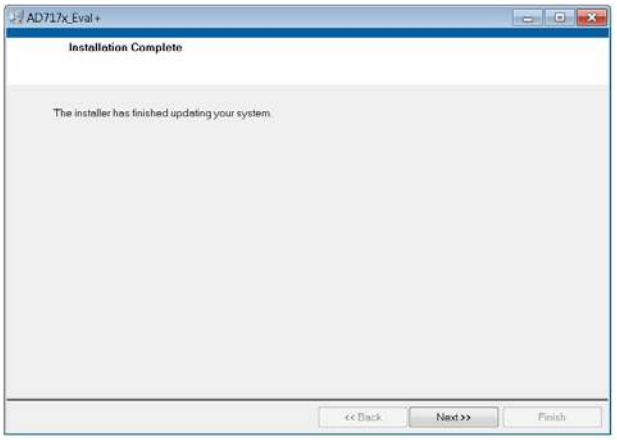

*Figure 7. **Installation Complete** Window*

INSTALLING THE Eval+ DEPENDENCIES

After the installation of the evaluation software is complete, a welcome window displays to install the **Eval+ Dependencies**.

1. Ensure that the SDP-B board is still disconnected from the USB port of the PC and that all other applications are closed, and then click **Install** (see Figure 8).

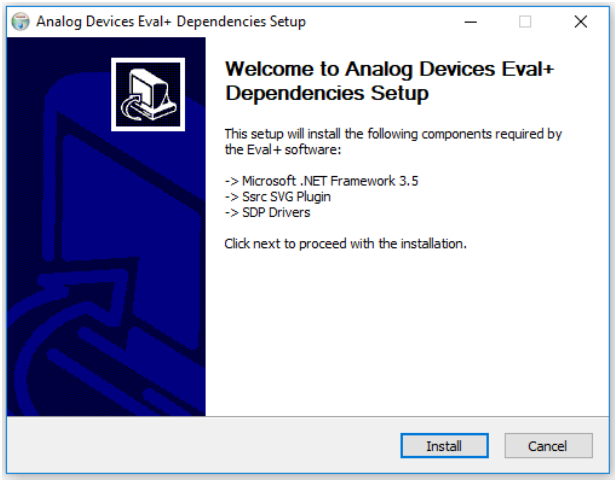

Figure 8. Beginning the Drivers Installation

2. The Ssrc SVG plug-in installs first, then the SDP-B drivers, and finally, the .NET Framework 3.5.
3. If using Windows 8 or Windows 10, see the Installing .NET Framework 3.5 for Windows 8/Windows 10 section.
4. To complete the SDP-B drivers installation and close the installation setup wizard, click **Close** (see Figure 9).

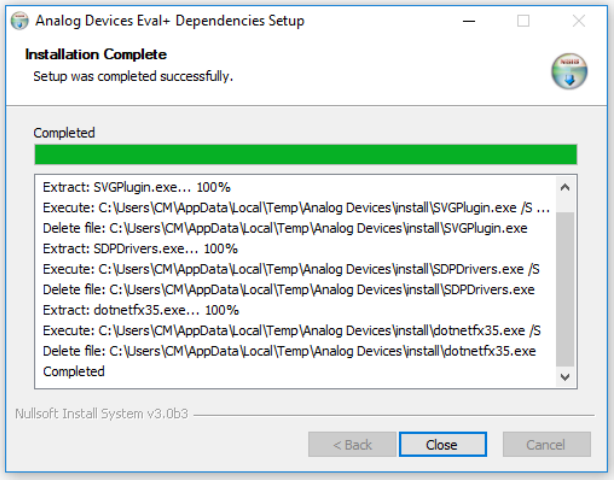

Figure 9. Completing the Drivers Setup Wizard

5. Before using the evaluation board, restart the PC (see Figure 10).

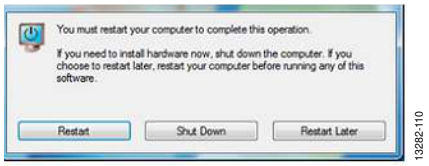

Figure 10. Restarting the PC

Installing .NET Framework 3.5 for Windows 8/Windows 10

Windows 8 and Windows 10 have a built in installer for the .NET Framework 3.5. To run this installer, an internet connection is required, and administrator privileges can be required. Contact a system administrator if the following steps do not work.

1. When the Eval+ Dependencies installer reaches the .NET Framework 3.5 installation step, a window appears, as shown in Figure 11.

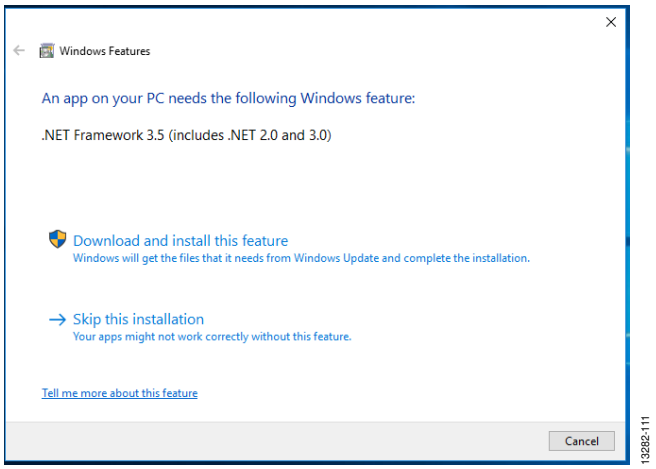

Figure 11. Windows 8/Windows 10 .NET Framework 3.5 Installation

2. Follow the steps shown in the installation wizard to complete the installation.
3. If the window shown in Figure 11 does not appear, the .NET Framework 3.5 may already be installed on the PC. To confirm that the software is installed, open the **Control Panel** > **Programs** > **Programs and Features**, and then select **Turn Windows features on or off**. In the pop up window, find .NET Framework 3.5 and confirm that the software is enabled.

SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Installing the AD717x Eval+ Software section and the Installing the Eval+ Dependencies section, take the following steps to set up the system for data capture:

1. Connect the SDP-B board to the PC and allow the **Found New Hardware Wizard** to run. If using Windows XP, search for the SDP-B drivers and choose to automatically search for the drivers if prompted by the operating system.
2. Use the **Device Manager** to confirm that the board is properly connecting to the PC.
3. Access the **Device Manager** by completing the following steps:
   a) From the **Start** menu, right-click **My Computer** and then click **Manage**.
   b) A dialog box appears asking for permission to allow the program to make changes to the PC. Click **Yes**.
   c) The **Computer Management** window appears. Click **Device Manager** from the list of **System Tools** (see Figure 12).
   d) The SDP-B board appears under **ADI Development Tools**, indicating that the driver software has installed and the board is connecting to the PC properly.

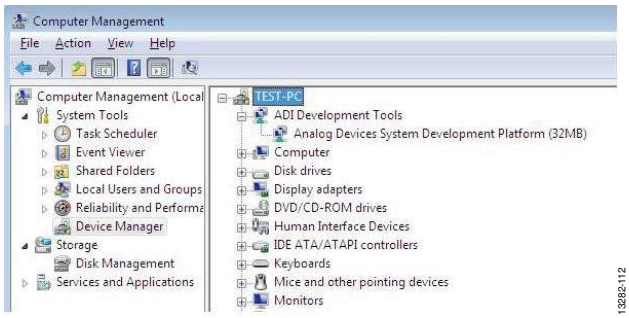

Figure 12. Device Manager

Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, take the following steps to launch the AD717x Eval+ software:

1. From the **Start** menu, click **Programs** > **Analog Devices** > **AD717x EVAL+** > **AD717x Eval+**.
2. The dialogue box in Figure 13 appears; select **AD7177-2 Evaluation Board** and click the **Select** button. The main window of the software box displays as shown in Figure 16.

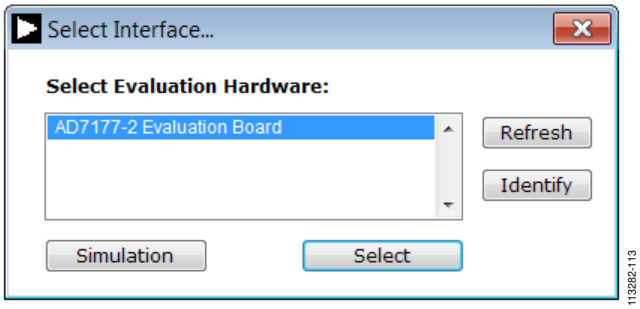

*Figure 13. **AD7177-2 Evaluation Board** Selection*

3. If the EVAL-AD7177-2SDZ evaluation system is not connected to the USB port via the SDP-B when the software is launched, the software displays the dialog box shown in Figure 14. Connect the evaluation board to the USB port of the PC; wait a few seconds, click **Refresh** and the option shown in Figure 13 appears.

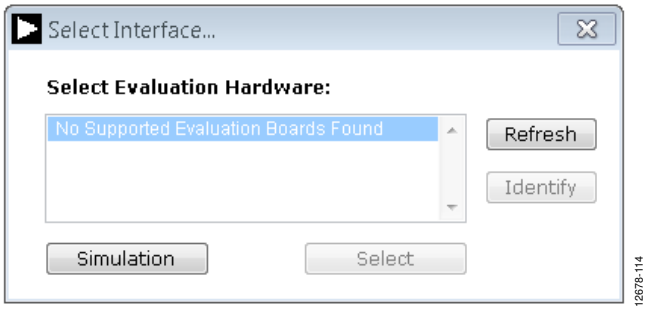

Figure 14. Evaluation Board Selection, No Board Connected

4. The AD717x Eval+ software can also be used without connecting hardware. Click the **Simulation** button and the options shown in Figure 15 appear. This option uses a software model and allows the AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, or AD7177-2 to be evaluated.

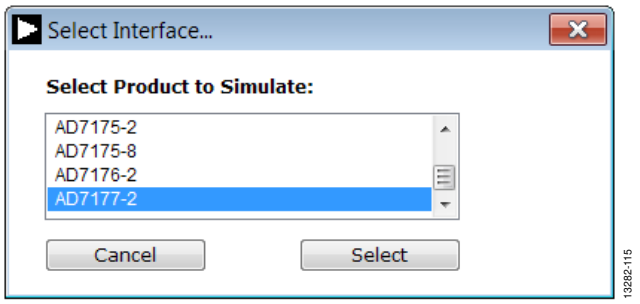

Figure 15. Evaluation Board Selection Simulation

EVALUATION BOARD SOFTWARE OPERATION

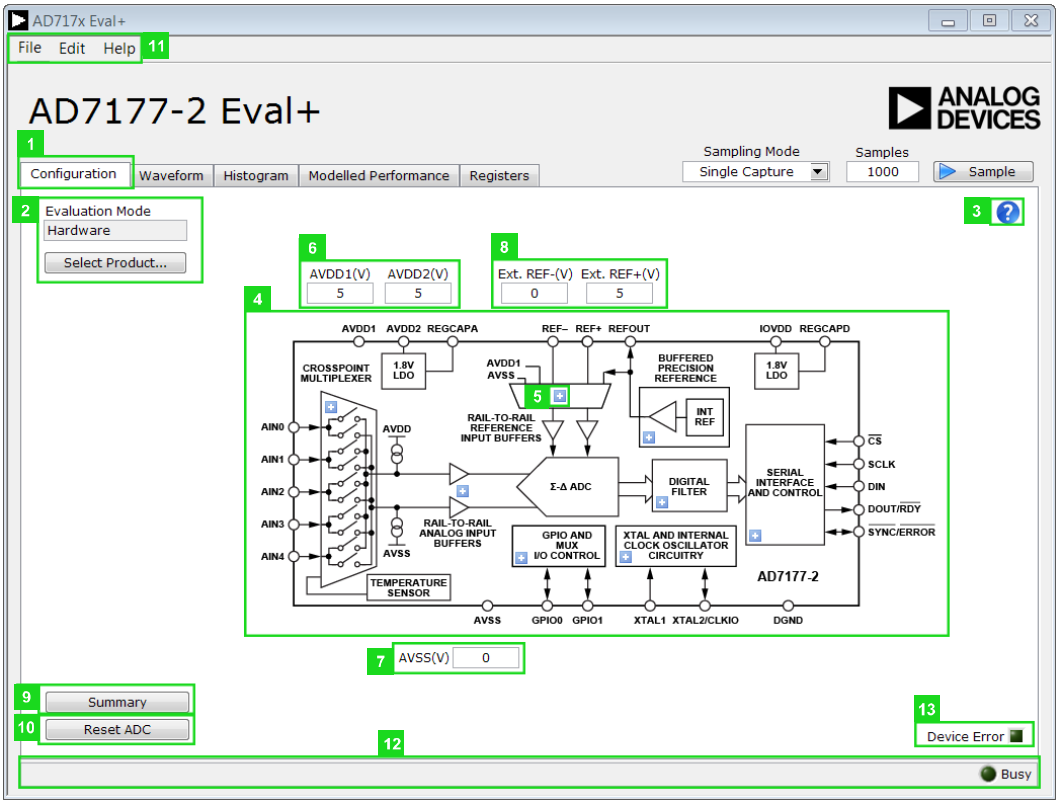

*Figure 16. **Configuration** Tab of the AD717x Eval+ Software in Hardware Mode*

OVERVIEW OF THE MAIN WINDOW

The main window of the AD717x Eval+ software displays the significant control buttons and analysis indicators of the AD717x Eval+ software. This window is divided into five tabs: **Configuration**, **Waveform, Histogram**, **Modelled Performance**, and **Registers**.

CONFIGURATION TAB

Figure 16 shows the **Configuration** (1) tab when **Hardware** mode is selected and Figure 17 shows the **Configuration** tab when **Simulation** mode is selected. The controls highlighted in Figure 17 are only available in **Simulation** mode.

Select Product/Evaluation Mode Pane

The **Evaluation Mode** (2) pane displays the evaluation mode in use. To switch between modes, click the **Select Product…** button, and the dialog box shown in Figure 13 appears.

Tutorial Icon

Click the tutorial icon (3) to open a tutorial and view additional information on using the AD717x Eval + software.

Functional Block Diagram and Configuration Pop-Up Buttons

The functional block diagram (4) of the ADC shows each of the separate functional blocks within the ADC. Click a configuration button (5) on any of the functional blocks to open the configuration pop-up window for the block selected. Not all blocks have a configuration button.

Analog and Digital Supply Voltage

The text fields labeled 6, 7, and 14 in Figure 16 and Figure 17 are input fields that are used to take the supply voltage levels selected for the AD7177-2. Checks are performed to ensure that the power supply voltage levels entered are within the specified limits. These power supply voltage levels are also used for the modelled performance to calculate the power dissipation.

External Reference

The **Ext. REF-(V)** and **Ext. REF+(V)** (8) text fields set the positive and negative external reference voltage values. The difference of these fields is used to calculate the results for both the **Waveform** and **Histogram** tabs. The evaluation board has an external 5 V ADR445 reference, which can be bypassed by removing R32. Change the external reference voltage value in the external reference text fields to ensure the correct calculation of results in the **Waveform** and **Histogram** tabs.

Register Configuration Summary

Click the **Summary** (9) button to display the selected configuration of the AD7177-2, which includes channel configuration, information on each of the individual setups, as well as, information on any error present.

Reset ADC

Click the **Reset ADC** (10) button to perform a software reset of the AD7177-2. The AD7177-2 does not have a hardware reset pin. To perform a hard reset, the power must be removed from the AD7177-2. The software reset has the same effect as a hard reset.

Menu Bar

The menu bar (11) has three sections: **File**, **Edit,** and **Help**.

File

Three options are available in the **File** menu: **Save**, **Load**, and **Exit**.

The **Save** option allows the user to save register configurations or waveform data. Register configurations can be saved as a JavaScript Object Notation (JSON) file or a header file. If the configuration is only used in the AD717x Eval+ software environment, it is recommended to use the JSON setting. Waveforms are saved as .csv files and the user is prompted to save the register configuration.

The **Load** option allows the user to load saved register configurations or waveform data. To load a header file into the AD717x Eval+ software, the file must be in the same format as the file that is saved from the AD717x Eval+ software. The header file can be used when developing firmware. When loading the waveform data, the user is prompted to load the register configuration. This step is so the software can correctly analyze the data.

Click **Exit** to close the AD717x Eval+ software.

Edit

There are two options available in the **Edit** dropdown menu, **Change Product Selection** and **Reset ADC**. The **Change Product Selection** option performs the same action as the **Select Product** button and **Reset ADC** performs the same action as the **Reset ADC** button.

Help

The **Help** dropdown menu provides links to extra information about the AD7177-2, which includes links to the product page, the evaluation board user guide, the datasheet, and the No-OS Drivers.

Selecting the AD717x Eval+ Tutorial

To open this tutorial, click the tutorial icon (3). For details on the version of the software, the **About** option opens a dialog box displaying the current version of the software and the relevant licenses.

Status Bar

The status bar (12) displays the busy indicator and status updates, such as **Analysis Completed** and **Reset Completed** during software use.

Device Error

The **Device Error** (13) LED icon illuminates when a when an ADC error is detected or when a cyclic redundancy check (CRC) error occurs. The CRC functionality on the AD7177-2 is disabled by default and must be enabled for this indicator to work. More specific information on the error can be found in the Register Configuration Summary section.

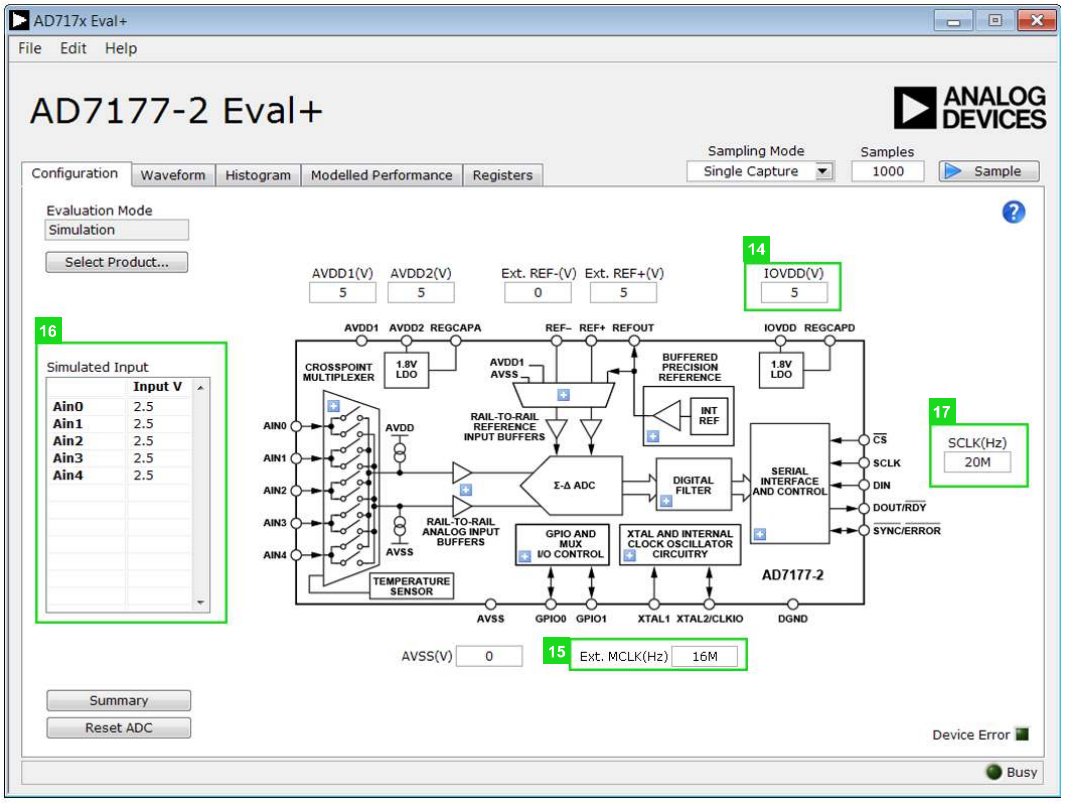

*Figure 17. **Configuration** Tab of the AD717x Eval+ Software in Simulation Mode*

External MCLK Frequency

The **Ext. MCLK(Hz)** text field (15) sets the external MCLK frequency. The **Ext. MCLK(Hz)** control is only visible in the **Configuration** tab when an external clock source is selected by the ADC. The value entered in this field is used by the functional model shown in the **Modelled Performance** tab.

Analog Input Voltage

The input fields shown in the **Simulated Input** pane (16) are only available when the AD717x Eval+ software is executed in simulation mode. These simulated inputs allow the analog input voltages to be set and can be changed at any time when the device is in simulation mode.

External SCLK Frequency

The **SCLK(Hz)** text field (17) sets the external SCLK frequency for the SPI interface. This text field is only available in simulation mode to determine if the SCLK frequency is within the permitted range.

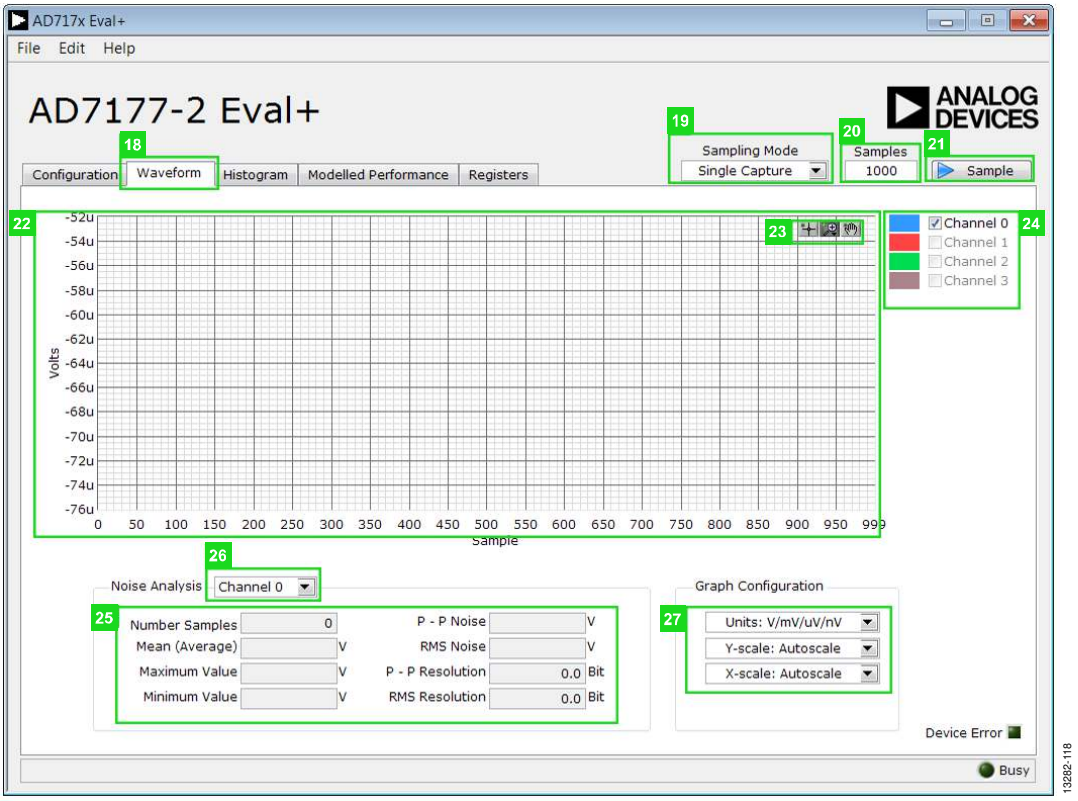

*Figure 18. **Waveform** Tab of the AD717x Eval+ Software*

WAVEFORM TAB

Figure 18 shows the **Waveform** tab (18) of the AD717x Eval+ Software.

Sampling Mode

The **Sampling Mode** control (19) is unrelated to the ADC mode. This control can be set to capture a defined sample set (single capture), or continuously gather batches of samples (repeated capture). The user can also select data logging, which runs in a similar manner to the repeated capture option; however, selecting data logging posts the results to a .csv file. When saving the results, the .csv file prompts the user to save the register configuration, which is necessary to load the analysis of the data back into the software.

Samples

The **Samples** text field (20) sets the number of samples gathered per batch. The **Single Capture** option selected from the **Sampling Mode** dropdown list returns the number of samples entered in the **Samples** text field. The **Repeated Capture** option continues to return batches of the number entered in the **Samples** text field until sampling is stopped by the user.

Sample

Click the **Sample** button (21) to start gathering ADC results. Results appear in the waveform graph (22).

Waveform Graph and Controls

The waveform graph (22) shows each successive sample of the ADC output. Zoom in on the data using the control toolbar (23). Click the x-axis and y-axis to change the scales on the graph.

Channel Selection

The channel selection control (24) allows the user to choose which channels display on the data waveform graph. These controls only affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

Noise Analysis Pane

The **Noise Analysis** pane (25) displays the results of the noise analysis for the selected analysis channel; this includes both noise and resolution measurements.

Analysis Channel

The noise analysis dropdown list (26) and histogram graph show the analysis of the channel selected.

Display Units and Axis Controls

I In the **Graph Configuration** pane (27), select the **Units: V/mV/uV/nV** dropdown menu to select the unit that the data displays in the graph. This control affects the waveform graph and the histogram graph. The axes controls can be switched between dynamic and fixed. When the dynamic control is selected, the axes automatically adjust to show the entire range of the ADC results after each batch of samples. When fixed is selected, the user can program the axes ranges. These ranges do not automatically adjust after each batch of samples.

HISTOGRAM TAB

Figure 19 shows the **Histogram** tab (28) of the AD717x Eval+ software.

Histogram Graph and Controls

The histogram graph (29) shows the number of times each sample of the ADC output occurs. The control toolbar (30) in the histogram graph allows you to zoom in on the data (see Figure 19). Click the x-axis and y-axis to change the scales on the graph.

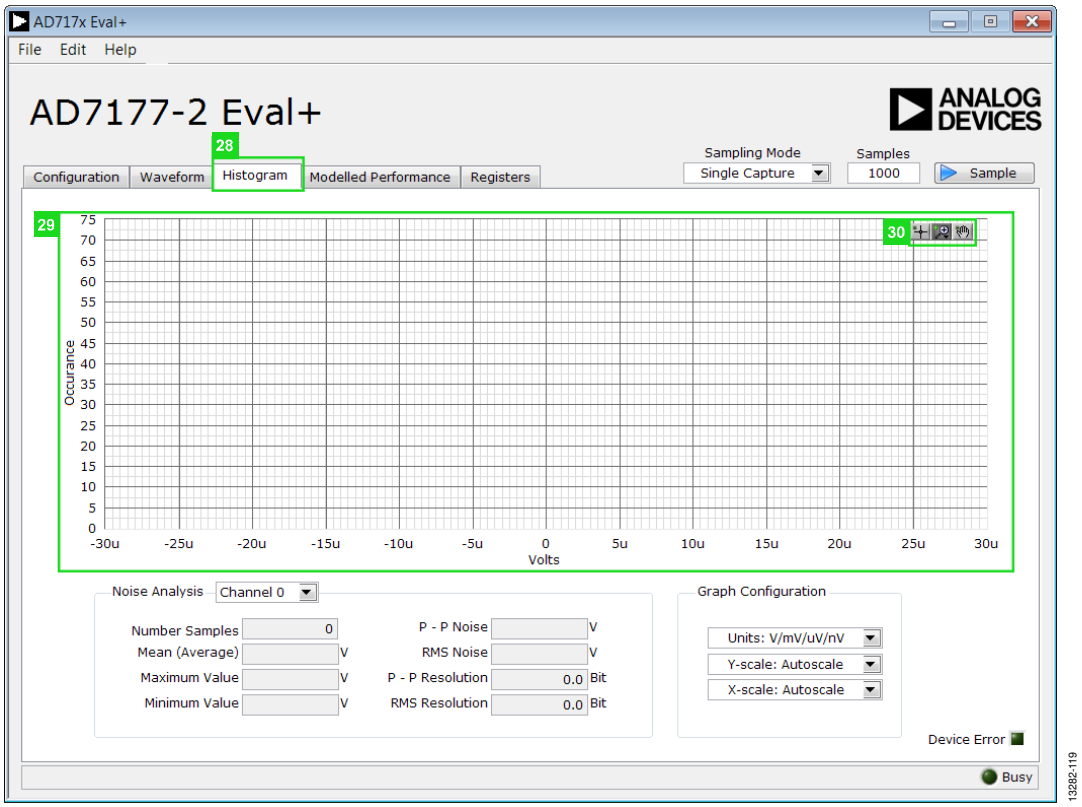

*Figure 19. **Histogram** Tab of the AD717x Eval+ Software*

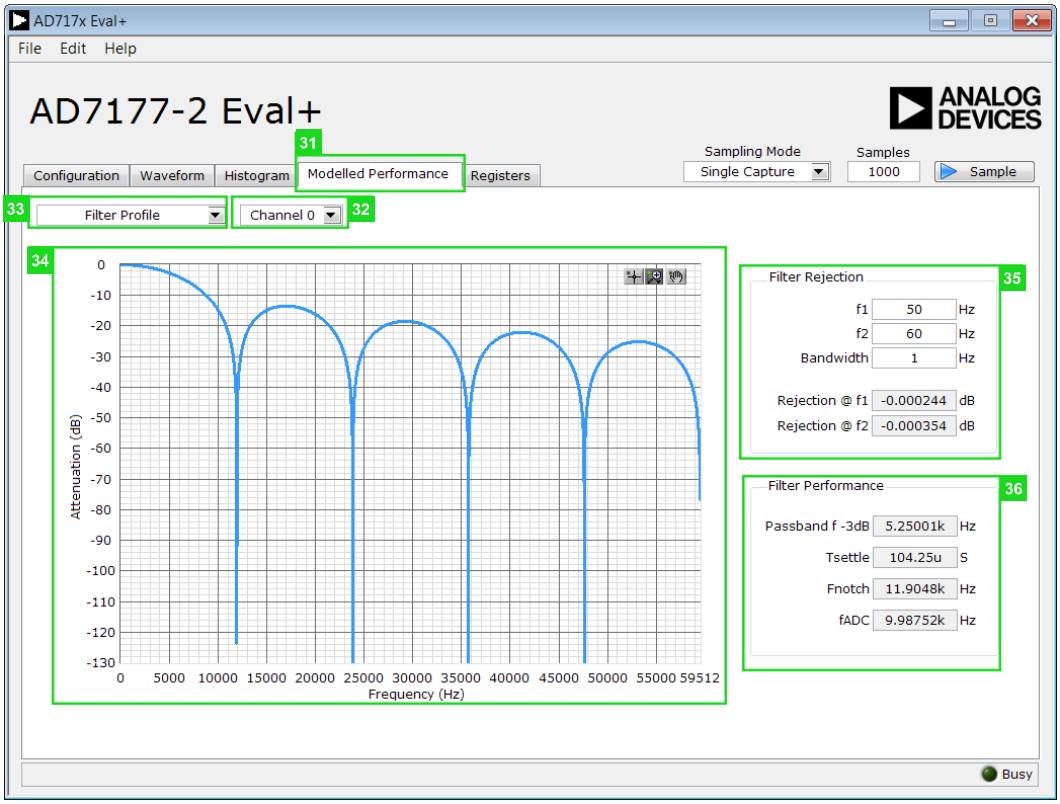

Figure 20. Filter Profiles of the AD717x Eval+ Software

MODELLED PERFORMANCE TAB

The **Modelled Performance** tab (31) shows a number of ADC performance parameters, which are calculated using the ADC functional model.

There are three main options in the **Modelled Performance** tab: **Filter Profile**, **Filter Step Response**, and **Timing Diagram/Power**. These options can be selected from the dropdown list (33). Figure 20 shows this tab when **Filter Profile** is selected.

Analysis Channel

The analysis channel dropdown list (32) selects the channel to be evaluated by the functional model.

Filter Profile Graph

This graph (34) shows the frequency response for the selected digital filter. The graph controls allows the user to zoom in on the data. Click the x-axis and y-axis to change the scales on the graph.

Filter Rejection

The **Filter Rejection** pane (35) shows the rejection/attenuation of the digital filter over the rejection bandwidth for f1 and f2 in decibels. The **f1**, **f2**, and **Bandwidth** values can be changed.

Filter Performance

The **Filter Performance** pane (36) shows timing information for the data rate of the selected output. This pane shows the ADC initial settling time (**Tsettle**), the first frequency notch (**Fnotch**), and the actual sampling frequency (**fADC**).

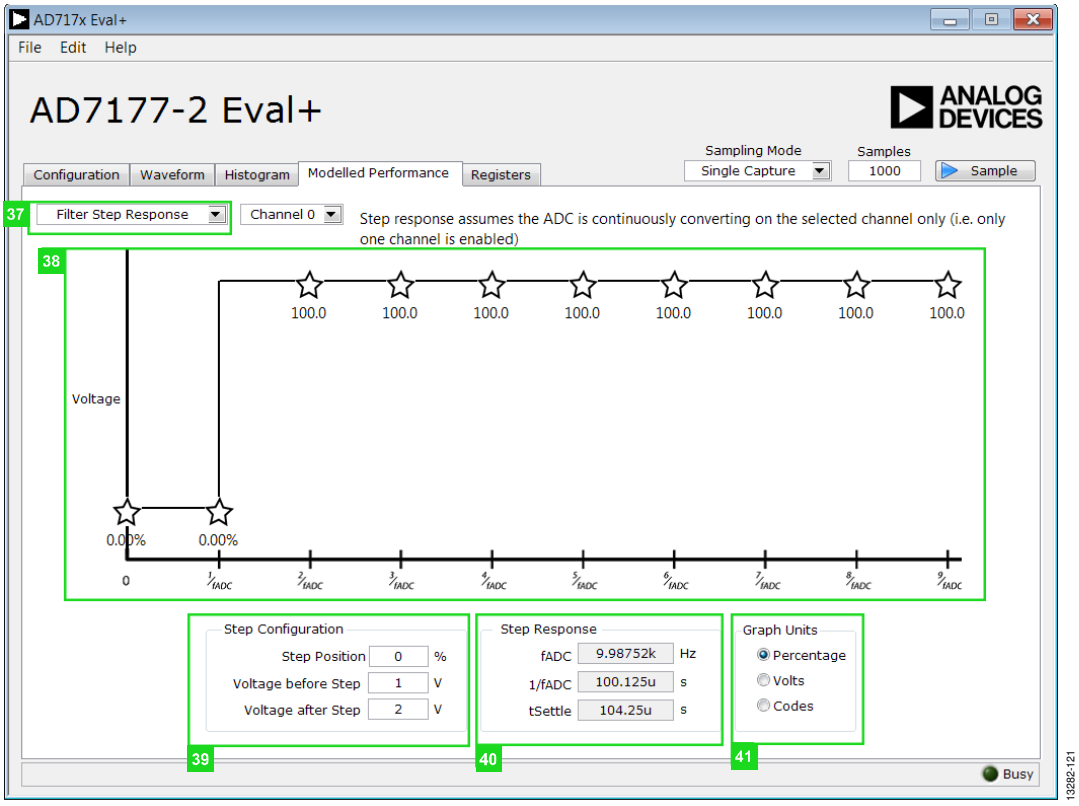

Figure 21. Filter Step Response of the AD717x Eval+ Software

Filter Step Response

The **Filter Step Response** dropdown list (37) allows the user to switch between the three sections of the **Modelled Performance** tab. Figure 21 shows this tab when **Filter Step Response** is selected from the dropdown list.

Step Response Graph

This graph (38) shows how long the filter takes to settle when the voltage is stepped from one voltage to the next. For this analysis, it is assumed the ADC is continuously converting on only one channel.

Step Configuration

The controls in the **Step Configuration** pane (39) allow the user to set the voltage before and after the step, as well as the step position. The **Step Position** text field is set as a percentage where 0% is $1/f_{ADC}$ and 100% is $2/f_{ADC}$.

Step Response

The controls in the **Step Response** pane (40) provide timing information for the data rate of the selected output. This pane shows the actual sampling frequency (**fADC**), the ADC initial settling time (**Tsettle**), and the settling time between conversions (**1/fADC**).

Graph Units

Use the controls in the **Graph Units** pane (41) to switch the step response between **Percentage**, **Volts**, and **Codes**.

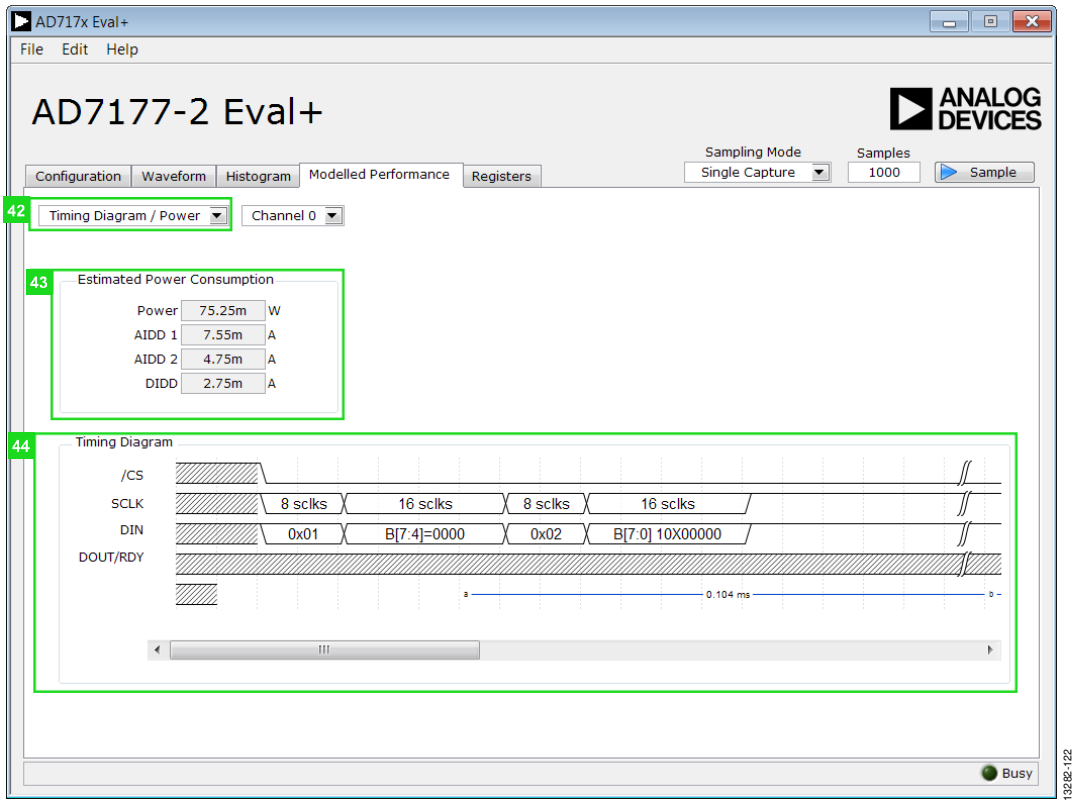

Figure 22. Timing Diagram/Power of the AD717x Eval+ Software

Timing Diagram/ Power

This dropdown list (42) allows the user to switch between the three sections of the **Modelled Performance** tab. Figure 22 shows the tab when **Timing Diagram/Power** is selected from the dropdown list.

Estimated Power Consumption

The **Estimated Power Consumption** pane (43) shows the total power consumption of the device in the selected configuration, as well as the current consumption on each of the power supply rails. Note that the estimated power consumption is for continuous conversion mode, only. No other mode of operation is supported by this control.

Timing Diagram

The graph shown in the **Timing Diagram** pane (44) shows the digital interface timing diagram for the current configuration. The graph shows the timing for the configuration of the ADC and the subsequent data reads from the ADC.

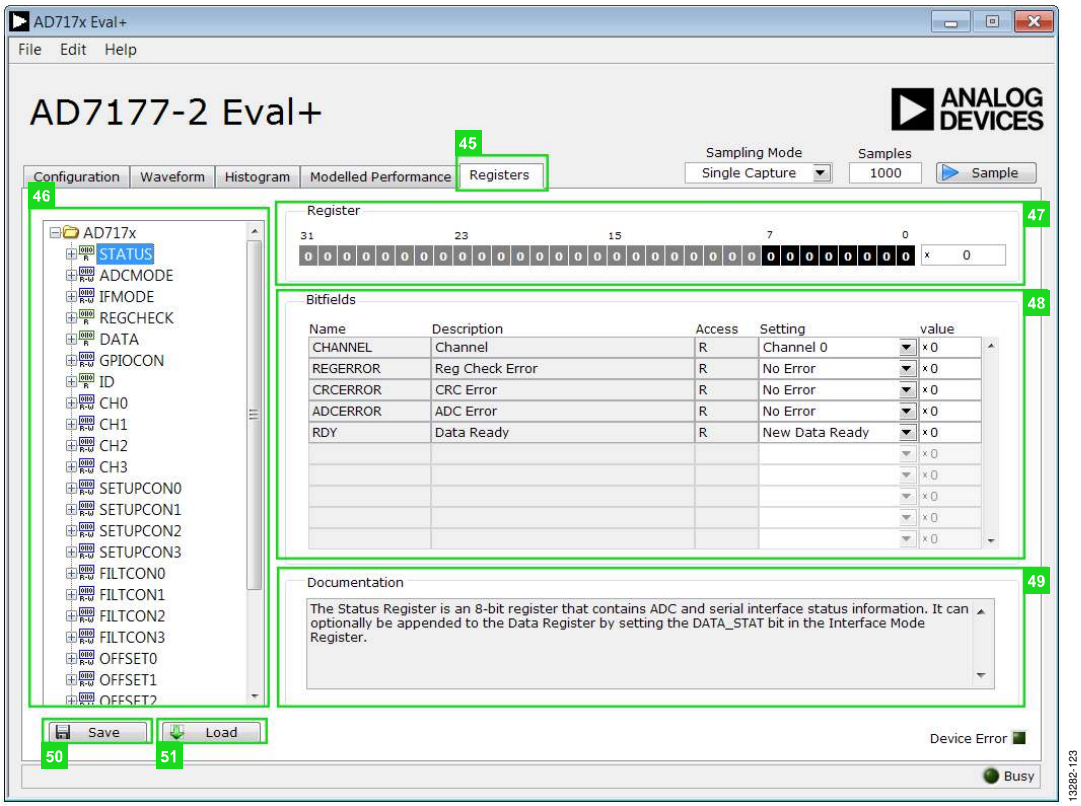

*Figure 23. **Registers** Tab of the AD717x Eval+ Software*

REGISTERS TAB

Figure 23 shows the **Registers** tab (45).

Register Tree

This register list control (46) shows the full register map in a tree control format. Each register is shown; click the expand button next to each register to show all of the bit fields contained within that register.

Register

The **Register** pane (47) allows the user to change the individual bit of the register selected in the register tree by clicking the bits or by entering the register value directly into the text field on the right side of the pane.

Bitfields

The **Bitfields** pane (48) shows the bit fields of the register selected in the register tree. Change the values in this pane by using the **Setting** dropdown lists or by directly entering a value into the **value** text fields.

Documentation

The **Documentation** pane (49) contains the documentation for the register or bit field selected in the register tree.

Save and Load

The **Save** (50) and **Load** (51) buttons allow the user to save the current configuration of the AD7177-2 by saving the register map settings to a file and loading the settings from the same file. When using these buttons, the register configurations are saved and loaded as JSON files.

EXITING THE SOFTWARE

To exit the software, click the close button at the top right corner of the AD717x Eval+ software.

EVALUATION BOARD SCHEMATICS AND ARTWORK

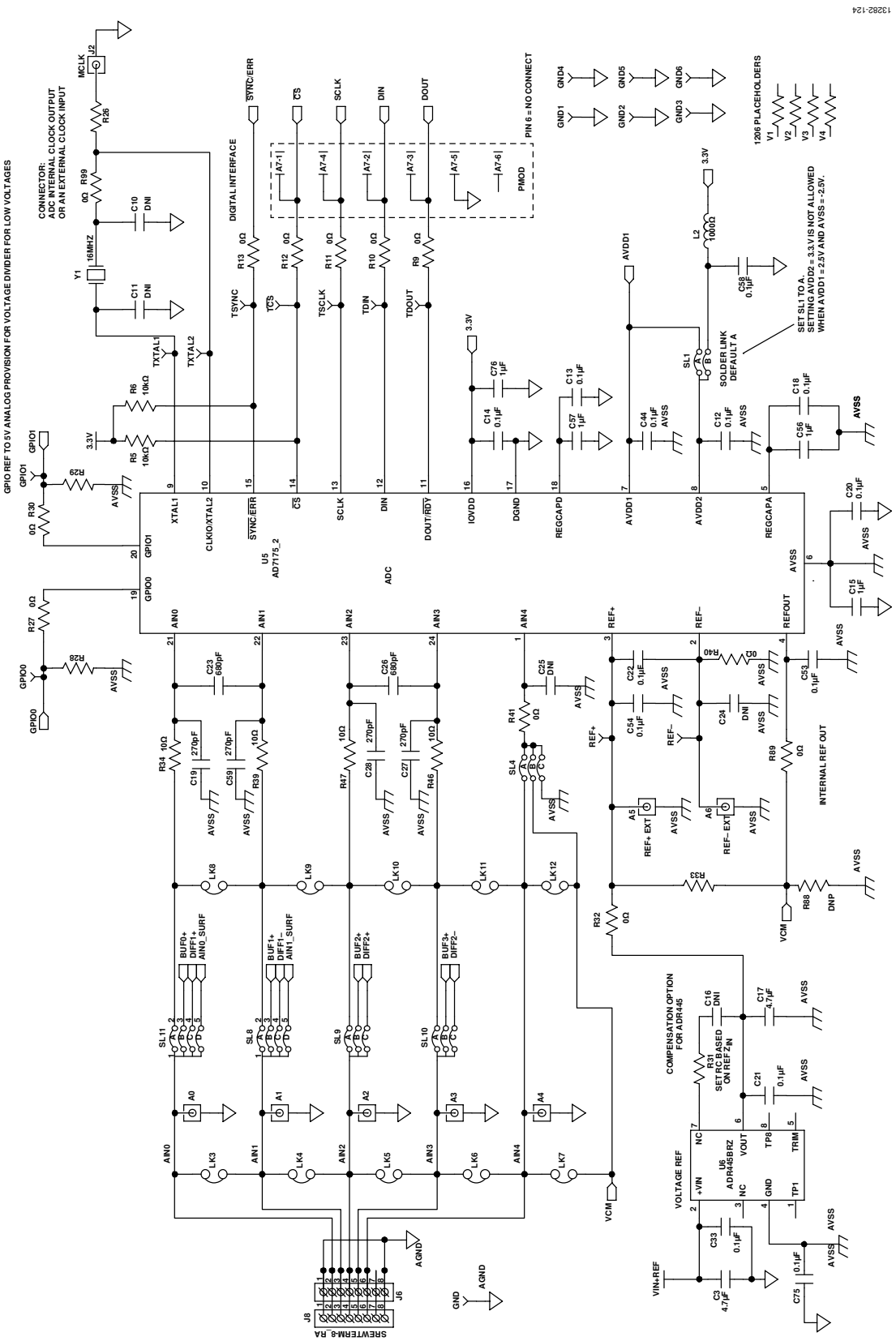

Figure 24. AD7177-2 Schematic

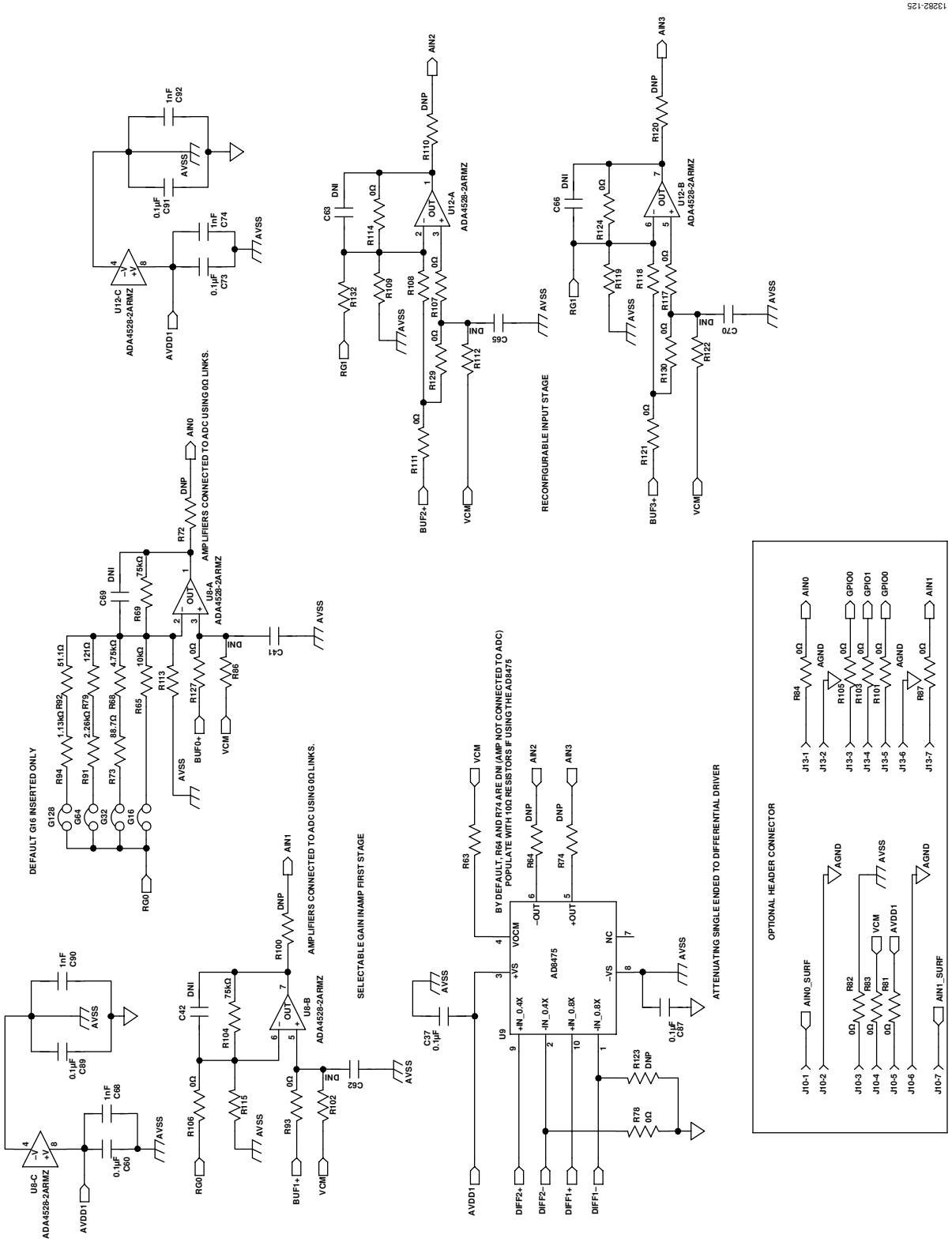

Figure 25. Amplifier Schematic

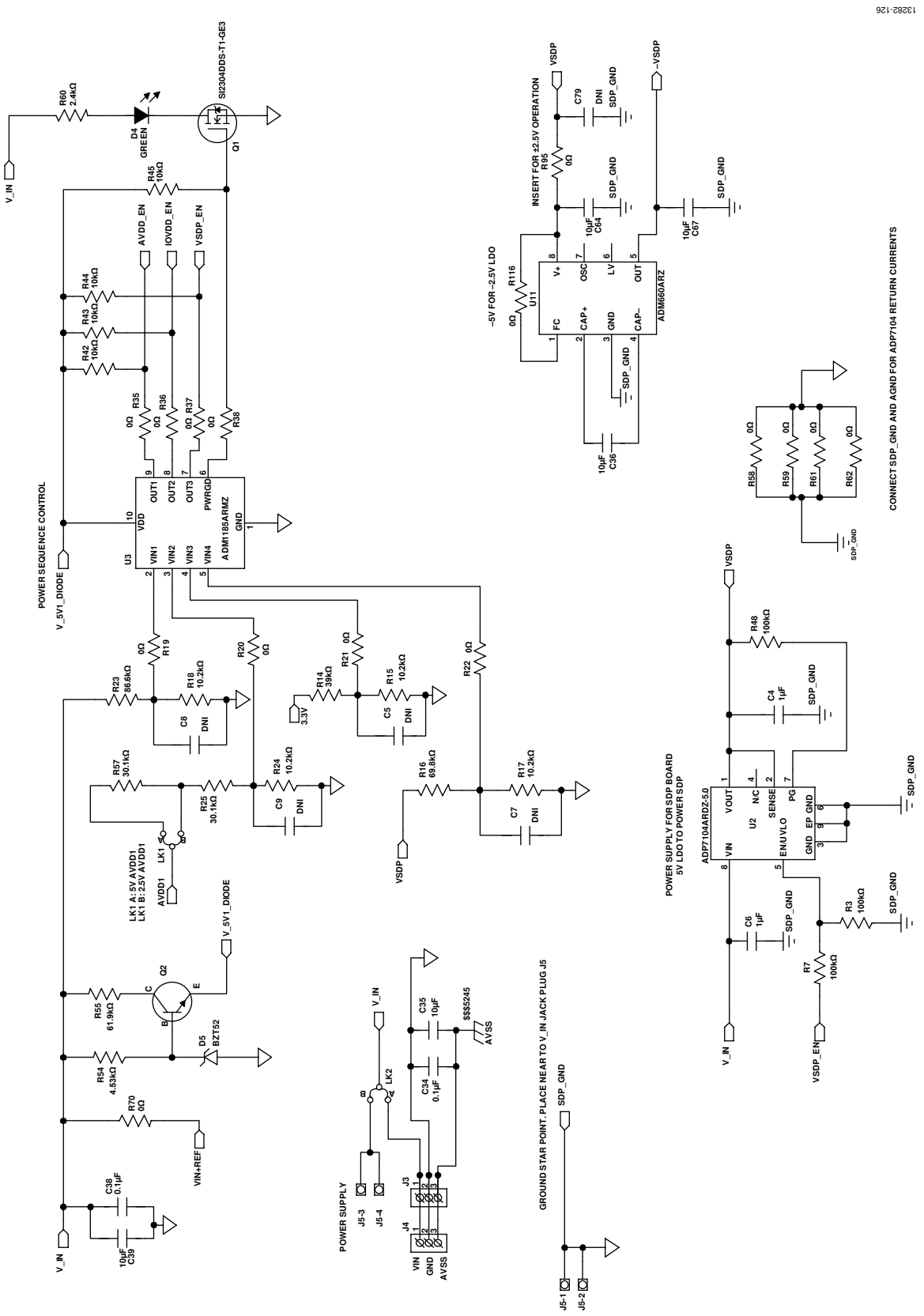

Figure 26. Power Supply Sequencing Schematic

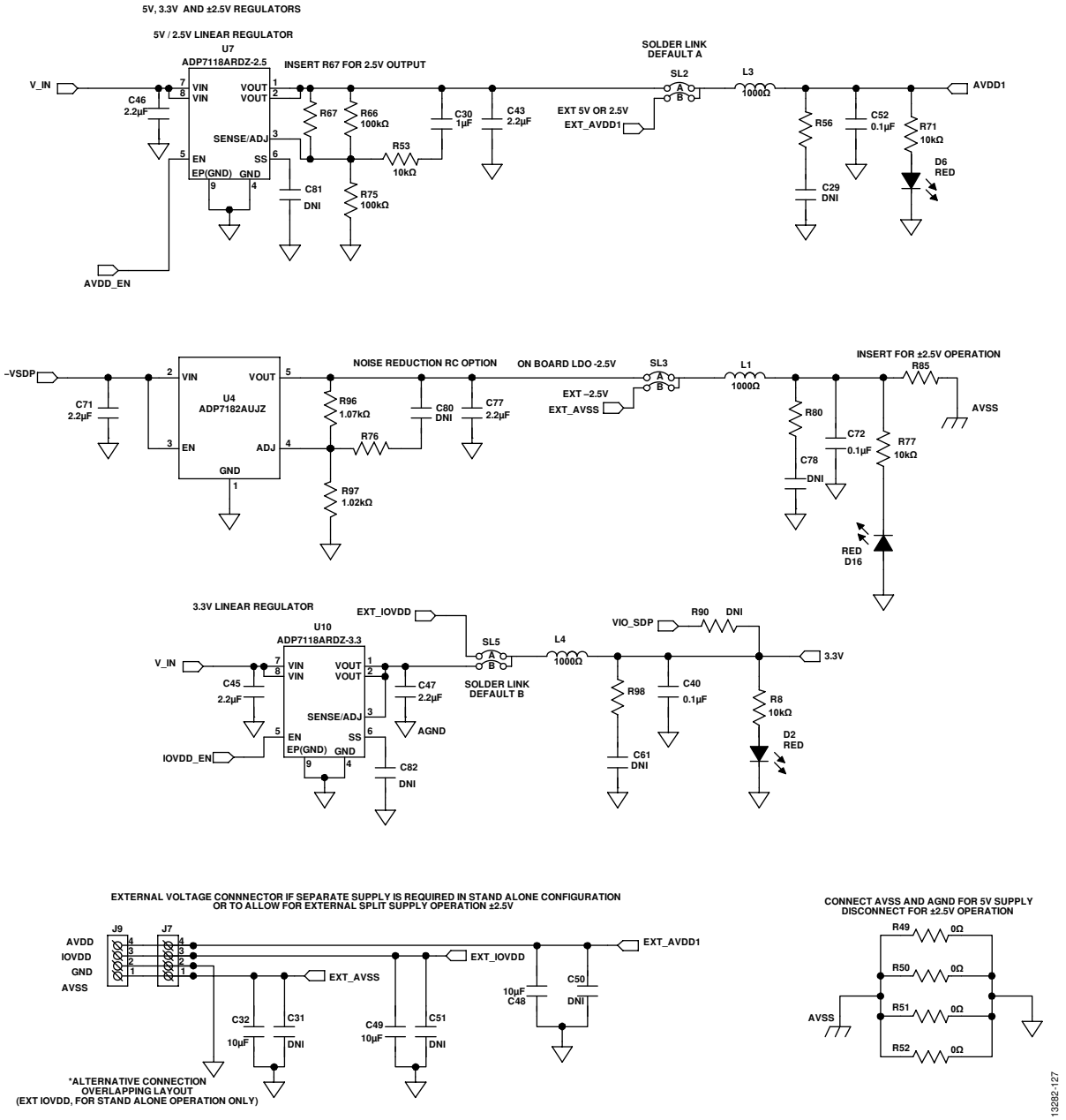

Figure 27. Regulator Schematic

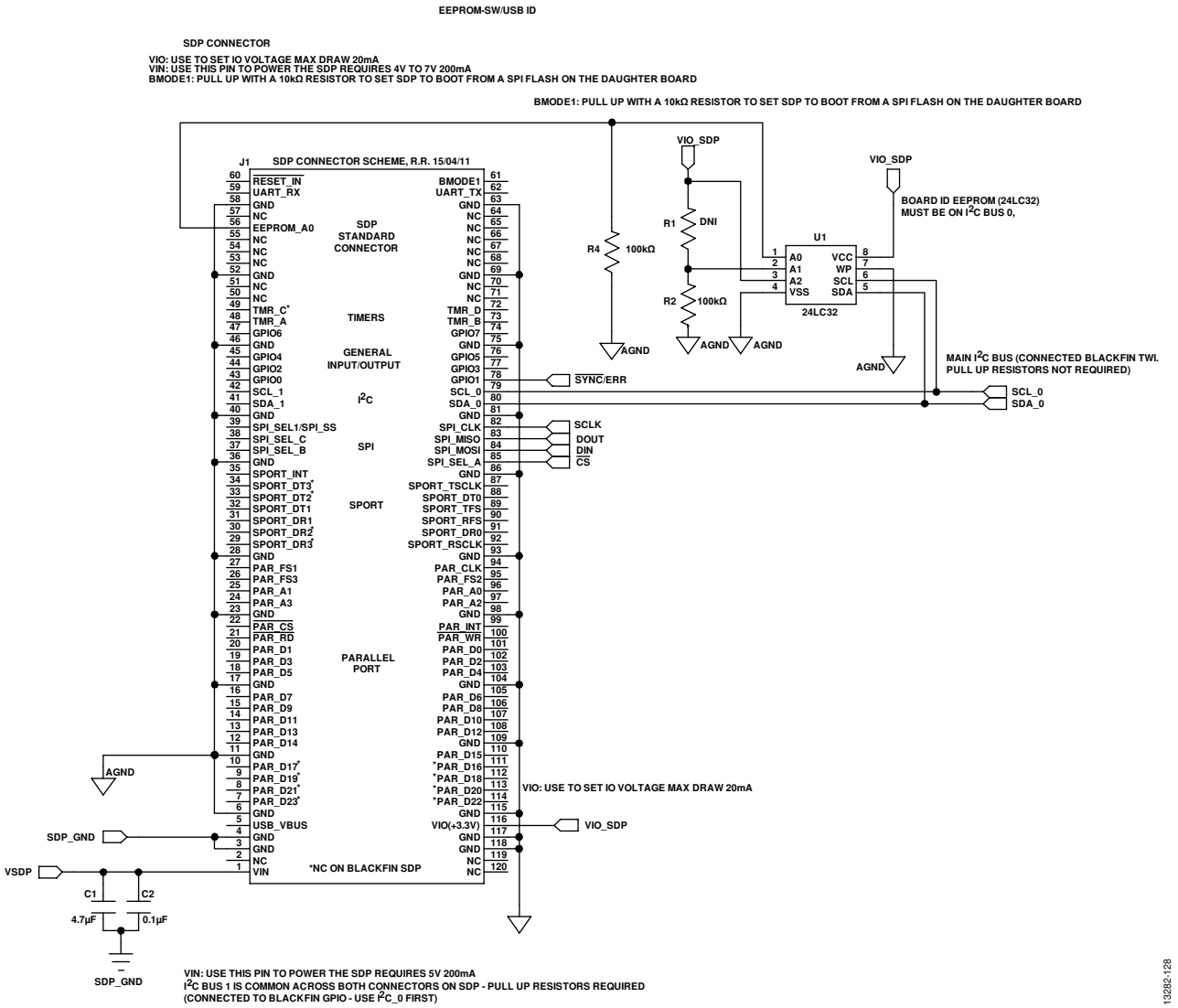

Figure 28. SDP-B Connector Schematic

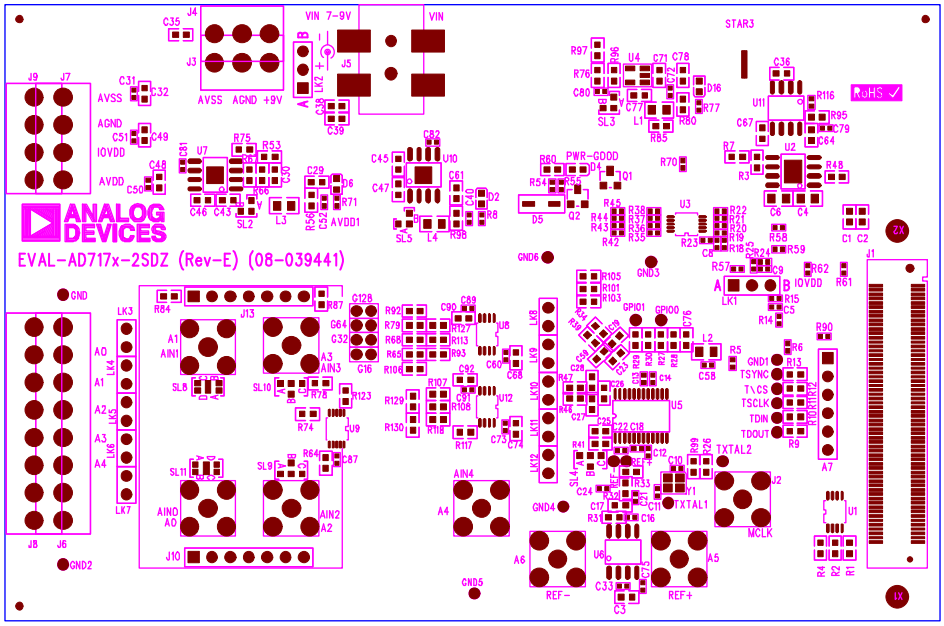

Figure 29. Top Printed Circuit Board (PCB) Silkscreen

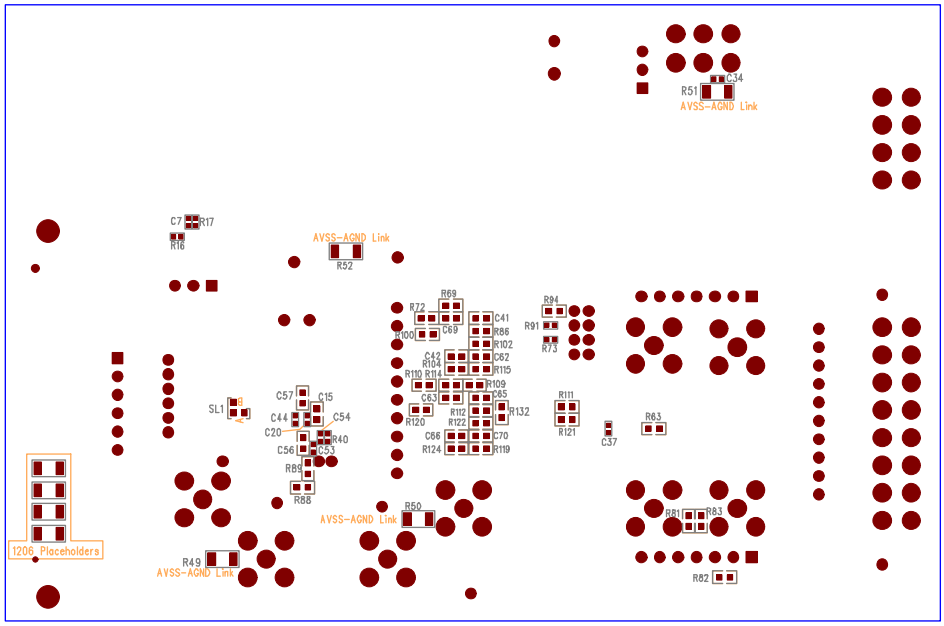

Figure 30. Bottom PCB Silkscreen

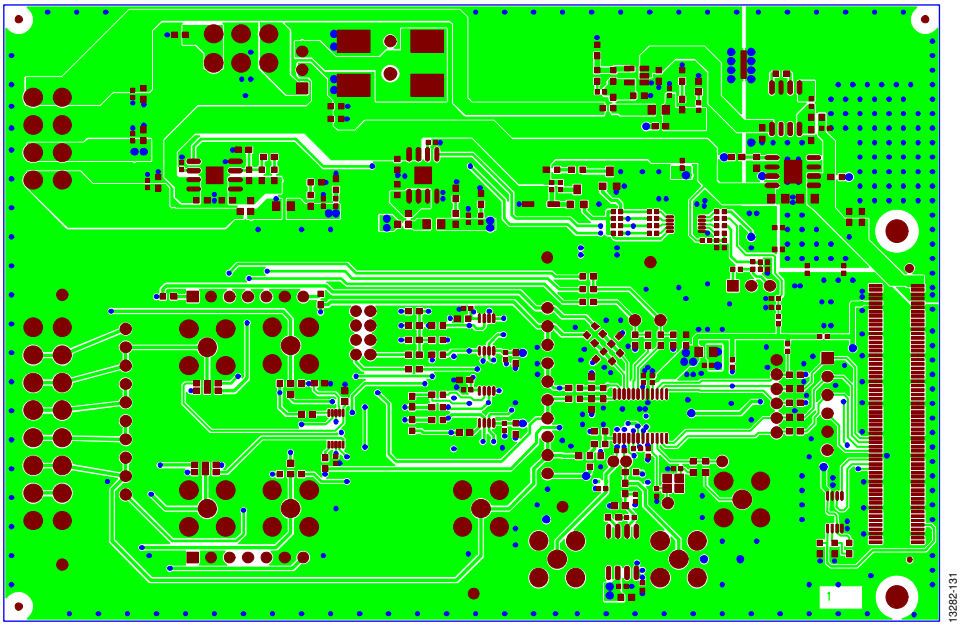

Figure 31. Layer 1, Component Side

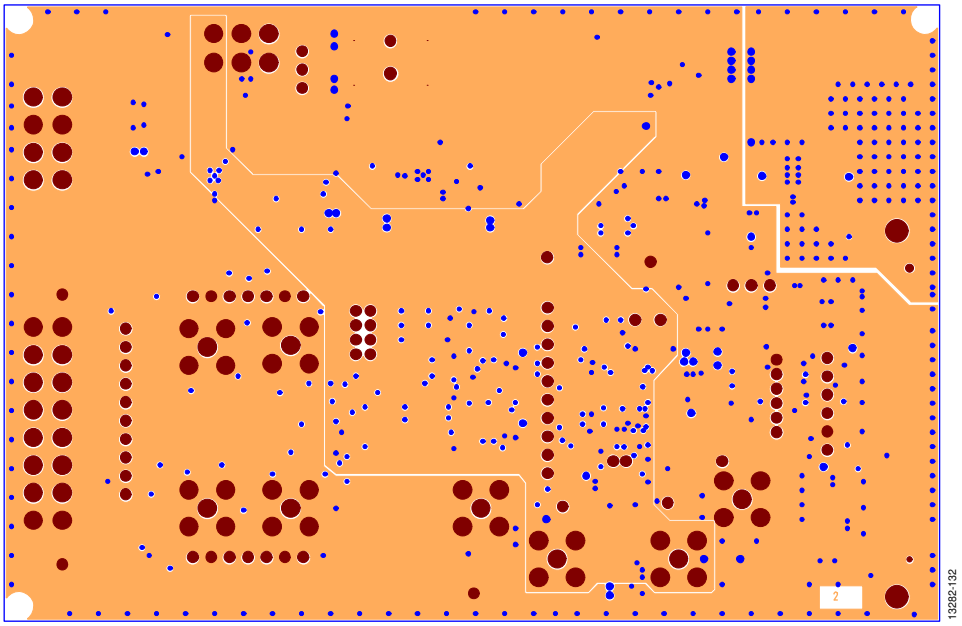

Figure 32. Layer 2, Ground Plane

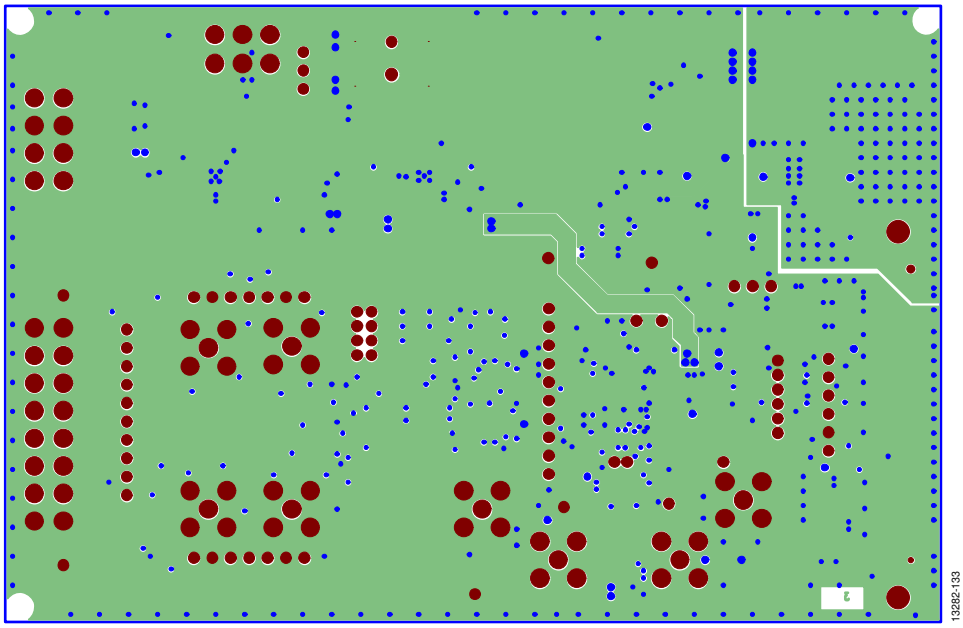

Figure 33. Layer 3, Power/Ground Plane

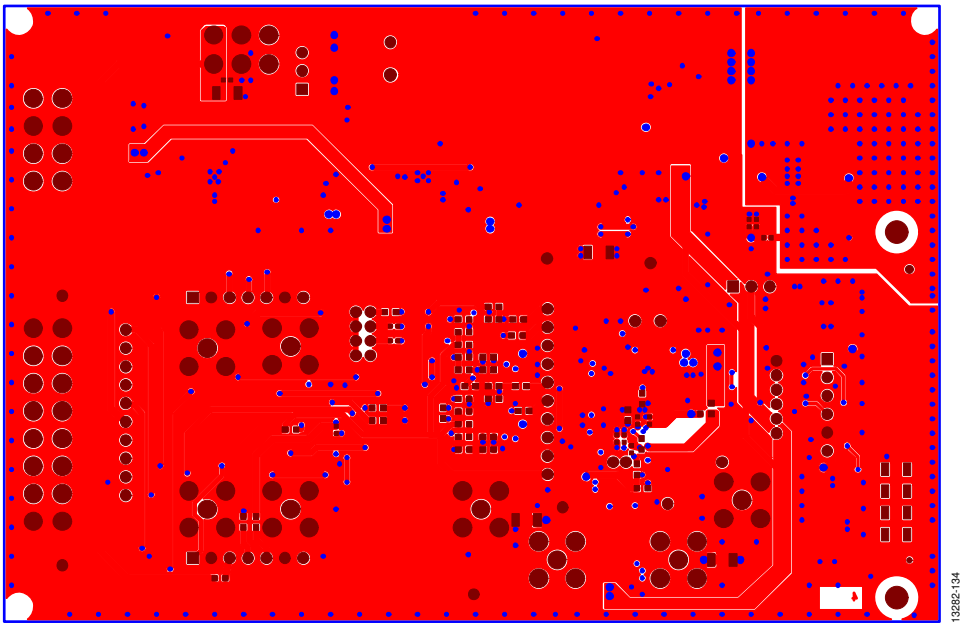

Figure 34. Layer 4, Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Qty.	Reference Designator	Description	Manufacturer	Part Number	Stock Code
5	A0 to A6	Straight PCB mount SMB jack, keep hole clear of solder, do not insert	TE Connectivity	1-1337482-0	Do not insert
1	A7	6-pin SIL header, 0.1 inch pitch	Harwin	20-9990646	FEC1022255
2	C1, C17	Ceramic capacitor, 6.3 V, X5R, 0603, 4.7 µF	Murata	GRM188R60J475K	FEC173-5527
2	C2, C38	Ceramic capacitor, 50 V, X7R, 0603, 0.1 µF	Murata	GRM188R71H104K	FEC882-0023
1	C3	Ceramic capacitor, 10 V, X5R, 0603, 4.7 µF	KEMET	C0603C475K8PACTU	FEC157-2625
2	C4, C6	Capacitor, 0805, 50 V, X7R, 1 µF	Murata	GRM21BR71H105KA12L	FEC1735541
22	C5, C7,C9, C16, C24, C25, C29, C41, C42, C61 to C63, C65, C66, C69, C70, C78 to C82	Ceramic capacitor, 0402, do not insert	Not applicable	Not applicable	
2	C10, C11	Ceramic capacitor, crystal, 0402, do not insert	Not applicable	Not applicable	
23	C12 to C14, C18, C20 to C22, C33, C34, C37, C40, C44, C52 to C54, C58, C60, C72, C73, C75, C87, C89, C91	Capacitor ceramic, 16 V, X7R, 0402	Murata	GRM155R71C104K	FEC881-9742
5	C15, C30, C56, C57, C76	Capacitor, 6.3 V, 0603, 1 µF	Murata	GRM188R70J105KA01D	FEC184-5765
8	C19, C27, C28, C55, C59, C83, C85, C86	Ceramic capacitor, 50 V, C0G/NPO, 0603	AVX Corporation	06035A271JAT2A	FEC1734627
4	C23, C26, C84, C88	Ceramic capacitor, 50 V, NPO, 0603	KEMET	C0603C681J5GACTU	FEC1414648
3	C31, C50, C51	Ceramic capacitor, 16 V, X7R, 0402, do not insert	Not applicable	Not applicable	
8	C32, C35, C36, C39, C48, C49, C64, C67	Capacitor, MLCC (multilayer ceramic capacitor) 10 V, X5R, 10 µF, 0603	TDK Corporation	C1608X5R1A106K080AC	FEC221-1164
6	C43, C45 to C47, C71, C77	Capacitor, MLCC, 10 V, X5R, 2.2 µF, 0603	Newark	MC0603X225K100CT	FEC232-0817
4	C68, C74, C90, C92	Capacitor, MLCC, 50 V, X7R	Yageo	2238 586 15623	FEC722170
3	D2, D6, D16	LED, red, high intensity (>90 mcd), 0603	Broadcom Limited	HSMC-C191	FEC855-4528
1	D4	LED, green, SMD	Osram	LGQ971	FEC1226372
1	D5	Zener diode, 0.5 W, 5.1 V	Vishay	BZT52B5V1-V-GS08	FEC1617767
1	G16	2-pin header and shorting shunt, 2 mm pitch	Harwin	M22-2010205 and M22-1920005	FEC671915 and FEC510944
3	G32, G64, G128	2-pin header, 2 mm pitch	Harwin	M22-2010205	FEC671915
19	GND, GND1 to GND6, GPIO0, GPIO1, REF+, REF−, TDIN, TDOUT, TERR, TCLK, TSYNC, TXTAL1, TXTAL2, T\CS	Test point, keep hole clear of solder, do not insert	Not applicable	Not applicable	
1	J1	120-way connector, 0.6 mm pitch	Hirose Electric Group	FX8-120S-SV(21)	FEC1324660
1	J2	Straight PCB mount, SMB jack, keep hole clear of solder, do not insert	TE Connectivity	1-1337482-0	
1	J3	Socket terminal block, 3.81 mm pitch	Phoenix Contact	MC 1.5/3-G-3.81	FEC370-4737

Qty.	Reference Designator	Description	Manufacturer	Part Number	Stock Code
1	J4	Screw terminal block, 3.81 mm pitch, do not insert	Phoenix Contact	1727023	
1	J5	DC power connectors, 2 mm pitch, SMT power jack	Lumberg	161314	FEC1243245
1	J6	8-pin terminal header, 3.81 mm pitch, vertical	Phoenix Contact	MC 1.5/8-G-3.81	FEC3704774
1	J7	Connector, 3.81 mm pitch, right angle, do not insert	Phoenix Contact	MC 1.5/4-G-3.81 and 180-3594	
1	J8	8-pin screw terminal, 3.81 mm pitch, vertical, do not insert	Phoenix Contact	1727078	
1	J9	Screw terminal block, 3.81 mm pitch	Phoenix Contact	1727036	FEC370-4592
1	J10	7-way SSW, 2.54 mm vertical socket, line up with connector on surf board	Samtec	SSW-107-01-T-S	FEC1803478
2	J11, J14	Screw terminal block, 3.81 mm pitch, do not insert	Phoenix Contact	MKDS1/4-3.81	
1	J12	4-way power socket block, 3.81 mm pitch	Phoenix Contact	MC1.5/4-G-3.81	FEC370-4749 and FEC370-4920
1	J13	7-way SIP, 2.54 mm through-hole header, line up with connector on surf board	Samtec	TLW-107-05-G-S	FEC 1668499
1	J15	4-way power socket block, 3.81 mm pitch	Phoenix Contact	MC1.5/4-G-3.81	FEC370-4749 and FEC370-4920
4	L1 to L4	Ferrite bead, 0.3 Ω at dc, 1000 Ω at 100 MHz, 350 mA, 0805	TE Connectivity	BMB2A1000LN2	FEC119-3421
2	LK1, LK2	3-pin (3 × 1) header and shorting block in, 0.1 inch pitch, Position A	Harwin	M20-9990346 and M7566-05	FEC1022249 and FEC150-411
5	LK3 to LK7	2-pin header, 0.1 inch pitch	Harwin	M20-9990246	FEC1022247
5	LK8 to LK12	2-pin header and shorting shunt, 0.1 inch pitch	Harwin	M20-9990246	FEC1022247 and FEC150-411
1	Q1	Diode, MOSFET, negative channel, 30 V, 3.6 A, SOT-23	Vishay	SI2304DDS-T1-GE3	FEC1858939
1	Q2	Transistor, NPN, SOT-23	ON Semiconductor	MMBT3904LT1G	FEC1459100
1	R1	Resistor, 0603, do not insert	Not applicable	Not applicable	
7	R2 to R4, R7, R48, R66, R75	Resistor, 100 kΩ, 0.063 W, 1%, 0603	Newark	MC0063W06031100K	FEC9330402
3	R5, R6, R77	Resistor, 10 kΩ, 0.063 W, 1%, 0402	Newark	MC00625W0402110K	FEC1358069
2	R8, R71	Resistor, 1%, 0402	Yageo	CRCW040210K0FKEAHP	FEC173-8864
31	R9 to R13, R27, R30, R32, R41, R63, R78, R81 to R84, R87, R95, R99, R101, R103, R105, R107, R111, R114, R117, R121, R124, R128 to R131	Resistor, 0603 1%, 0R	Newark	MC0063W06030R	FEC9331662
1	R14	Resistor, 0402, 1%, 39 kΩ	Newark	MC 0.0625W 0402 1% 39K	FEC1358085
4	R15, R17, R18, R24	Resistor, SMD	Newark	MC 0.0625W 0402 1% 10K2	FEC1803137
1	R16	Resistor, 0402, 1%, 69K8	Newark	MC 0.0625W 0402 1% 69K8	FEC1803735
15	R19 to R22, R35 to R38, R40, R58, R59, R61, R62, R70, R116	Resistor, 0402	Vishay	CRCW04020000Z0ED	FEC146-9661
1	R23	Resistor, 0402, 1%, 86K6	Newark	MC 0.0625W 0402 1% 86K6	FEC1803744
2	R25, R57	Resistor, 0402, 1%, 30k1	Newark	MC 0.0625W 0402 1% 30k1	FEC1803699

Qty.	Reference Designator	Description	Manufacturer	Part Number	Stock Code
32	R26, R28, R29, R31, R33, R56, R64, R67, R72, R74, R76, R80, R85, R86, R88, R98, R100, R102, R108 to R110, R112, R113, R115, R118 to R120, R122, R123, R125, R126, R132	Resistor, SMD, 0603, do not insert	Not applicable	Not applicable	
4	R34, R39, R46, R47	Resistor, 10 kΩ, 0.063 W, 1%, 0603	Newark	MC0063W0603110R	FEC9330429
4	R42 to R45	Resistor, thick film, 10 kΩ, 62.5 mW, 5%	Yageo	RC0402JR-1310KL	FEC179-9316
4	R49 to R52	Resistor, 1206	Newark	MC 0.125W 1206 0R	FEC9336974
2	R53, R65	Resistor, 10 kΩ, 0.063 W, 1%, 0603	Newark	MC0063W0603110K	FEC9330399
1	R54	Resistor, thick film, 4.53 kΩ, 63 mW, 1%	Vishay	CRCW04024K53FKED	FEC1151244
1	R55	Resistor, 0402, 1%, 61R9	Newark	MC 0.0625W 0402 1% 61R9	FEC1802915
1	R60	Resistor, thick film, 2.4 kΩ, 0603, 100 mW, 1%	Yageo	RC0603FR-072K4L	FEC1799329
1	R68	Resistor, 0603, 4K75, 0.1%, 0.1 W	Panasonic	ERA3ARB4751V	FEC209-4611
2	R69, R104	Resistor, 0603, 0.1%, 0.1 W, 75 kΩ	Panasonic	ERA3ARB753P	FEC171-7620
1	R73	Resistor, 88R7, 0.063 W, 0.1%, 0402	TE Connectivity	RN73C1E88R7B	FEC173-7900
1	R79	Resistor, 121 kΩ, 0.063 W, 0.1%, 0603	TE Connectivity	RN73C1J121RBTG	FEC114-0465
1	R90	Resistor, 0402, do not insert	Not applicable	Not applicable	
1	R91	Resistor, 2K26, 0.063 W, 0.1%, 0402	TE Connectivity	RN73C1E2K26B	FEC173-8050
1	R92	Resistor, 51R1, 0.063 W, 0.1%, 0603	TE Connectivity	RN73C1J51R1BTG	FEC114-0446
2	R93, R106	Resistor, 0603	Vishay	CRCW06030000Z0EA	FEC146-9739
1	R94	Resistor, 0603, 1K13, 0.1%, 0.1 W	Panasonic	ERA3ARB1131V	FEC209-4485
1	R96	Resistor, 1K07, 0.063 W, 1%, 0603	Newark	MC0063W060311K07	FEC1170792
1	R97	Resistor, 1K02, 0.063 W,1%, 0603	Newark	MC0063W060311K02	FEC1170789
1	R127	Resistor, 0603	Vishay	CRCW06030000Z0EA	FEC146-9739
1	SL1	2-way resistor link option	Newark	MC 0.063W 0603 0R	FEC9331662
2	SL2, SL3	2-way solder link, use 0R 0603 resistor, insert link in Position A	Not applicable		FEC933-1662
1	SL4	3-way solder link, use 0R 0603 resistor, insert link in Position C	Not applicable		FEC933-1662
1	SL5	2-way solder link, use 0R 0603 resistor, insert link in Position B	Not applicable		FEC933-1662
1	SL8	4-way solder link, use 0R 0603 resistor, insert link in Position A	Not applicable		FEC933-1662
2	SL9, SL10	3-way solder link, use 0R 0603 resistor, insert link in Position A	Not applicable		FEC933-1662
1	SL11	4-way solder link, use 0R 0603 resistor, insert link in Position A	Not applicable		FEC933-1662
1	STAR3	Ground link, copper short	Not applicable	Not applicable	Not applicable
1	U1	Serial EEPROM, 32 kΩ, I²C	Microchip	24LC32A-I/MS	FEC1331330
1	U2	Linear regulator, 5 V, 20 V, 500 mA, ultralow noise, CMOS	Analog Devices, Inc.	ADP7104ARDZ-5.0	ADP7104ARDZ-5.0
1	U3	Quad voltage monitor and sequencer	ADI	ADM1185ARMZ-1	ADM1185ARMZ-1
1	U4	Linear regulator, 8 V, −200 mA, low noise	ADI	ADP7182AUJZ	ADP7182AUJZ-R7
1	U5	ADC	ADI	AD7172-2BRUZ	AD717-2BRUZ
1	U6	Reference, 5 V, XFET	ADI	ADR445BRZ	ADR445BRZ
1	U7	Linear regulator 2.5 V, ultralow noise, CMOS	ADI	ADP7118ARDZ-2.5	ADP7118ARDZ-2.5-R7
1	U8	Dual op amp, 5.0 V, ultralow noise, zero drift, rail-to-rail input/output (RRIO)	ADI	ADA4528-2ARMZ	ADA4528-2ARMZ
1	U9	Funnel amplifier, fully differential	ADI	AD8475ARMZ	AD8475ARMZ

Qty.	Reference Designator	Description	Manufacturer	Part Number	Stock Code
1	U10	Linear regulator 3.3 V, ultralow noise, CMOS	ADI	ADP7118ARDZ-3.3	ADP7118ARDZ-3.3-R7
1	U11	Voltage converter, switched capacitor, CMOS	ADI	ADM660ARZ	ADM660ARZ
1	U12	5.0 V ultralow noise, zero-drift, RRIO, dual op-amp	ADI	ADA4528-2ARMZ	ADA4528-2ARMZ
4	V1 to V4	1206 place holder, do not insert	Not applicable	Not applicable	
1	Y1	Crystal, miniature, SMD, 16 MHz, 10 ppm, 9 pF	Epson	FA-20H	FEC 71-2814

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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