Frequency Generator with 133MHz Differential CPU Clocks

ICS932S203

Recommended Application:

Servers based on Intel CK408 processors

Output Features:

- 4 Differential CPU Clock Pairs @ 3.3V
- 7 PCI (3.3V) @ 33.3MHz
- 3 PCI_F (3.3V) @ 33.3MHz
- 1 USB (3.3V) @ 48MHz
- 1 DOT (3.3V) @ 48MHz
- 1 REF (3.3V) @ 14.318MHz
- 1 3V66 (3.3V) @ 66.6MHz
- 1 VCH/3V66 (3.3V) @ 48MHz or 66.6MHz
- 3 66MHz_OUT/3V66 (3.3V) @ 66.6MHz_IN or 66.6MHz
- 1 66MHz_IN/3V66 (3.3V) @ Input/66MHz

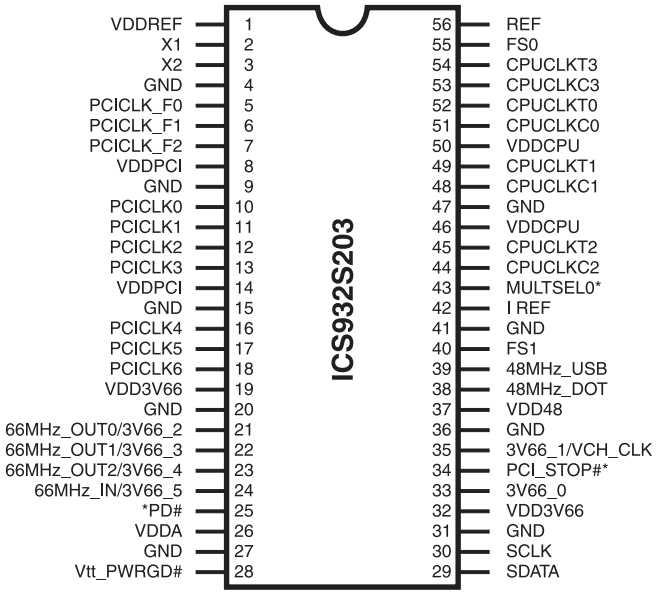
Features:

- Supports spread spectrum modulation, down spread 0 to -0.5%.
- Efficient power management scheme through PD# and PCI_STOP#.
- Uses external 14.318MHz crystal
- Stop clocks and functional control available through SMBus interface.

Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <150ps

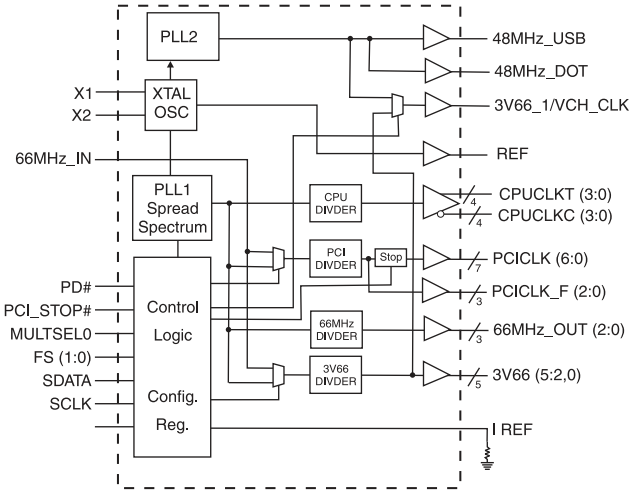
Pin Configuration



56-Pin 300mil SSOP/TSSOP

* These inputs have 150K internal pull-up resistor to VDD.

Block Diagram



Functionality

FS1	FS0	CPU (MHz)	3V66 (MHz)	66Buff[2:0] 3V66[4:2] (MHz)	PCI_F PCI (MHz)
1	0	100	66.6	66.6 In path	66.6 in/2
1	1	133.3	66.6	66. In path	66.6 in/2
0	0	100	66.6	66.6	33.3
0	1	133.3	66.6	66.6	33.3
mid	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
mid	1	Tclk/2	Tclk/4	Tclk/4	Tclk/8

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 14, 19, 26, 32, 37, 46, 50	VDD	PWR	3.3V power supply
2	X1	X2 Crystal Input	14.318MHz Crystal input
3	X2	X1 Crystal Output	14.318MHz Crystal output
7, 6, 5	PCICLK_F (2:0)	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
4, 9, 15, 20, 27, 31, 36, 41, 47	GND	PWR	Ground pins for 3.3V supply
18, 17, 16, 13, 12,11, 10	PCICLK (6:0)	OUT	PCI clock outputs
23, 22, 21	66MHz_OUT (2:0)	OUT	66MHz buffered 66MHz_OUT from 66MHz_IN input.
	3V66 (4:2)	OUT	66MHz reference clocks, from internal VCO
24	66MHz_IN	IN	66MHz input to buffered 66MHz_OUT and PCI clocks
	3V66_5	OUT	66MHz reference clock, from internal VCO
25	PD#	IN	Invokes power-down mode. Active Low.
28	Vtt_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS[0:2] and MULTISEL0 inputs are valid and are ready to be sampled (active low)
29	SDATA	I/O	Data pin for SMBus circuitry 5V tolerant
30	SCLK	IN	Clock pin of SMBus circuitry 5V tolerant
33	3V66_0	OUT	66MHz reference clocks, from internal VCO
34	PCI_STOP#	IN	Halts PCICLK clocks at logic 0 level, when input low except PCICLK_F which are free running
35	3V66_1/VCH_CLK	OUT	3.3V output selectable through I^2C to be 66MHz from internal VCO or 48MHz (non-SSC)
38	48MHz_DOT	OUT	48MHz output clock for DOT
39	48MHz_USB	OUT	48MHz output clock for USB
40, 55	FS (1:0)	IN	Special 3.3V input for Mode selection
42	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
43	MULTSEL0	IN	MULTSEL0 input is sensed on power-up and then internally latched prior to the pin being used for output on 3V 14.318MHz clocks.
44, 48, 51, 53	CPUCLKC (3:0)	OUT	"Complementary" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
45, 49, 52, 54	CPUCLKT (3:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
56	REF	OUT	14.318MHz reference clock.

Power Groups

(Analog)
VDDA = PLL1
VDD48 = 48MHz, PLL
VDDREF = VDD for Xtal, POR

(Digital)
VDDPCI
VDD3V66
VDDCPU

Frequency Select Table

FS1	FS0	CPU	3V66 (1:0)	66Buff (2:0) / 3V66 (4:2)	66 In / 3V66_5	PCI	REF	USB, DOT	note
1	0	100	66.6	66.6 In path	66.6 IN	66.6 in/2	14.318	48	Buffer mode 66
1	1	133.3	66.6	66.6 In path	66.6 IN	66.6 in/2	14.318	48	Buffer mode 66
0	0	100	66.6	66.6	66.6	33.3	14.318	48	Driven 66
0	1	133.3	66.6	66.6	66.6	33.3	14.318	48	Driven 66
mid[1]	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Tri-state outputs
mid[1]	1	Tclk/2	Tclk/4	Tclk/4	Tclk/4	Tclk/8	Tclk	Tclk/2	Tclk is at X1 input

1. Low=Vin < 0.8V, Mid=1.0V < Vin < 1.8V, High=Vin > 2.0V

Host Swing Select Functions

MULTISEL0	Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3*Rr)	Output Current	Voh @ Z
0	50 ohms	Rr = 221 1%, Iref = 5.00mA	Ioh = 4* I REF	1.0V @ 50
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6* I REF	0.7V @ 50

Byte 0: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	-		1		(Reserved)
Bit 1	55	FS0	X	R	Reflects the value of FS0 pin sampled on power up
Bit 2	40	FS1	X	R	Reflects the value of FS1 pin sampled on power up
Bit 3	34	PCI_STOP#[3]	X	R	Hardware mode: Reflects the value of PCI_STOP# pin sampled on PWD
Bit 4	-		1		(Reserved)
Bit 5	35	3V66_1/VCH	0	RW	VCH Select 66MHz/48MHz 0=66MHz, 1=48MHz
Bit 6	-		0		(Reserved)
Bit 7	-	Spread Enabled	0	RW	0=Spread Off, 1=Spread On

Byte 1: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	52, 51	CPUCLKT0 CPUCLKC0	1	RW	0=Disabled 1=Enabled
Bit 1	49, 48	CPUCLKT1 CPUCLKC1	1	RW	0=Disabled 1=Enabled
Bit 2	45, 44	CPUCLKT2 CPUCLKC2	1	RW	0=Disabled 1=Enabled
Bit 3	52, 51		0	-	Reserved
Bit 4	49, 48		0	-	Reserved
Bit 5	45, 44		0	-	Reserved
Bit 6	53, 54	CPUCLKT3 CPUCLKC3	1	RW	0=Disabled 1=Enabled
Bit 7	43	MULTSEL0	X	R	Reflects the current value of MULTSEL0

Notes:

1. R= Read only RW= Read and Write
2. PWD = Power on Default
3. The purpose of this bit is to allow a system designer to implement PCI_STOP functionality in one of two ways. Wither the system designer can choose to use the externally provided PCI_STOP# pin to assert and de-assert PCI_STOP functionality via SMBus Byte 0 Bit 3.

   In Hardware mode it is not allowed to write to the SMBus Byte 0 Bit3. In Software mode it is not allowed to pull the external PCI_STOP pin low. This avoids the issues related with Hardware started and software stopped PCI_STOP conditions. The clock chip is to be operated in the Hardware or Software PCI_STOP mode ONLY, it is not allowed to mix these modes.

   In Hardware mode the SMBus byte 0 Bit 3 is R/W and should reflect the status of the part. Whether or not the chip is in PCI_STOP mode.

   Functionality PCI_STOP mode should be entered when [(PCI_STOP#=0) or (SMBus Byte 0 Bit 3 = 0)].

Byte 2: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	10	PCICLK0	1	RW	0=Disabled 1=Enabled
Bit 1	11	PCICLK1	1	RW	0=Disabled 1=Enabled
Bit 2	12	PCICLK2	1	RW	0=Disabled 1=Enabled
Bit 3	13	PCICLK3	1	RW	0=Disabled 1=Enabled
Bit 4	16	PCICLK4	1	RW	0=Disabled 1=Enabled
Bit 5	17	PCICLK5	1	RW	0=Disabled 1=Enabled
Bit 6	18	PCICLK6	1	RW	0=Disabled 1=Enabled
Bit 7	-	-	0	-	(Reserved)

Byte 3: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	5	PCICLK_F0	1	RW	0=Disabled 1=Enabled
Bit 1	6	PCICLK_F1	1	RW	0=Disabled 1=Enabled
Bit 2	7	PCICLK_F2	1	RW	0=Disabled 1=Enabled
Bit 3	5	PCICLK_F0	0	RW	Allow control of PCICLK_F0 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 4	6	PCICLK_F1	0	RW	Allow control of PCICLK_F1 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 5	7	PCICLK_F2	0	RW	Allow control of PCICLK_F2 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 6	39	48MHz_USB	1	RW	0=Disabled 1=Enabled
Bit 7	38	48MHz_DOT	1	RW	0=Disabled 1=Enabled

Byte 4: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	21	66MHz_OUT0/3V66-2	1	RW	0=Disabled 1=Enabled
Bit 1	22	66MHz_OUT0/3V66-3	1	RW	0=Disabled 1=Enabled
Bit 2	23	66MHz_OUT0/3V66-4	1	RW	0=Disabled 1=Enabled
Bit 3	24	3V66_5	1	RW	0=Disabled 1=Enabled
Bit 4	35	3V66_1/VCH_CLK	1	RW	0=Disabled 1=Enabled
Bit 5	33	3V66_0	1	RW	0=Disabled 1=Enabled
Bit 6	-	-	0	R	(Reserved)
Bit 7	-	-	0	R	(Reserved)

Notes:

1. R= Read only RW= Read and Write
2. PWD = Power on Default

Byte 5: Programming Edge Rate
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Type	Description
Bit 0	X	48MHz_USB	0	RW	USB edge rate cntrol
Bit 1	X	48MHz_USB	0	RW	USB edge rate cntrol
Bit 2	X	48MHz_DOT	0	RW	DOT edge rate control
Bit 3	X	48MHz_DOT	0	RW	DOT edge rate control
Bit 4	X	-	0	-	(Reserved)
Bit 5	X	-	0	-	(Reserved)
Bit 6	X	-	0	-	(Reserved)
Bit 7	X	-	0	-	(Reserved)

Byte 6: Vendor ID Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Type	Description
Bit 0	X	Vendor ID Bit0	1	R	(Reserved)
Bit 1	X	Vendor ID Bit1	0	R	(Reserved)
Bit 2	X	Vendor ID Bit2	0	R	(Reserved)
Bit 3	X	Vendor ID Bit3	0	R	(Reserved)
Bit 4	X	Revision ID Bit0	X	R	Revision ID values will be based on individual device's revision
Bit 5	X	Revision ID Bit1	X	R	
Bit 6	X	Revision ID Bit2	X	R	
Bit 7	X	Revision ID Bit3	X	R	

Notes:
1. R= Read only RW= Read and Write
2. PWD = Power on Default

Absolute Maximum Ratings

Supply Voltage	5.5 V
Logic Inputs	GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature	0°C to +70°C
Case Temperature	115°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load; Select @ 100 MHz	229	230	360	mA
	$I_{DD3.3OP}$	C_L =Full load; Select @ 133 MHz	220	233	360	mA
Powerdown Current	$I_{DD3.3PD}$				60	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	770	850	mV	1
Voltage Low	VLow		-150	5	150		1
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		756	1150	mV	1
Min Voltage	Vuds		-300	-7			1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		5.4000	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	200MHz nominal	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	332	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	344	700	ps	1
Rise Time Variation	d-t_r			30	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	49	55	%	1
Skew	t_{sk3}	V_T = 50%		8	100	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom		60	150	ps	1

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - PCICLK Un-Buffered Mode

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.32	0.5to 2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.39	0.5 to 2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		247	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		111	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK Buffered Mode

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.29	0.5to 2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.32	0.5 to 2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.9	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		209	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		107	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66 -Un-Buffered Mode: 3V66 [5:0]

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.38	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.45	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	54.4	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		90	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66		128	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics- 3V66 - Buffered Mode: 3V66 [1:0] 66MHz_OUT [2:0]

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	W
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.44	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.36	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	54.6	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V 3V66 [1:0]		105	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66 [1:0]		121	300	ps
Skew	t_{sk1}[1]	V_T = 1.5 V 66MHz_OUT [2:0]		169	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 66MHz_OUT [2:0]		89	300	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			48		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.6	1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.8	1	ns
VCH 48 USB Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.2	2	ns
VCH 48 USB Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.3	2	ns
48 DOT Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.8	55	%
VCH 48 USB Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53.5	55	%
48 DOT Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		183	350	ps
VCH Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		223	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.25	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.15	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		723	1000	ps

[1]Guaranteed by design, not 100% tested in production.

General SMBus serial interface information

The information in this section assumes familiarity with SMBus programming.
For more information, contact ICS for an SMBus software program.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

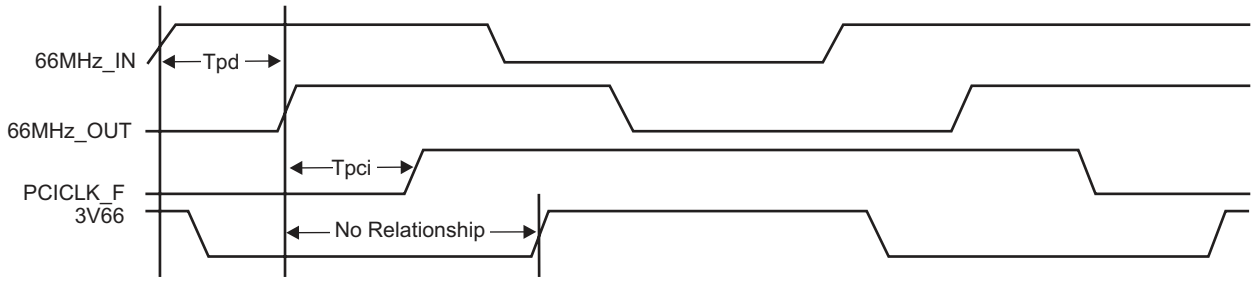
Notes:

1. The ICS clock generator is a slave/receiver, SMBus component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator SMBus interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Buffered Mode - 3V66[0:1], 66MHz_IN, 66MHz_OUT[0:2] and PCI Phase Relationship

All 3V66 clocks are to be in phase with each other. All 66MHz_OUT clocks are to be in phase with each other. There is NO phase relationship between the 3V66 clocks and the 66MHz_OUT and PCI clocks. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1/VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.

The 66MHz_IN to 66MHz_OUT delay is shown in the figure below and is specified to be within a min and max propagation value.



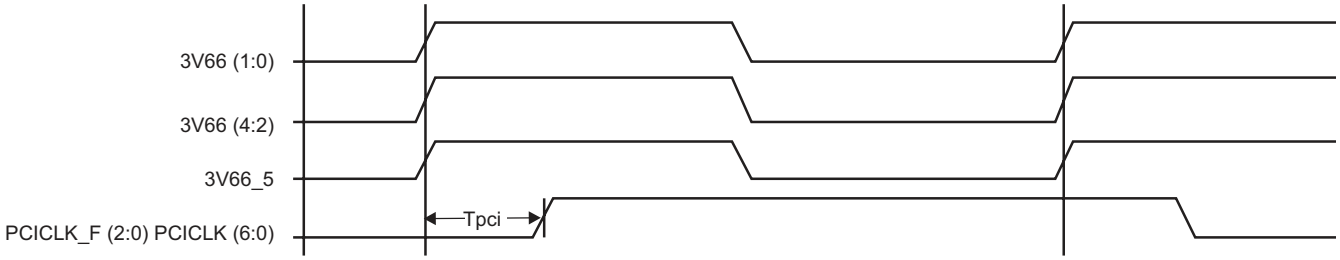
Group Skews at Common Transition Edges: (Buffered Mode)

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66	3V66	3V66 (1:0) pin to pin skew	0		500	ps
66MHz_OUT	66OUT	66MHz_OUT (2:0) pin to pin skew	0		175	ps
PCI	PCI	PCI_F (2:0) and PCI (6:0) pin to pin skew	0		500	ps
66MHz_IN 66MHz_OUT	Tpd	Propogation delay from 66MHz_IN to 66MHz_OUT (2:0)	2.5		4.5	ns
66MHz_OUT to PCI	Tpci	66MHz_OUT (2:0) leads 33 MHz PCI	1.5		3.5	ns

[1]Guaranteed by design, not 100% tested in production.

Un-Buffered Mode 3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1/VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Group Skews at Common Transition Edges: (Un-Buffered Mode)

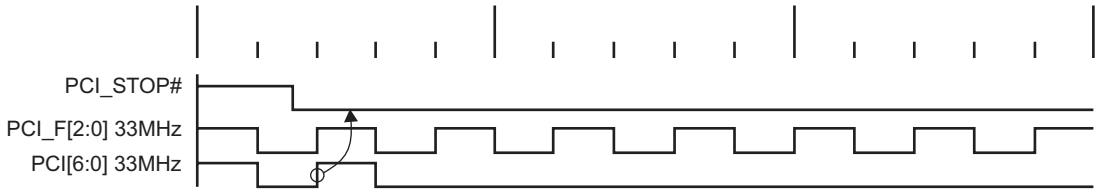
GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66	3V66	3V66 (5:0) pin to pin skew	0		500	ps
PCI	PCI	PCI_F (2:0) and PCI (6:0) pin to pin skew	0		500	ps
3V66 to PCI	$S_{3V66\text{-}PCI}$	3V66 (5:0) leads 33MHz PCI	1.5		3.5	ns

[1]Guaranteed by design, not 100% tested in production.

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[6:0] and stoppable PCI_F[2,0] clocks will latch low in their next high to low transition.

Assertion of PCI_STOP# Waveforms

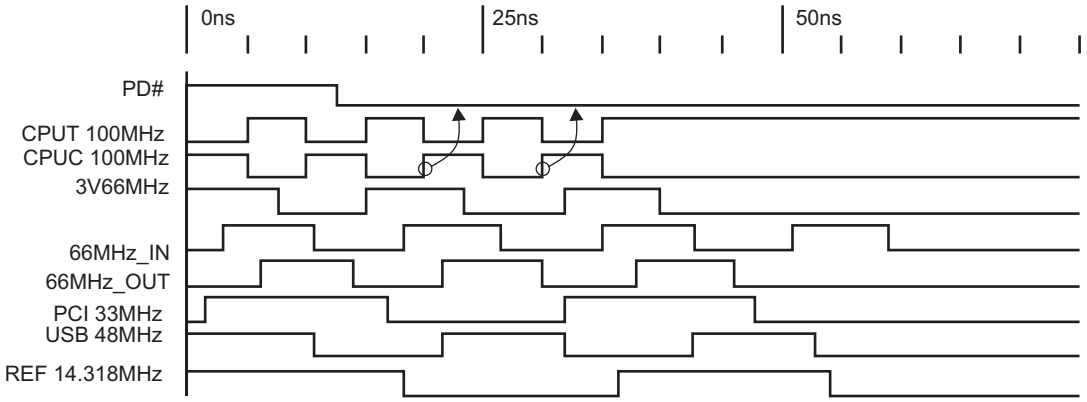


PD# - Assertion (transition from logic "1" to logic "0")

When PD# is sampled low by two consecutive rising edges of CPU clock then all clock outputs except CPU clocks must be held low on their next high to low transition. CPU clocks must be held with the CPU clock pin driven high with a value of 2x Iref, and CPUC undriven. Note the example below shows CPU = 100MHz, this diagram and description is applicable for all valid CPU frequencies 66, 100, 133, 200MHz.

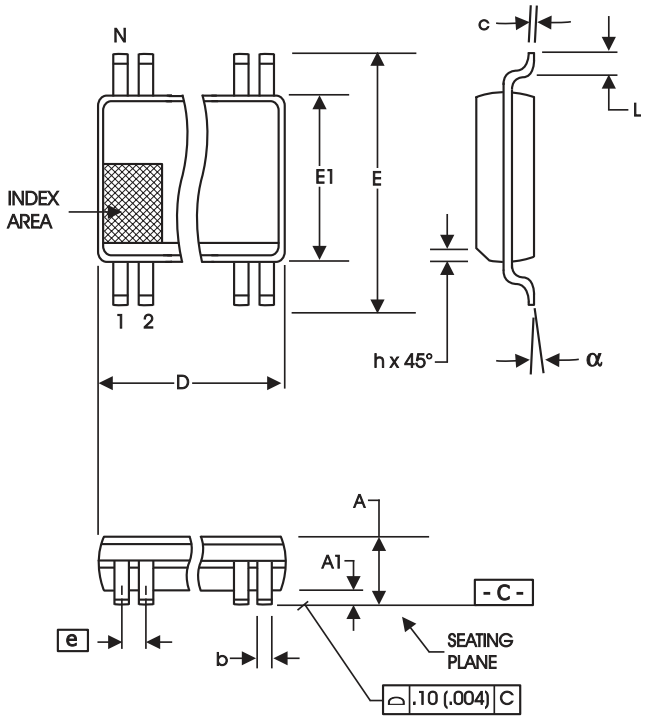
Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power Down Assertion of Waveforms - Buffered Mode



PD# Functionality

CPU_STOP#	CPUT	CPUC	3V66	66MHz_OUT	PCICLK_F PCICLK	PCICLK	USB/DOT 48MHz
1	Normal	Normal	66MHz	66MHz_IN	66MHz_IN	66MHz_IN	48MHz
0	iref * Mult	Float	Low	Low	Low	Low	Low



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.288	18.542	.720	.730

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300 mil SSOP

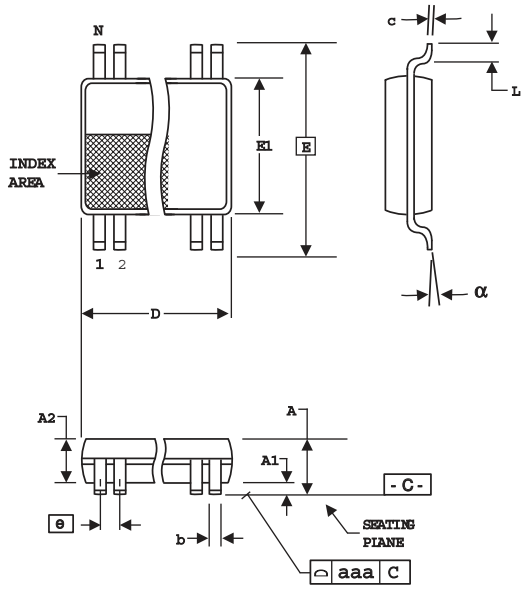
Ordering Information

932S203yFLxT

Example:

XXXX y F Lx T

- **Designation for tape and reel packaging**
- **LF or LN = Lead Free, RoSH Compliant (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 to 7 digit numbers)**



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.30
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

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Ordering Information

932S203yGLxT

Example:

XXXX y G Lx T

- **Designation for tape and reel packaging**
- **LF or LN = Lead Free, RoSH Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 to 7 digit numbers)**

Revision History

Rev.	Issue Date	Description	Page #
F	9/30/2005	1. Corrected Frequency Select Table Typo. i. Added Foot Note. 2. Updated LF Ordering Information.	3, 16-17
G	1/26/2010	Update document template	

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