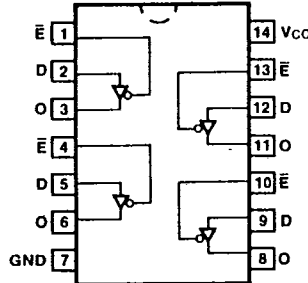


**54/74125**  
**54LS/74LS125A**  
 QUAD BUS BUFFER GATE  
 (With 3-State Outputs)

**CONNECTION DIAGRAM**  
 PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74125PC, 74LS125APC		9A
Ceramic DIP (D)	A	74125DC, 74LS125ADC	54125DM, 54LS125ADM	6A
Flatpak (F)	A	74125FC, 74LS125AFC	54125FM, 54LS125AFM	3I

**TRUTH TABLE**

INPUTS		OUTPUT
$\bar{E}$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10 (50)	65/15 (25)/(7.5)

DC AND AC CHARACTERISTICS: See Section 3\*

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
V <sub>OH</sub>	Output HIGH Voltage	XM	2.4			V	I <sub>OH</sub> = -2.0 mA
			2.4				I <sub>OH</sub> = -5.2 mA
				2.4			I <sub>OH</sub> = -1.0 mA
				2.4			I <sub>OH</sub> = -2.6 mA
I <sub>OS</sub>	Output Short Circuit Current	XC	-30 -70	-30 -130	mA	V <sub>CC</sub> = Max	
			-28 -70	-30 -130			
I <sub>CC</sub>	Power Supply Current		54	20	mA	Outputs OFF, V <sub>IN</sub> = Gnd V <sub>E</sub> = 4.5 V, V <sub>CC</sub> = Max	
t <sub>PLH</sub>	Propagation Delay		13	15	ns	Figs. 3-3, 3-5	
t <sub>PHL</sub>	Data to Output		18	18			
t <sub>PZH</sub>	Output Enable Time		17	16	ns	Figs. 3-3, 3-11, 3-12	
t <sub>PZL</sub>			25	25			
t <sub>PLZ</sub>	Output Disable Time		8.0	25	ns	Figs. 3-3, 3-11, 3-12	
t <sub>PHZ</sub>			12	25			

\*DC limits apply over operating temperature range; AC limits apply at T<sub>A</sub> = +25°C and V<sub>CC</sub> = +5.0 V.

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