S28HS256T/S28HS512T/S28HS01GT
S28HL256T/S28HL512T/S28HL01GT

256-Mb (32-MB)/512-Mb (64-MB)/ 1-Gb (128-MB), HS-T (1.8-V)/HL-T (3.0-V), Semper® Flash with Octal Interface

Device Overview

Architecture

- Cypress 45-nm MirrorBit® technology that stores two data bits in each memory array cell
- Sector Architecture options
  - Uniform: Address space consists of all 256 KB Sectors
  - Hybrid:
    - Configuration 1 - Address space consists of thirty-two 4 KB sectors grouped either on the top or the bottom while the remaining sectors are all 256 KB
    - Configuration 2 - Address space consists of thirty-two 4 KB sectors equally split between top and bottom while the remaining sectors are all 256 KB
- Page Programming buffer of 256 or 512 bytes
- OTP Secure Silicon array of 1024 bytes (32 × 32 bytes)

Interface

- Octal Interface (8S-8S-8S, 8D-8D-8D)
  - JEDEC eXpanded SPI (JESD251) compliant
  - SDR option runs up to 200 MBps (200 MHz clock speed)
  - DDR option runs up to 400 MBps (200 MHz clock speed)
  - Supports Data Strobe (DS) to simplify the read data capture in high-speed systems
- Serial Peripheral Interface (1S-1S-1S)
  - JEDEC eXpanded SPI (JESD251) compliant
  - SDR option runs up to 21 MBps (166 MHz clock speed)

Highlights

- Safety Features
  - Functional Safety with the Industry's first ISO26262 ASIL B compliant and ASIL D ready NOR flash
  - EnduraFlex™ Architecture provides High-Endurance and Long Retention Partitions
  - Interface CRC detects errors on communication interface between host controller and Semper™ Flash device
  - Data Integrity CRC detects errors in memory array
  - SafeBoot reports device initialization failures, detects configuration corruption and provides recovery options
  - Built-in Error Correcting Code (ECC) corrects Single-bit Error and detects Double-bit Error (SECDED) on memory array data
  - Sector Erase Status indicator for power loss during erase
- Protection Features
  - Legacy Block Protection for memory array and device configuration
  - Advanced Sector Protection for individual memory array sector based protection
- AutoBoot enables immediate access to the memory array following power-on
- Hardware Reset through CS# Signaling method (JEDEC) OR individual RESET# pin

Identification

- Serial Flash Discoverable Parameters (SFDP) describing device functions and features
- Device Identification, Manufacturer Identification and Unique Identification

Data Integrity

- 256 Mb Devices
  - Min. 640,000 Program-Erase Cycles for the Main array
- 512 Mb Devices
  - Min. 1,280,000 Program-Erase Cycles for the Main array
- 1 Gb Devices
  - Min. 2,560,000 Program-Erase Cycles for the Main array
- All Devices
  - Min. 300,000 Program-Erase Cycles for the 4 KB Sectors
  - Minimum 25 Years Data Retention

Supply Voltage

- 1.7-V to 2.0-V (HS-T)
- 2.7-V to 3.6-V (HL-T)

Grade/Temperature Range

- Industrial (–40 °C to +85 °C)
- Industrial Plus (–40 °C to +105 °C)
- Automotive AEC-Q100 Grade 3 (–40 °C to +85 °C)
- Automotive AEC-Q100 Grade 2 (–40 °C to +105 °C)
- Automotive AEC-Q100 Grade 1 (–40 °C to +125 °C)

Packages

- 256 Mb and 512 Mb:
  - 24-ball BGA 6 × 8 mm
- 1 Gb:
  - 24-ball BGA 8 × 8 mm

Performance Summary

Maximum Read Rates

Transaction	Initial Access Latency (Cycles)	Clock Rate (MHz)	MBps
SPI Read	0	50	6.25
SPI Read Fast	10	166	20.75
Octal Read SDR (HS-T)	16	200	200
Octal Read SDR (HL-T)	14	166	166
Octal Read DDR (HS-T)	23	200	400
Octal Read DDR (HL-T)	20	166	332

Typical Program and Erase Rates

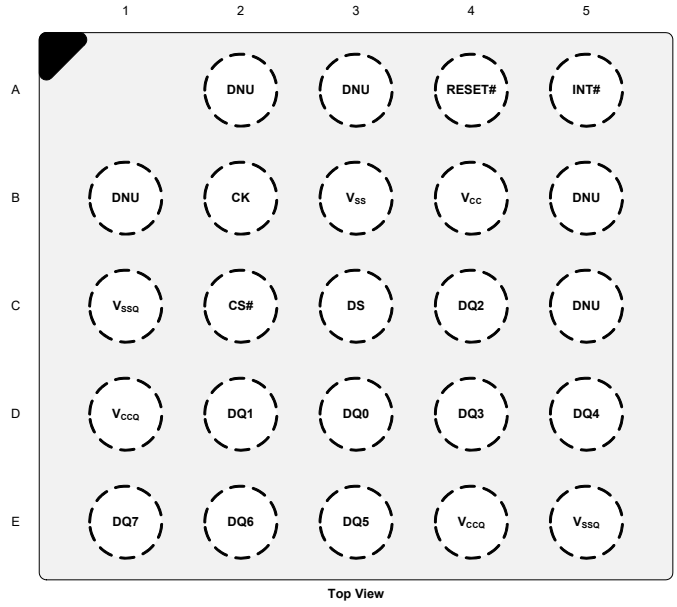
Operation	KBps
256B Page Programming (4 KB Sector / 256 KB Sector)	595 / 533
512B Page Programming (4 KB Sector / 256 KB Sector)	753 / 898
256 KB Sector Erase	331
4 KB Sector Erase	95

Typical Current Consumption

Operation	HL-T Current (mA)	HS-T Current (mA)
SDR Read 50 MHz	10	10
SDR Read (Octal)	75 (166 MHz)	156 (200 MHz)
DDR Read (Octal)	75 (166 MHz)	156 (200 MHz)
Program	50	50
Erase	50	50
Standby	0.014	0.011
Deep Power Down	0.0022	0.0013

Pinout and Signal Description

Figure 1. 24-Ball BGA Pinout Configuration[1]



Top View

Note
1. Flash memory devices in BGA packages can be damaged if exposed to ultrasonic cleaning methods. The package, data integrity, or both may be compromised if the package body is exposed to temperatures above 150 °C for prolonged periods of time.

Table 1. Signal Description

Symbol	Type	Mandatory / Optional	Description
CS#	Input	Mandatory	**Chip Select (CS#).** All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the active mode. When CS# is driven HIGH, the device enters standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in high impedance state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH.
CK	Input	Mandatory	**Clock (CK)**. Clock provides the timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
DS	Output	Mandatory	**Read Data Strobe (DS)**. DS is used for data read operations only and indicates output data valid for SDR/DDR modes. During a read transaction while CS# is LOW, DS toggles to synchronize data output until CS# goes High.
DQ[7:0]	Input/Output	Mandatory	**Serial Data (DQ[7:0])**. Bidirectional signals that transfer command, address and data information. **Legacy (x1) SPI Interface**: DQ[0] is an input (SI) and DQ[1] is an output (SO). **Octal (x8) Interface**: DQ[7:0] are input and output.
RESET#	Input (weak pull-up)	Optional	**Hardware Reset (RESET#)**. When LOW, the device will self initialize and return to the array read state. DS and DQ[7:0] are placed into the high impedance state when RESET# is LOW. RESET# includes a weak pull-up, meaning, if RESET# is left unconnected it will be pulled up to the HIGH state on its own.
INT#	Output (Open Drain)	Optional	**System Interrupt (INT#)**. When LOW, the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. The recommended pull-up resistor for the INT# outputs is 5 kΩ to 10 kΩ.
V_{CC}	Power supply	Mandatory	Core Power Supply
V_{CCQ}	Power supply	Mandatory	Input / Output Power Supply
V_{SS}	Ground supply	Mandatory	Core Ground
V_{SSQ}	Ground supply	Mandatory	Input / Output Ground
DNU	–	–	**Do Not Use.**

General Description

The Cypress Semper™ Flash Octal family of products are high-speed CMOS, MirrorBit NOR flash devices that are compliant with the JEDEC JESD251 eXpanded SPI (xSPI) specification. Semper Flash is designed for Functional Safety with development according to ISO 26262 standard to achieve ASIL-B compliance and ASIL-D readiness.

Semper Flash with Octal Interface devices support both the Octal Peripheral Interface (OPI) as well as Legacy x1 Serial Peripheral Interface (SPI). Both interfaces serially transfer transactions reducing the number of interface connection signals. SPI supports SDR whereas OPI supports both SDR and DDR.

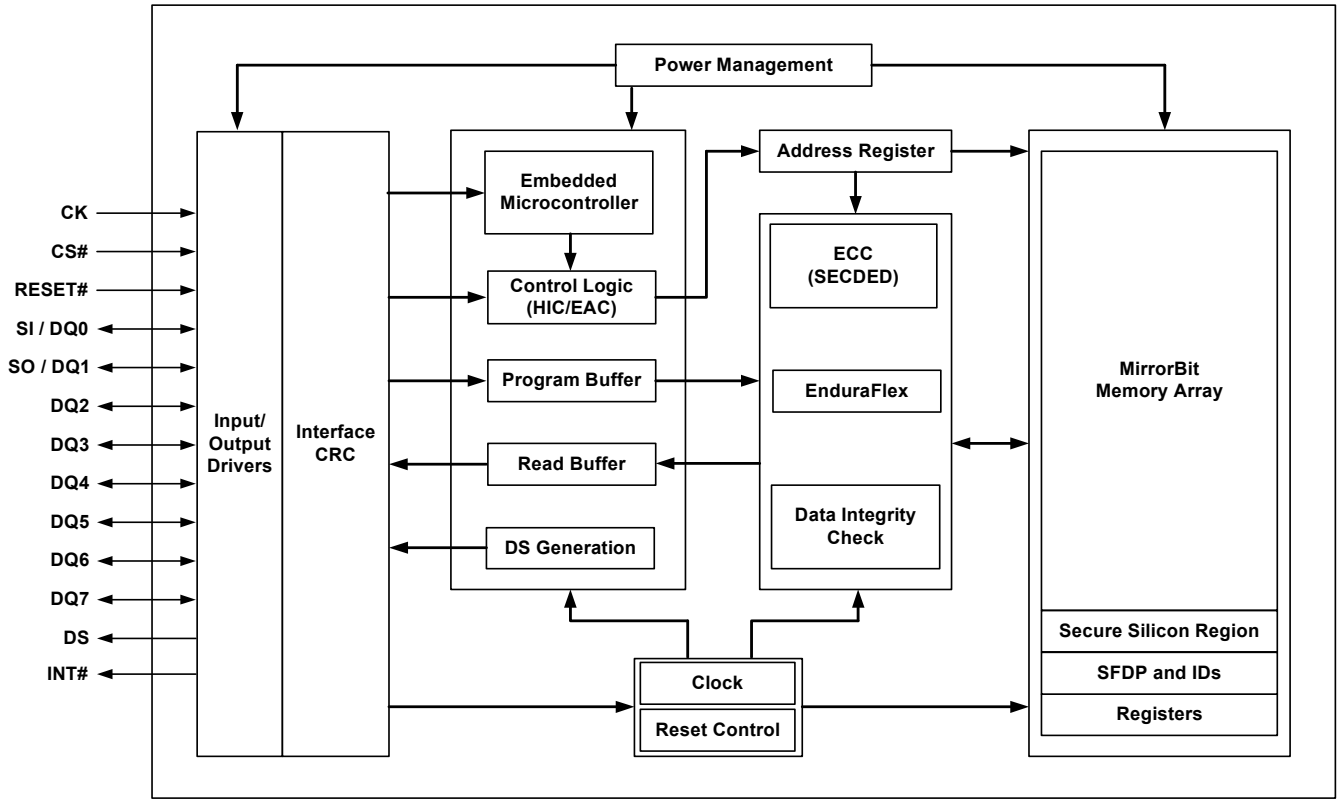
Read operations from the device are burst oriented. Read transactions can be configured to use either a wrapped or linear burst. Wrapped bursts read from a single page whereas linear bursts can read the whole memory array.

The erased state of each memory bit is a logic 1. Programming changes a logic 1 (HIGH) to a logic 0 (LOW). Only an erase operation can change a memory bit from a 0 to a 1. An erase operation must be performed on a complete sector (4 KBs or 256 KBs).

Semper Flash provides a flexible sector architecture. The address space can be configured as either a uniform 256 KB sector array, or a hybrid configuration 1 where thirty-two 4 KB sectors are either grouped at the top or at the bottom while the remaining sectors are all 256 KB, or a hybrid configuration 2 where the thirty-two 4 KB sectors are equally split between the top and the bottom while the remaining sectors are all 256 KB.

The Page Programming Buffer used during a single programming operation is configurable to either 256 bytes or 512 bytes. The 512 byte option provides the highest programming throughput.

Figure 2. Logic Block Diagram



The Semper Flash with Octal Interface family consists of multiple densities with, 1.8V and 3.0V core and I/O voltage options.

The device control logic is subdivided into two parallel operating sections: the Host Interface Controller (HIC) and the Embedded Algorithm Controller (EAC). The HIC monitors signal levels on the device inputs and drives outputs as needed to complete read, program, and write data transfers with the host system. The HIC delivers data from the currently entered address map on read transfers; places write transfer address and data information into the EAC command memory, and notifies the EAC of power transition, and write transfers. The EAC interrogates the command memory, after a program or write transfer, for legal command sequences and performs the related Embedded Algorithms.

Changing the nonvolatile data in the memory array requires a sequence of operations that are part of Embedded Algorithms (EA). The algorithms are managed entirely by the internal EAC. The main algorithms perform programming and erase of the main flash

array data. The host system writes command codes to the flash device. The EAC receives the command, performs all the necessary steps to complete the transaction, and provides status information during the progress of an EA.

In addition to the mandatory SPI signals CK, CS#, SI/DQ0, SO/DQ1, and DQ[7:2], the Semper Flash with Octal Interface device also includes RESET#, DS and INT# signals. The RESET# transition from LOW to HIGH returns the device to the default state that occurs after an internal power-on reset (POR). The Data Strobe (DS) is synchronized with the output data during read transactions enabling host system to capture data at high clock frequency operation. The INT# is an open-drain output that can provide an interrupt to the device master to indicate when the device transitions from busy to ready at the end of a program or erase operation or to indicate the detection of an error (ECC) during read.

EnduraFlex™ Architecture provides system designers the ability to customize the NOR Flash endurance and retention for their specific application. The host defines partitions for high endurance or long retention, providing up to 1+ million cycles or 25 years of data retention.

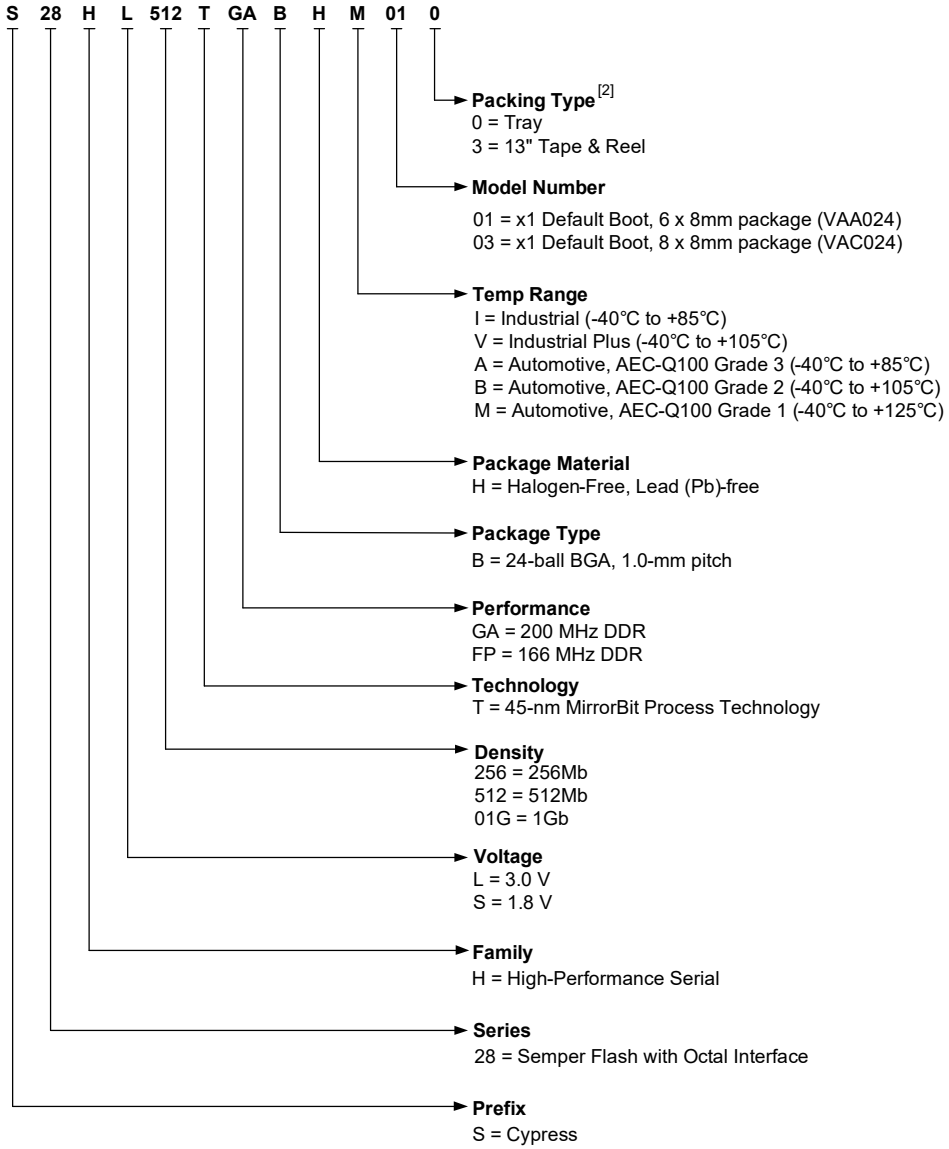
The Semper Flash with Octal Interface device supports error detection and correction by generating an embedded Hamming error correction code during memory array programming. This ECC code is then used for single-bit and double-bit error detection and single-bit correction during read.

The Semper Flash with Octal Interface device has built-in diagnostic features providing the host system with the device status.

- Program and Erase Operation: Reporting of program or erase success, failure and suspend status
- error detection and correction: 1-bit and/or 2-bit error status with address trapping and error count
- Data Integrity Check: Error detection over memory array contents
- Interface CRC: Error detection over device interface
- SafeBoot: Reporting of proper flash device initialization and configuration corruption recovery
- Sector Erase Status: Reporting of erase success or failure status per sector
- Sector Erase Counter: Counts the number of erase cycles per sector

Ordering Information

The ordering part number is formed by a valid combination of the following:



Register for the Semper Access Program and get access to datasheets, application notes, models, software, and evaluation kits.

Note
2. See Packing and Packaging Handbook on www.cypress.com for further information.

Document History Page

Document Title: S28HS256T/S28HS512T/S28HS01GT/S28HL256T/S28HL512T/S28HL01GT, 256-Mb (32-MB)/512-Mb (64-MB)/ 1-Gb (128-MB), HS-T (1.8-V)/HL-T (3.0-V), Semper® Flash with Octal Interface Document Number: 002-23881			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	6169693	05/09/2018	New data sheet.
*A	6616129	07/08/2019	Changed status from Preliminary to Final. Updated Document Title to read as "S28HS256T/S28HS512T/S28HS01GT/S28HL256T/S28HL512T/S28HL01GT, 256-Mb (32-MB)/512-Mb (64-MB)/ 1-Gb (128-MB), HS-T (1.8-V)/HL-T (3.0-V), Semper® Flash with Octal Interface". Added S28HS256T, S28HL256T parts related information in all instances across the document. Updated to new template.

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