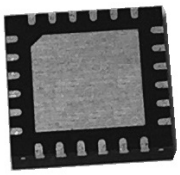
15SCT000C
DUAL-CHANNEL RCD CONTROLLER
(Residual Current Device)

15SCT000C - SPECIFICATION - RELEASED FEBRUARY 21, 2020

Features

- **Dual channels**
- **Noise filter**
- **Adjustable sensitivity**
- **Precision sense amplifiers**
- **Integrated output driver**
- **Trip feedback**
- **5 × 5 QFN-24 package**



Description

The 15SCT000C is a a dual-channel control circuit intended for application in a Residual Current Circuit Breaker (RCBO) or Residual Current Device (RCD). It features precision sense amplifiers and window comparators for sensing any imbalance in a current transformer, integrated together with fault integration timers and fault latches. External components configure the circuit for sensitivities of 10mA or 30mA as well as different line voltages. The circuit features allow trip feedback and active noise filters to minimize power-on and nuisance tripping.

Absolute maximum ratings

Supply current ($I_{CC)}$ . . . . . +15 mA
Operating temperature . . . . . -40 C to 100 C
Storage temperature. . . . . -65 C to 125 C

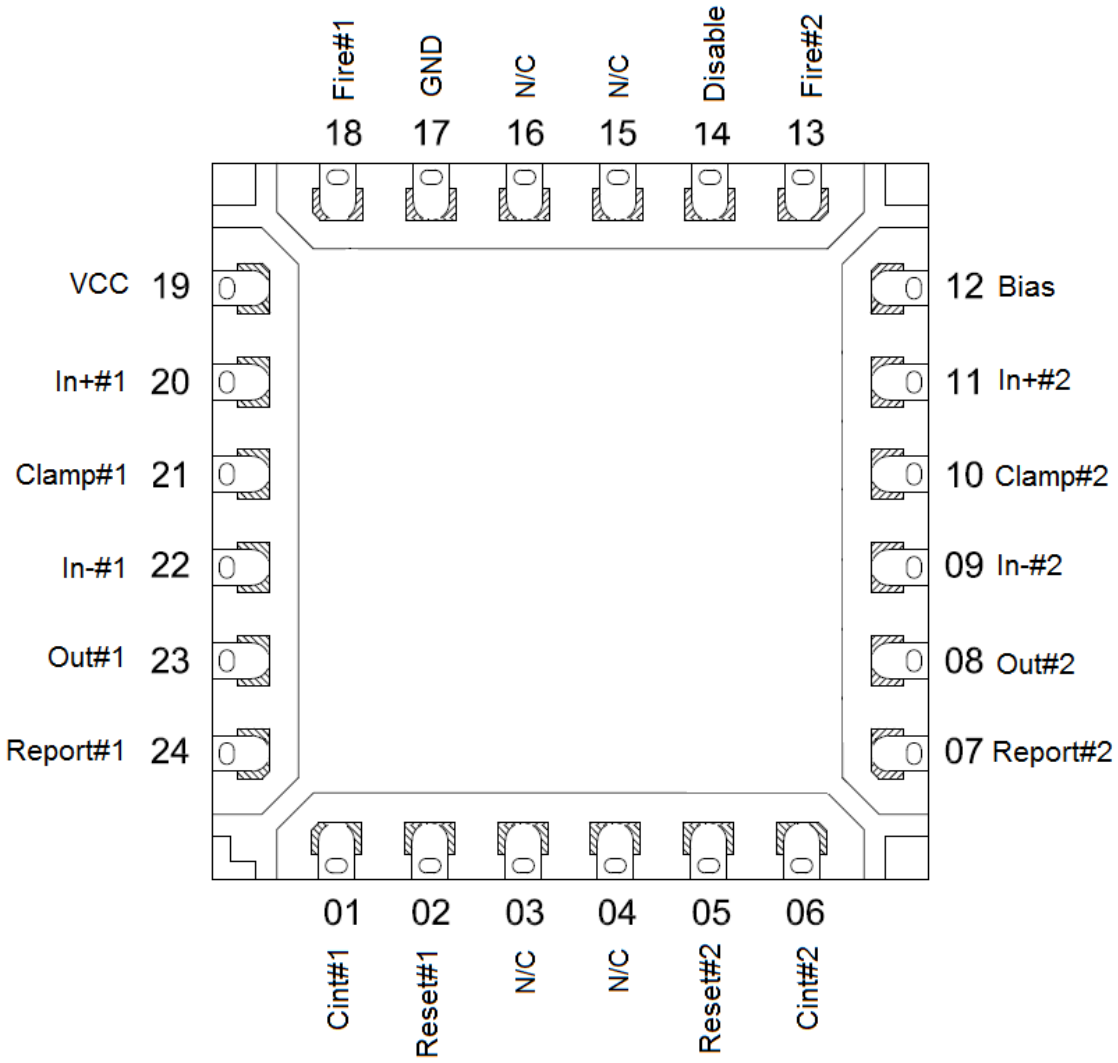
Recommended operating conditions

PARAMETER	TYP	UNIT
Operating current (V_{CC})	10	mA

Pin definitions

Pin #	Name	Description
1	CInt#1	Channel 1 integration capacitor (external capacitor to GND)
2	Reset#1	Channel 1 reset (asserted high)
3	NC	No connection
4	NC	No connection
5	Reset#2	Channel 2 reset (asserted high)
6	Cint#2	Channel 2 integration capacitor (external capacitor to GND)
7	Report#2	Channel 2 report output (asserted low)
8	Out#2	Channel 2 pre-amplifier output
9	In-#2	Channel 2 pre-amplifier inverting input
10	Clamp#2	Channel 2 clamp
11	In+#2	Channel 2 pre-amplifier non-inverting input
12	Bias	Chip current bias (external resistor to GND)
13	Fire#2	Channel 2 fire output (asserted low)
14	Disable	Disable input for both channels
15	NC	No connection
16	NC	No connection
17	GND	Negative power supply
18	Fire#1	Channel 1 fire output
19	VCC	Positive power supply
20	In+#1	Channel 1 pre-amplifier non-inverting input
21	Clamp#1	Channel 1 clamp
22	In-#1	Channel 1 pre-amplifier inverting input
23	Out#1	Channel 1 pre-amplifier output
24	Report#1	Channel 1 report output (asserted low)

Pinout



Top View

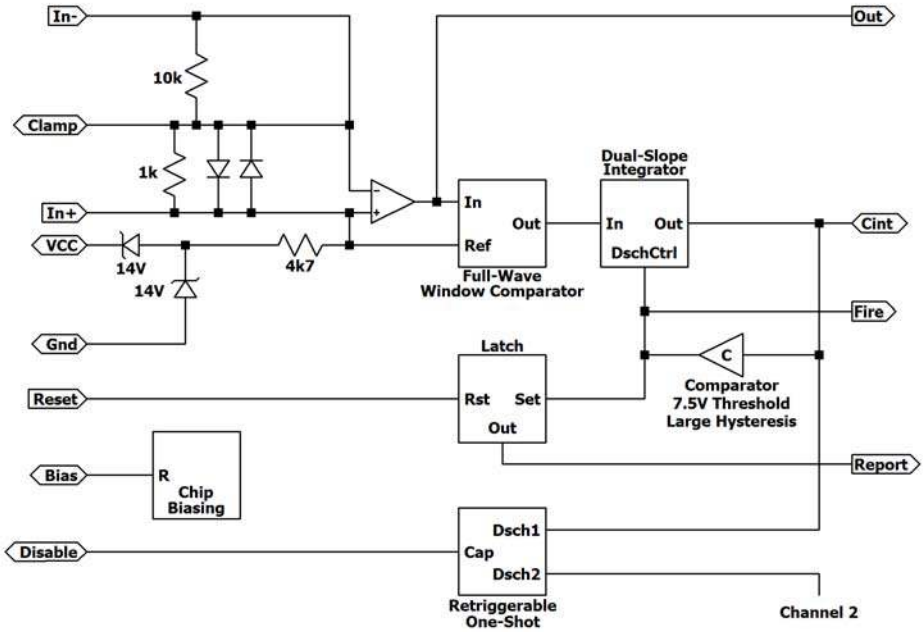
Electrical characteristics ($25^oC \pm 5^oC$ unless specified)

(where #n is either 1 or 2, the channel number)

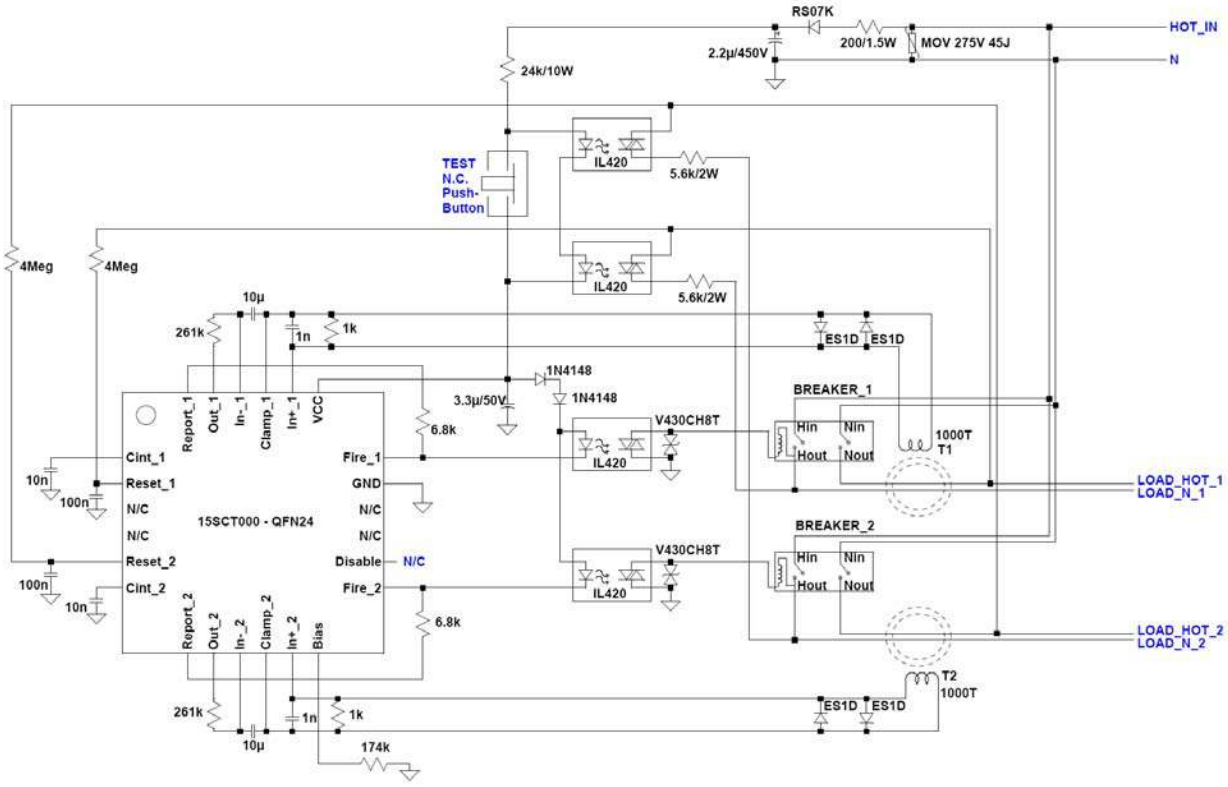
Symbol	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VCC	Supply Voltage	ICC=10mA	26.00	28.00	30.00	V
Vin+#n	Preamp non-inv input voltage	ICC=10mA	13.00	14.00	15.00	V
Vout#n-Vin+#n	Preamp Vout#n - Vin+#n	ICC=10mA 200kΩ between Vout#n & Vin+#n	-500	0	+500	mV
Bias	Voltage reference	100k to GND	6.35	6.70	7.25	V
Disable	Disable voltage	ICC=10mA	12.00	12.70	13.25	V
I(Disable)	Disable current	Disable=0V	-9.00	-6.50	-4.00	μA
Cint#n; V(Cint#n)	Integration cap minimum voltage	I(CInt#n)=10mA	0.60	1.00	1.50	V
NoFlt; Report#n	V_{Report}#n; no fault detected	Reset=10V Vin-#n=14V	25.00	27.00	29.00	V
NoFlt; VCC-VF#n	V_{CC} - V_{Fire}#n; no fault detected	Reset=10V Vin-#n=14V	0.10	0.50	1.00	V
Flt; Report#nL	V_{Report}#n; fault detected	Reset=10V Vin-#n=5V	0.80	1.00	1.20	V
Flt; VCC-VF#n	V_{CC} - V_{Fire}#n; fault detected	Reset=10V Vin-#n=5V	3.00	4.50	6.00	V
Mem; VCC-VF#n	V_{CC} - V_{Fire}#n; fault removed	Reset=10V Vin-#n=14V	1.00	1.50	1.90	V
Mem; Report#n	V_{Report}#n; fault removed	Reset=10V Vin-#n=14V	0.80	1.00	1.20	V
Clrd; Report#n	V_{Report}#n; memory cleared	Reset=-10V then +10V Vin-#n=14V	25.00	27.00	29.00	V
Clrd; VCC-VF#n	V_{CC} - V_{Fire}#n; memory cleared	Reset=-10V then +10V Vin-#n=14V	0.10	0.50	1.00	V
OutL#n	Vin-#n; Window cmp low threshold	Ramp Vin-#n 6.0V to 9.0V until VReport>14V	6.50	7.00	8.50	V
OutH#n	Vin-#n; Window cmp high threshold	Ramp Vin-#n 18.0V to 24.0V until VReport<14V	19.00	21.00	22.00	V

Symbol	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Cint#n NrmlDsch	Integration cap normal discharge	Vin-#n=14V Cint#n=5V	1.00	1.70	2.30	µA
Cint#n FltChrg	Integration cap fault charge	Vin-#n=5V Cint#n=5V	-90.00	-65.00	-40.00	µA
V(HCth#n)	Hysteresis cmp. trigger threshold	Vin-#n=5V Ramp Cint#n 5.5V to 8.5V |I(Cint#n)|<10µA	6.70	7.20	7.50	V
I(HCth#n) Fault	Int. cap discharge; fault detected	Vin-#n=5V Cint#n=8V	-5.30	-3.50	-1.80	µA
I(HCth#n) NoFlt	Int. cap discharge; no fault detected	Vin-#n=14V Cint#n=8V	1.15	1.70	2.57	µA
R(In+Clamp#n)	Resistance In+ to Clamp	@ 200µA	0.94	1.00	1.58	kΩ
R(In-Clamp#n)	Resistance In- to Clamp	@ 200µA	8.48	10.00	14.22	kΩ
V(Clmp#n) Diff	Sum of two Clamp diodes forward V	@ 1mA	1.35	1.47	1.60	V
BiasThresh	Bias threshold; VCC	Disable=0V Ramp VCC 10.0V to 24.0V I(Disable)<-3µA	16.0	21.00	23.50	V
PowerOnTrip#n	Monitor V_{Report} at power-on	ICC=10mA	25.00	27.00	29.00	V

Functional partition (block diagram of one channel)



Reference Design (Dual channel RCBO 230V I∆n=30mA)



Concept of operation

The chip is powered by supplying 10mA (typical) into V_{CC} (here set at 230Vac). The chip will regulate the V_{CC} voltage to approximately 28V with respect to neutral, with the non-inverting inputs of the pre-amplifiers (In+#n) biased at about V_{CC} /2 with respect to neutral. The bias pin is connected to a 180k resistor and establishes a reference current (6.7V/180k) providing internal bias to both channels.

Any imbalance in the active and neutral load currents is detected by an external toroid (T1 or T2). A secondary winding on the toroid will produce a current proportional to the difference in the current flowing in the active and neutral wires passing through the toroid core divided by the number of turns (1000T in the reference design). This secondary imbalance current is input to the preamplifier. Preamplifier sensitivity is controlled by 270k external resistors for meeting 30mA trip threshold.

The sensitivity threshold is set by ΔIn/1000 X R(Out:In-) > 7.2V. In the reference design above R is 261k and the DC sensitivity threshold (ΔIn) is set at 7.2V/261k*1000 = 27.6mAdc which is a good value for ensuring that the RCBO trips below 30mArms.

The preamplifier output is internally applied to a full-wave window comparator, which detects signals above or below its threshold (+/-7.0V).

The output of the fault detecting comparator is then integrated by charging and discharging a 10nF external capacitor with the “Integration Fault Charge” current if a fault is present and with “Integration cap normal discharge“ current if the fault is removed. This integration provides noise immunity since the output of the integrator will only be asserted if the fault is present for a time determined by a current supplied by the chip charging and discharging an external capacitor combined with a high detection threshold (~7.2V).

In the Reference Design above, the integration capacitor is 10nF, assuming the fault is constant a nominal current of ~37uA (Cint#n FltChrg / 1.74) will charge this capacitor to 7.2V (HCth#n) in 1.9mSec. This provide provides sufficient noise immunity while having little impact on the detection time which are typically 5-10 times longer.

If the integrator output exceeds the firing comparator threshold, the fault is latched, and the Report line turns low to trip the breaker. Simultaneously, the Fire line voltage drops, which is optically coupled to breaker’s solenoid, therefore opening the AC circuit under fault. When the breaker is manually reset, the Reset pin is pulled high within a half-cycle to clear the fault condition returning the circuit to monitoring mode.

The circuit can be tested by pressing the TEST switch (open) which connects the 5.6k resistors to LOAD_HOT forcing a current imbalance of about 41mArms (~230Vrms/5.6k). This imbalance current will cause the circuit to trip both breakers open.

Each channel is completely independent for the other one. Channels only share the bias current set at pin 12. The reference current is used for internal bias and also capacitor integration currents setting noise immunity.

If trip feedback is required, the user can add an opto-coupler to sense current flowing in the 6.8k resistors between Report and Fire pins, therefore allowing the system to interact with micro-controllers for example.

Shorting the disable pin to GND will disable both channels. This is obviously not the case in a standard reference design but can be useful should the user require to temporarily bypass the RCD function.

Sample EN 61009 results

Subset of worst case results EN 61009-1-2012 Clause 9.9.1

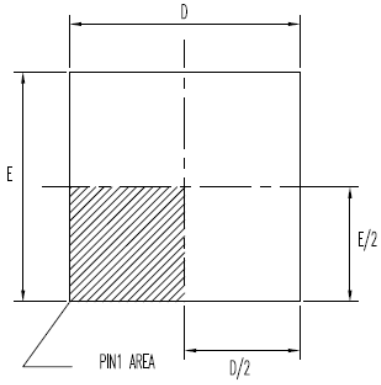
Sub-Clause		Worse Case	MaxSpec	
9.9.1.2.a	(Trip Threshold)			
	195V 50Hz	22.97	30.00	mA
	230V 50Hz	22.95	30.00	mA
	253V 50Hz	23.33	30.00	mA
9.9.1.2.b	(Breaker close on of fault current)			
	230V 50Hz @ 30mA	17	300	mSec
	230V 50Hz @ 60mA	20	150	mSec
	230V 50Hz @ 150mA	20	40	mSec
9.9.1.2.c	(Source close on)			
	230V 50Hz @ 30mA	22	300	mSec
	230V 50Hz @ 60mA	22	150	mSec
	230V 50Hz @ 150mA	20	40	mSec
9.9.1.2.d	(High current faults)			
	230V 50Hz @ 5A	10	40	mSec
	230V 50Hz @ 20A	18	40	mSec
9.9.1.2.e.B	(With load tests)			
	230V 50Hz @ 30mA	21	300	mSec
	230V 50Hz @ 60mA	13	150	mSec
	230V 50Hz @ 150mA	13	40	mSec
9.9.1.2.e.C	(With load tests)			
	230V 50Hz @ 30mA	21	300	mSec
	230V 50Hz @ 60mA	14	150	mSec
	230V 50Hz @ 150mA	14	40	mSec
9.9.1.2.f (-5°C)	(Temperature limits)			
	230V 50Hz @ 30mA	26	300	mSec
	230V 50Hz @ 60mA	19	150	mSec
	230V 50Hz @ 150mA	19	40	mSec
9.9.1.2.f (+40°C)	(Temperature limits)			
	230V 50Hz @ 30mA	24	300	mSec
	230V 50Hz @ 60mA	22	150	mSec
	230V 50Hz @ 150mA	22	40	mSec

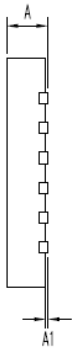
Sub-Clause		Worse Case	MaxSpec	
9.9.1.3.a (0°)	(Trip threshold halfwave with phase control no load)			
	230V 50Hz Pole 1, S3 = I (+HW)	24.07	42	mA
	230V 50Hz Pole 1, S3 = II (+HW)	23.67	42	mA
	230V 50Hz Pole 2, S3 = I (+HW)	24.64	42	mA
	230V 50Hz Pole 2, S3 = II (+HW)	23.54	42	mA
9.9.1.3.a (90°)	(Trip threshold halfwave with phase control no load)			
	230V 50Hz Pole 1, S3 = I (+HW)	13.72	42	mA
	230V 50Hz Pole 1, S3 = II (+HW)	13.28	42	mA
	230V 50Hz Pole 2, S3 = I (+HW)	13.70	42	mA
	230V 50Hz Pole 2, S3 = II (+HW)	13.16	42	mA
9.9.1.3.a (135°)	(Trip threshold halfwave with phase control no load)			
	230V 50Hz Pole 1, S3 = I (+HW)	11.01	42	mA
	230V 50Hz Pole 1, S3 = II (+HW)	10.84	42	mA
	230V 50Hz Pole 2, S3 = I (+HW)	10.95	42	mA
	230V 50Hz Pole 2, S3 = II (+HW)	10.84	42	mA
9.9.1.3.b	(Trip Time half wave no load)			
	230V 50Hz @ 42mA	8	300	mSec
	230V 50Hz @ 84mA	8	150	mSec
	230V 50Hz @ 350mA	8	40	mSec
9.9.1.3.c (0°)	(Trip threshold halfwave with phase control with rated load)			
	230V 50Hz Pole 1, S3 = I (+HW)	26.07	42	mA
	230V 50Hz Pole 1, S3 = II (+HW)	25.55	42	mA
	230V 50Hz Pole 2, S3 = I (+HW)	26.05	42	mA
	230V 50Hz Pole 2, S3 = II (+HW)	25.53	42	mA
9.9.1.3.c (90°)	(Trip threshold halfwave with phase control with rated load)			
	230V 50Hz Pole 1, S3 = I (+HW)	15.79	42	mA
	230V 50Hz Pole 1, S3 = II (+HW)	15.25	42	mA
	230V 50Hz Pole 2, S3 = I (+HW)	15.42	42	mA
	230V 50Hz Pole 2, S3 = II (+HW)	15.12	42	mA
9.9.1.3.c (135°)	(Trip threshold halfwave with phase control with rated load)			
	230V 50Hz Pole 1, S3 = I (+HW)	12.68	42	mA
	230V 50Hz Pole 1, S3 = II (+HW)	12.04	42	mA
	230V 50Hz Pole 2, S3 = I (+HW)	11.08	42	mA
	230V 50Hz Pole 2, S3 = II (+HW)	12.1	42	mA
9.9.1.3.d (0°)	(Trip threshold half wave with superimposed 6mA DC)			
	230V 50Hz Pole 1, S3 = I (+HW)	24.15	42	mA
	230V 50Hz Pole 1, S3 = II (+HW)	24.11	42	mA
	230V 50Hz Pole 2, S3 = I (+HW)	24.86	42	mA
	230V 50Hz Pole 2, S3 = II (+HW)	24.17	42	mA

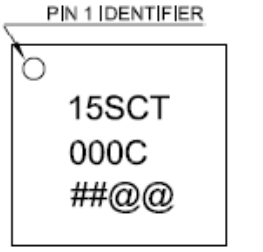
Package dimensions

5.0x5.0 MM QFN

PACKAGE INFORMATION







= Year Code

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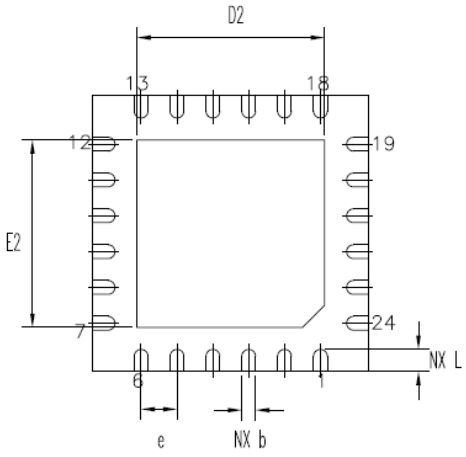

JEDEC#	NOT APPLICABLE			
TYPE	24 LEAD			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.85	0.95	33.46	37.40
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	4.9	5.1	192.91	200.79
E	4.9	5.1	192.91	200.79
D2	3.35	3.45	131.89	135.83
E2	3.35	3.45	131.89	135.83
e	0.65 BSC		25.59 BSC	
NX b	0.2	0.3	7.88	11.81
NX L	0.35	0.45	13.78	17.72
θ°	0°	4°	0°	4°
ND	6			
NE	6			

NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
   DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.