User's Guide

TLV841EVM Voltage Supervisor User Guide

Ben Chan

ABSTRACT

This user guide describes the TLV841EVM evaluation module (EVM). This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The TLV841EVM is an evaluation module (EVM) for the TLV841 voltage supervisor. Refer to TLV841 datasheet to understand the device features supported by different variants. The TLV841EVM can be used with any TLV841 device variant, TLV841M, TLV841C, and TLV841S. The TLV841EVM comes pre-populated with TLV841SADL01YBHR. If users need a different option, the existing device must be removed from the board and replaced. The EVM board is designed to support all possible options by changing jumper configuration.

The TLV841EVM also can accommodate push-pull variants (TLV841xxPLxx or TLV841xxPHxx). If a push-pull variant is placed onto the TLV841EVM, the shunt on J1 must be removed as push-pull devices do not use a pull-up resistor. Therefore, R1 on the TLV841EVM must be disconnected. Please also note if using TLV841EVM with the active-high variant (TLV841xxPHxx), the active-low $\overline{\text{RESET}}$ label on the EVM board and throughout this User Guide becomes active-high RESET. Active low $\overline{\text{RESET}}$ output with open-drain and push-pull topologies have a supply voltage range of 0.7 V to 5.5 V. For active high push-pull outputs (PH output topology), the supply voltage range is 1 V to 5.5 V. The TLV841EVM includes the TLV841S device (TLV841xxDLxx) and the EVM offers connections for all device input and output pins. Test points are provided to give the user additional access, if needed, for oscilloscope or multi-meter measurements.

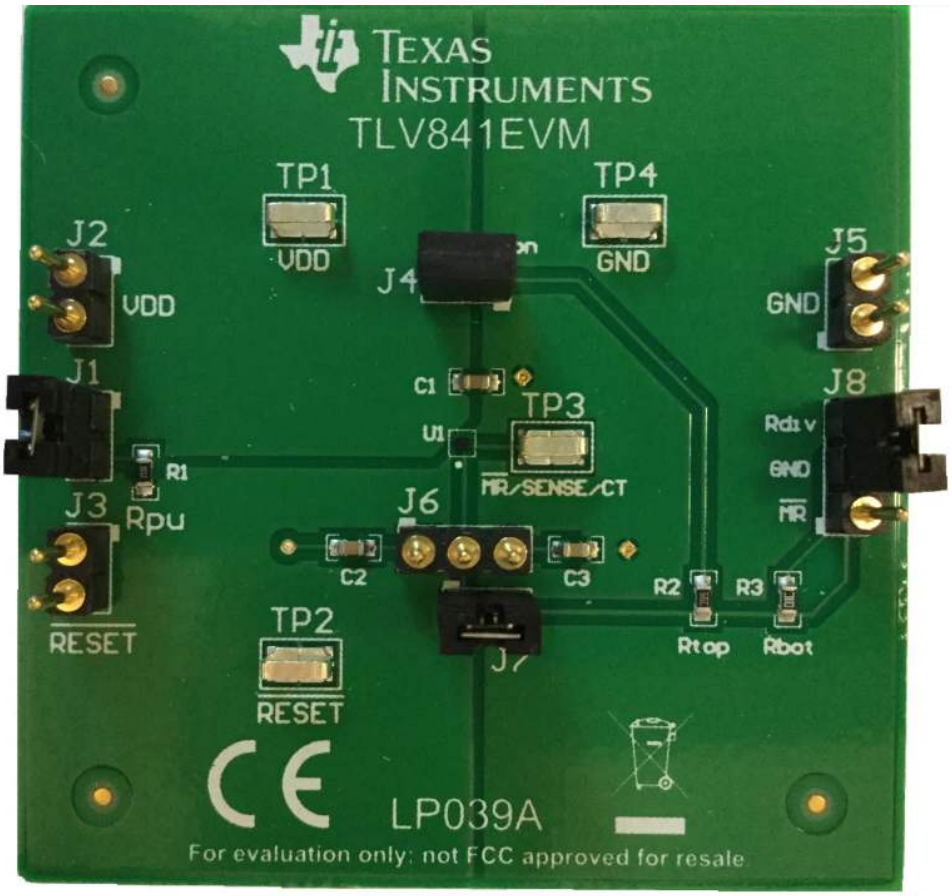

Figure 1-1. TLV841EVM Board Top

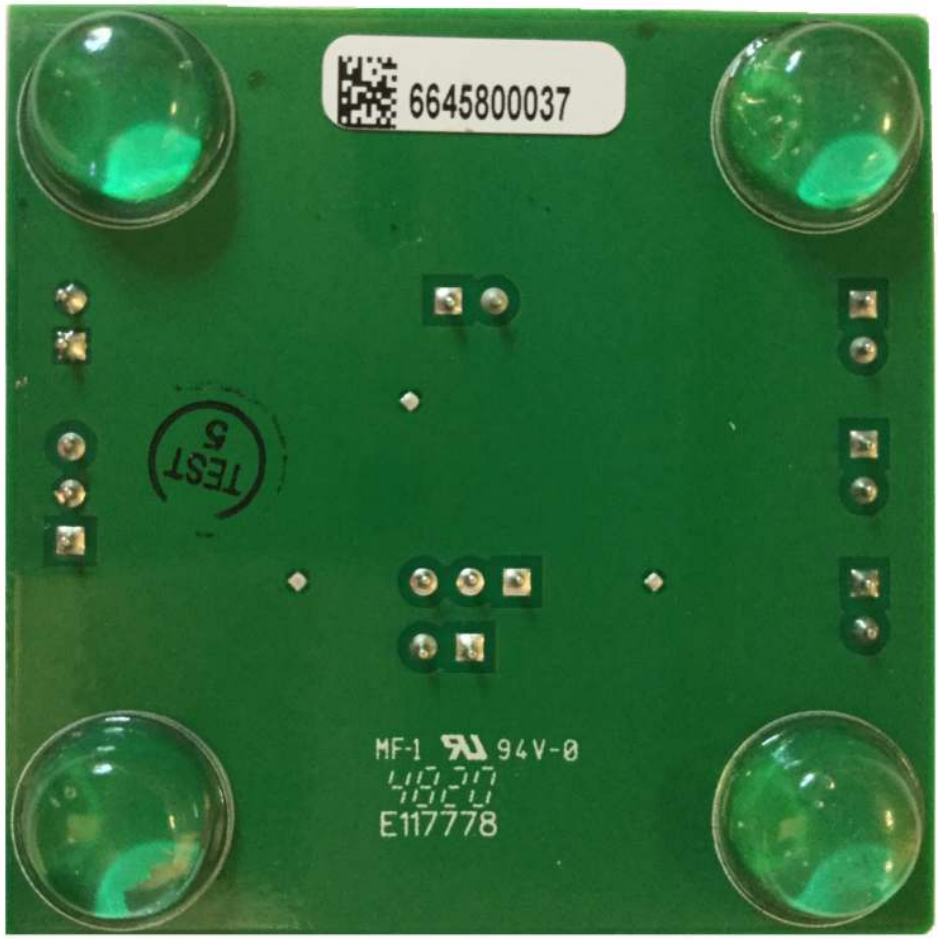

Figure 1-2. TLV841EVM Board Bottom

1.1 Related Documentation

TLV841 Tiny Nano-Power, Ultra-Low Voltage Supervisor in WCSP Package data sheet, TLV841.

1.2 TLV841 Applications

- Personal electronics
- Home theater and entertainment
- Electronic point of sale
- Grid infrastructure
- Data center and enterprise computing

2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TLV841EVM schematic, bill of materials (BOM), and layout.

2.1 TLV841EVM Schematic

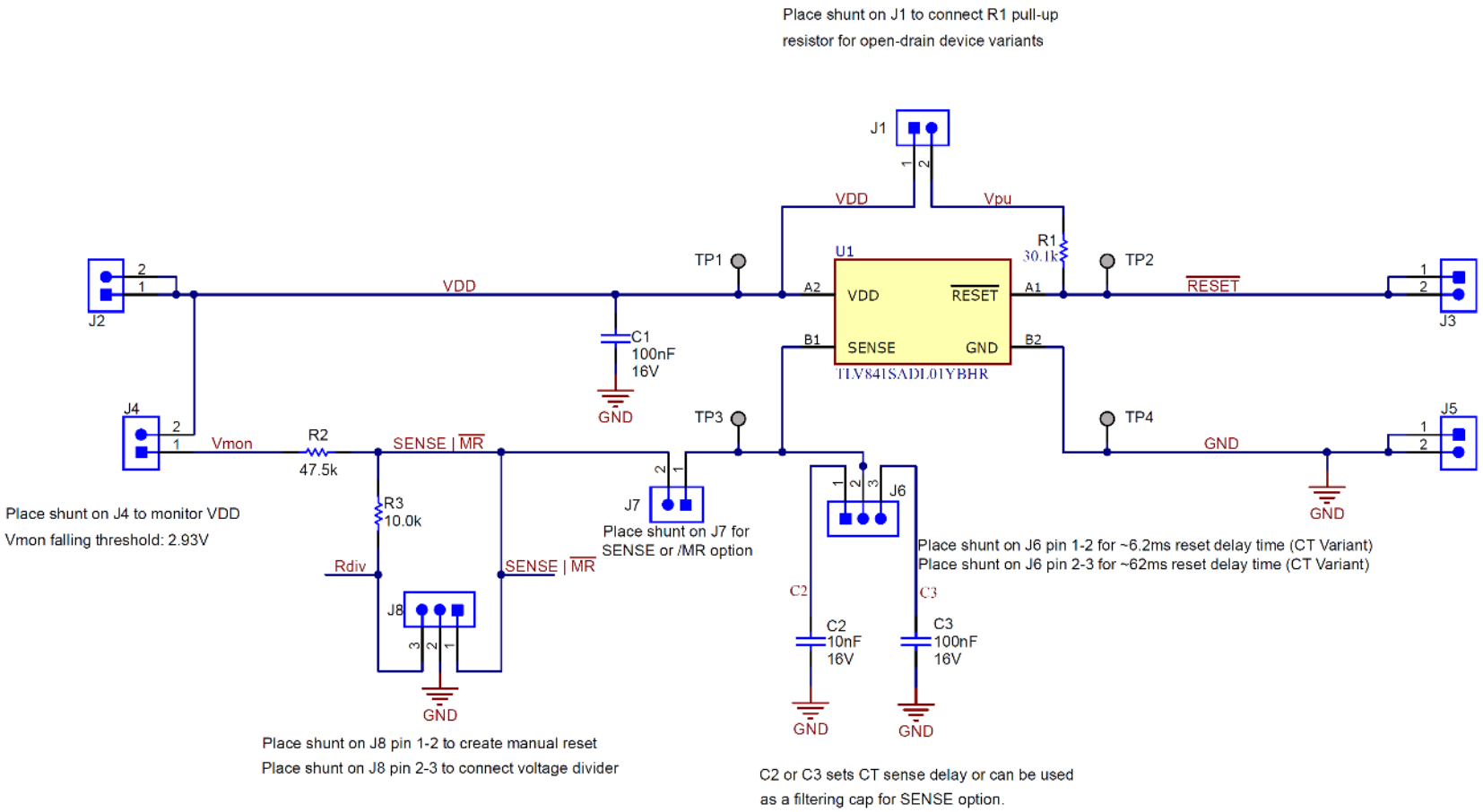

Figure 2-1. TLV841EVM Schematic with TLV841S

2.2 TLV841EVM Bill of Materials

Table 2-1. BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
PCB	1		Printed Circuit Board		TLV841EVM	Any
C1, C3	2	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ± 10%, X7R, 0603	0603	C0603C104K4RACTU	Kemet
C2	1	0.01 µF	CAP, CERM, 0.01 µF, 16 V, +/- 10%, X7R, 0603	0603	C0603C103K4RACTU	Kemet
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J4, J5, J7	6		Header, 100mil, 2x1, TH	Header, 2x1, 100mil, TH	800-10-002-10-001000	Mill-Max
J6, J8	2		Header, 100mil, 3x1, TH	Header, 3x1, 100mil, TH	800-10-003-10-001000	Mill-Max
R1	1	30.1kΩ	RES, 30.1 kΩ, 1%, 0.1 W, 0603	0603	RC0603FR-0730K1L	Yageo America
R2	1	47.5kΩ	RES, 47.5 kΩ, 1%, 0.1 W, 0603	0603	RC0603FR-0747K5L	Yageo America
R3	1	10kΩ	RES, 10.0 kΩ, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo America
SH-J1, SH-J2, SH-J3,SH-J4, SH-J5	5		Shunt, 100mil, Tin plated, Black	Shunt Connector Black Open Top, 2x1	SNT-100-BK-T-H	Samtec
TP1, TP2, TP3, TP4	4		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		Tiny Nano-power Ultra-low Voltage Supervisor in WCSP Package (SENSE option)	DSBGA4	TLV841SADL01YBHR	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

2.3 Layout and Component Placement

Figure 2-2 and Figure 2-3 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 2-4 and Figure 2-5 show the top and bottom layouts, Figure 2-6 and Figure 2-7 show the top and bottom layers, and Figure 2-8 shows the top solder mask of the EVM.

2.4 Layout

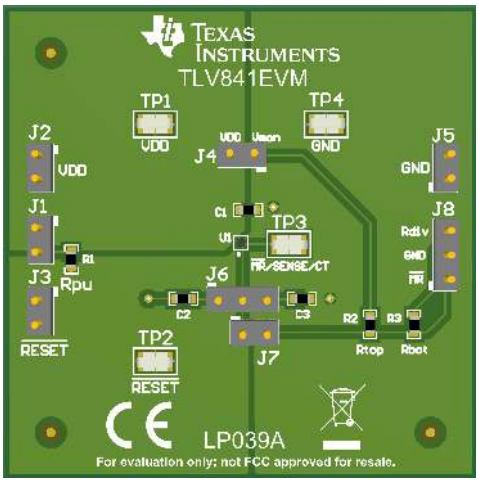

Figure 2-2. Component Placement—Top Assembly

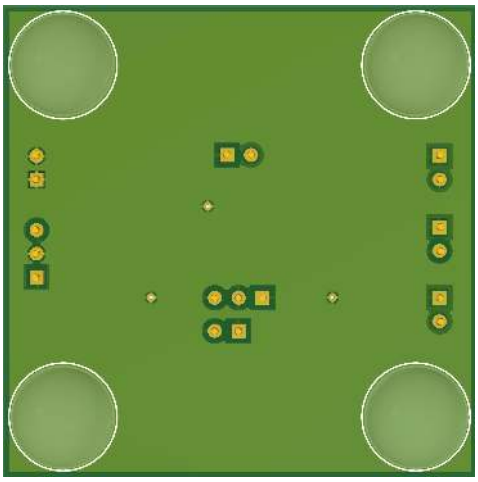

Figure 2-3. Component Placement—Bottom Assembly

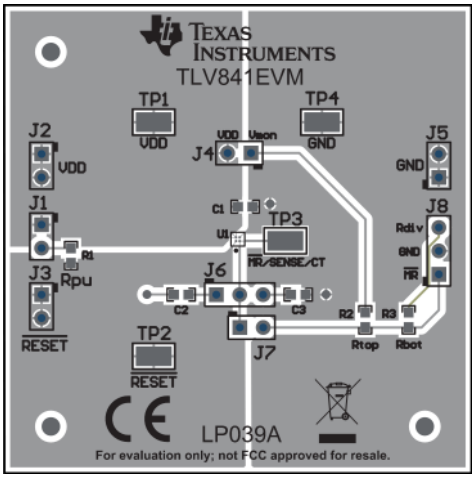

Figure 2-4. Layout—Top

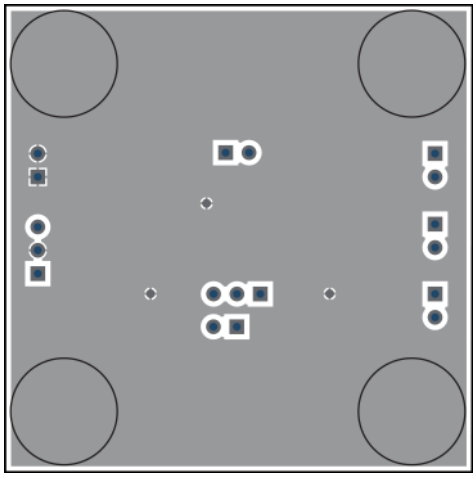

Figure 2-5. Layout—Bottom

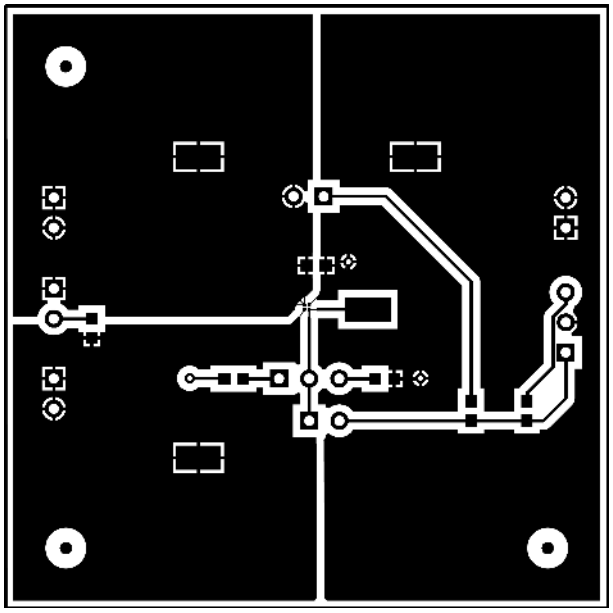

Figure 2-6. Top Layer

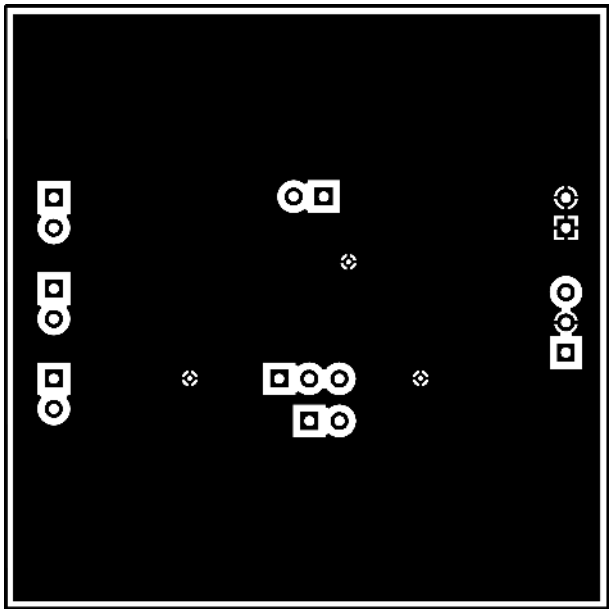

Figure 2-7. Bottom Layer

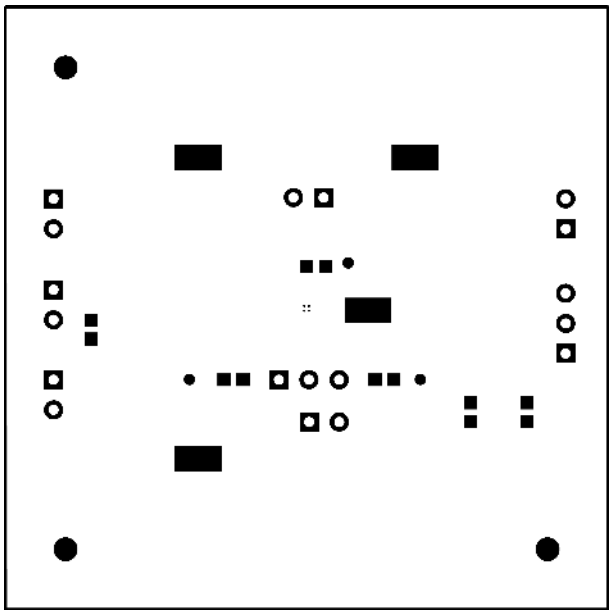

Figure 2-8. Top Solder Mask

3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 3-1 lists the test points and functional descriptions. All TLV841 pins have a corresponding test point to the EVM. These test points are located close to the pins for more accurate measurements.

Table 3-1. Test Points

TEST POINT NUMBER	TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
TP1	VDD	Connection to VDD pin	Allows the user to monitor the VDD pin. The VDD pin connects to the input power supply.
TP2	$\overline{\text{RESET}}$	Connection to $\overline{\text{RESET}}$ pin	Allows the user to monitor the $\overline{\text{RESET}}$ output pin.
TP3	$\overline{\text{MR}}$, SENSE, CT	Connect to SENSE pin (variant option #1) Connect to $\overline{\text{MR}}$ pin (variant option #2) Connect to CT pin (variant option #3)	Depending on which variant option is on the EVM board, the EVM allows the user to connect to: • SENSE pin. The SENSE pin is the voltage that will be monitored by TLV841S • $\overline{\text{MR}}$ pin. The $\overline{\text{MR}}$ (Manual Reset) pin, when pulled to a logic low allows the user to assert a reset signal on the $\overline{\text{RESET}}$ output pin. • CT pin. Allows the user to monitor the CT pin. The CT capacitor sets the time delay of the $\overline{\text{RESET}}$ output.
TP4	GND	Connection to GND pin.	Allows the user to connect to the ground plane.

3.2 EVM Jumpers

Table 3-2 lists the jumpers on the TLV841EVM. As ordered, the EVM will have eight (8) jumpers and five (5) shunts installed.

Table 3-2. List of Onboard Jumpers

JUMPER	JUMPER CONFIGUATION	DESCRIPTION
J1	Shunted	Connect a shunt to jumper J1 to use R1 as the pull-up resistor on the output $\overline{\text{RESET}}$ pin.
J2	N/A	Both pins on J2 are connected together. Connect either pin on jumper J2 to the input power supply.
J3	N/A	Both pins on J3 are connected together. Use either pin on jumper J3 to monitor the output $\overline{\text{RESET}}$ pin.
J4	Shunted	Connect a shunt to jumper J4 to short V_{mon} to VDD
J5	N/A	Both pins on J5 are connected together. Connect either pin on jumper J5 to connect to ground.
J6	Open (Default)	For TLV841C: If no shunt is placed on J6, the reset time delay t_D defaults to the minimum $\overline{\text{RESET}}$ time delay set internally by the TLV841C.
	Pin 1 [C2] to Pin 2 [CT]	For TLV841C: Connect a shunt to jumper J6 for different $\overline{\text{RESET}}$ time delay configurations.
		OPTIONAL: For TLV841S: Jumper J6 allows the user the option to connect C2 to the SENSE input, as a bypass capacitor, to reduce the sensitivity of transient voltages on the monitored signal. Connecting C2 to the SENSE input will affect the timing specs such as reset time delay t_D.
	Pin 2 [CT] to Pin 3 [C3]	For TLV841C: Connect a shunt to jumper J6 for different $\overline{\text{RESET}}$ time delay configurations.
		OPTIONAL: For TLV841S: Jumper J6 allows the user the option to connect C3 to the SENSE input, as a bypass capacitor, to reduce the sensitivity of transient voltages on the monitored signal. Connecting C3 to the SENSE input will affect the timing specs such as reset time delay t_D.
J7	Shunted Pin 1 to Pin 2	For TLV841S and TLV841M: Connect a shunt to jumper J7 to connect different configurations (Rdiv or $\overline{\text{MR}}$) from J8.
		For TLV841C: Remove shunt to jumper J7 for this option.
J8	Open Pin 1 [$\overline{\text{MR}}$] to Pin 2 [GND]	Connect the shunt to jumper J8 for different configurations. Connect the shunt from $\overline{\text{MR}}$ (Manually Reset) and to GND.
	Shunted (Default) Pin 2 [GND] to Pin 3 [Rdiv]	Connect the shunt to jumper J8 for different configurations. Connect the shunt to Rdiv and GND for the voltage divider configuration.

4 EVM Setup and Operation

This section describes the functionality and operation of the TLV841EVM. The user must read the TLV841 datasheet for electrical characteristics of the device.

4.1 Input Power (V_{DD})

The VDD supply is connected through the J2 header on board. Both pins of jumper J2 are connected together where power can be applied to either pin. The TLV841S voltage range is 0.85 V to 5.5 V whereas the TLV841C and TLV841M has a voltage range of 0.7 V to 5.5 V for the open-drain (DL) and push-pull (PL) active-low variants. For all push-pull active-high (PH) variants, the voltage range is 1 V to 5.5 V.

4.2 Monitoring Voltage on SENSE Pin (TLV841S)

The TLV841S device variant option monitors the voltage via the SENSE pin. The user can connect to the SENSE pin using TP3. The TLV841EVM provides two options for voltage monitoring.

1. Monitor VDD: VDD can be monitored by connecting the shunt to jumper J4 which creates a short and makes V_{mon} = VDD

2. Voltage divider for V_{mon}: V_{mon} connects to the SENSE pin through a voltage divider. To use this voltage divider, connect the shunt to jumper J8 (pin 3 [Rdiv] to pin 2 [GND]). This voltage divider can be adjusted to monitor any voltage above the V_{IT-}, which is 0.505 V, for the default device **TL841SADL01YBHR**. (See Table 4-1 for information on the default EVM threshold voltage values.)

OPTIONAL: Although not required in most cases, for noisy applications, the TLV841EVM contains jumper J6 (Jumper J6 is meant for TLV841C option) that allows the user the flexibility to add a bypass capacitor C2 or C3 on the SENSE input. Adding a bypass capacitor at the SENSE input will help reduce the sensitivity to transient voltages on the monitored signal but affect the timing specs such as increasing the reset time delay t_D.

Table 4-1. Nominal Input Threshold Voltage

DEVICE	V_{IT-}	V_{IT+}	V_{mon} NEGATIVE-GOING THRESHOLD VOLTAGE	V_{mon} POSITIVE-GOING THRESHOLD VOLTAGE
TLV841SADL01, R1 = 47.5 kΩ, R2 = 10 kΩ (x0.174 Voltage Divider Ratio)	0.505 V	0.530 V	2.90 V	3.05 V

Upon start-up, the TLV841 requires VDD to be above V_{POR} = 0.7 V before the $\overline{\text{RESET}}$ output is in the correct logic state. The TLV841 has built-in glitch immunity so voltage transients on VDD or SENSE are ignored if the pulse duration is 10 µs or less as shown in Figure 4-1. The glitch immunity specification depends on the amplitude of the voltage transient and the operating conditions. Please see the Glitch Immunity specification in the Timing Requirements section of the TLV841 datasheet for more detailed information.

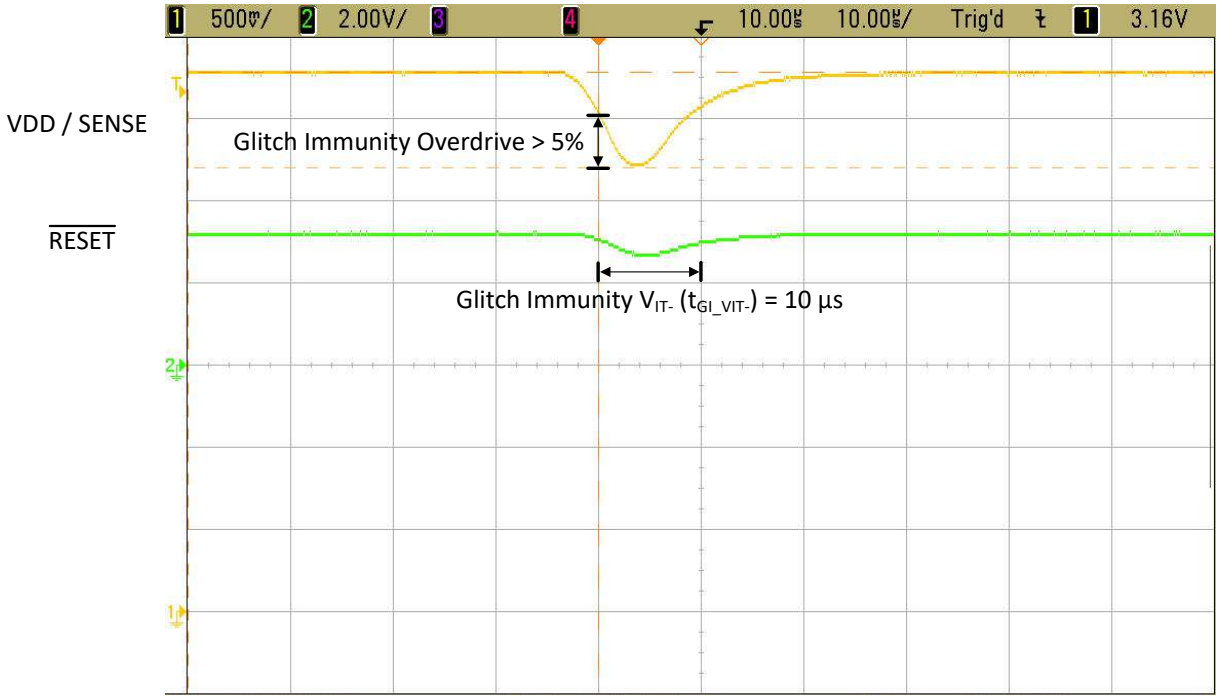

Figure 4-1. TLV841EVM Glitch Immunity

4.3 Monitoring Voltage on VDD (TLV841M and TLV841C)

The TLV841M and TLV841C device variant options monitor the voltage via the VDD pin. The EVM provides jumper J2 and test point TP1 for connecting the power supply input to the VDD pin. If the voltage on this pin drops below V_{IT-}, $\overline{\text{RESET}}$ is asserted low. The VDD pin is connected internally to a comparator through an internal resistor divider at the positive input and the negative input is connected to an internal reference. The internal resistor divider is set to provide the input voltage threshold to cause a reset, V_{IT-}, that corresponds to the chosen voltage option variant. Please see the Device Comparison Table in the TLV841 datasheet for more information on the different voltage device variants.

4.4 Manual Reset ($\overline{\text{MR}}$) (TLV841M)

The TLV841M device variant option offers a Manual Reset ($\overline{\text{MR}}$) pin that is utilized via jumper J8 (short pin 1 [$\overline{\text{MR}}$] to pin 2 [GND]). If a shunt jumper is placed on jumper J8, the $\overline{\text{RESET}}$ pin is asserted and forced into a low state. After the shunt jumper is removed and VDD is above its reset threshold, $\overline{\text{MR}}$ returns to a logic high due to the internal pull-up resistor, and $\overline{\text{RESET}}$ is de-asserted to a logic high after the user-defined delay expires. If jumper J8 is left floating, the device operates normally as the $\overline{\text{MR}}$ pin defaults to a logic high via internal pull-up resistor. Pin 1 of jumper J8 can also be connected to a control signal to set the logic level on $\overline{\text{MR}}$ pin. If pin 1 on jumper J8 is a logic low, the device asserts a reset. There is also test point TP3 connected directly to the $\overline{\text{MR}}$ pin in case the user wants to monitor the $\overline{\text{MR}}$ pin.

4.5 Reset Output ($\overline{\text{RESET}}$)

The TLV841EVM comes populated with **TL841SADL01YBHR** device variant which has an open-drain, active-low output topology for the $\overline{\text{RESET}}$ pin. The other device variants provide different output topolgies and can be used on this EVM. Note: if using a TLV841 device variant with push-pull output topology, the pull-up resistor must be disconnected by leaving jumper J1 open. The TLV841EVM provides an option to apply a separate pull-up voltage by leaving jumper J1 open and connecting the pull-up voltage to pin 2 [V_{PU}] of jumper J1. The TLV841EVM provides jumper J3 and test point TP2 that is connected directly to the $\overline{\text{RESET}}$ pin for monitoring and/or interfacing to other devices.

The reset signal will be asserted low when:

- The voltage on the SENSE pin falls below V_{IT-} for the TLV841S version. See Figure 4-2
- The $\overline{MR}$ pin is pulled low or when the voltage on the VDD pin falls below V_{IT-} for the TLV841M version
- The voltage on the VDD pin falls below V_{IT-} for the TLV841C version.
- For TLV841M and TLV841C device variant option, the propagation detect delay t_{P_HL} when VDD goes below V_{IT-}.

For TLV841M ($\overline{MR}$ pin > V_{OH}) and TLV841C, when the voltage on VDD or when TLV841S SENSE pin monitoring voltage rises above (V_{IT+} + V_{HYS}), the output reset pin will de-assert and remain de-asserted until a reset condition occurs again. Please refer to TLV841 datasheet for more information on the $\overline{RESET}$ output and how it reacts to start up conditions and minimum values of VDD.

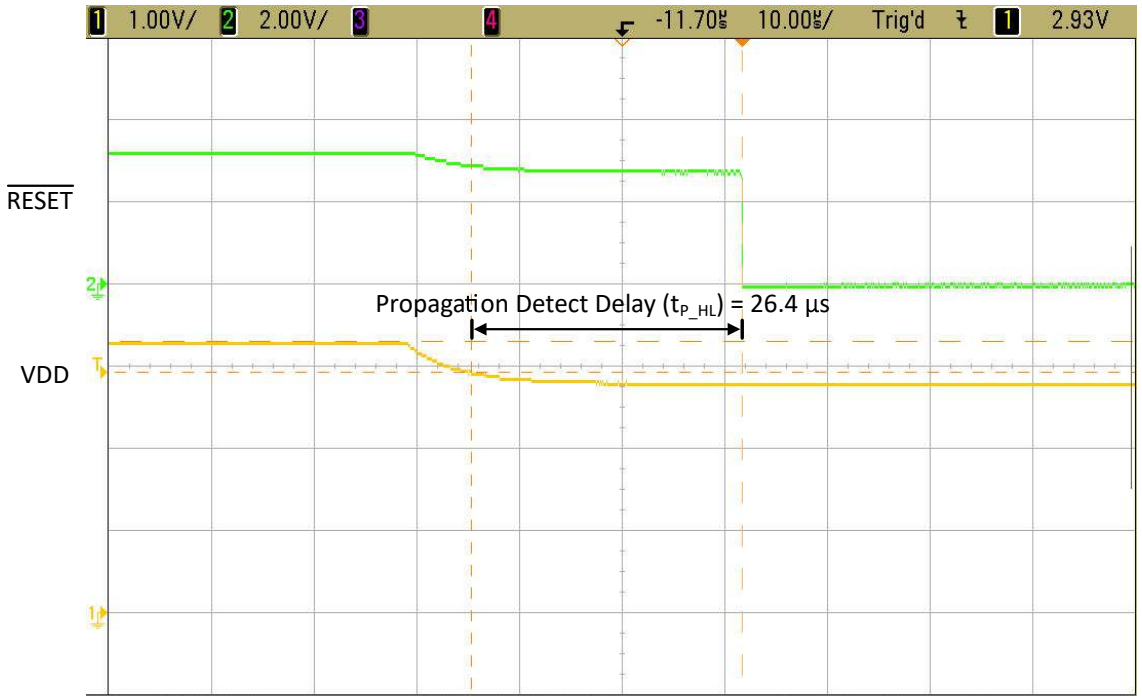

Figure 4-2. TLV841EVM $\overline{RESET}$ Propagation Detect Delay

4.6 Reset Time Delay Programming (Program t_D via C_T) (TLV841C)

The TLV841C device variant has two options for setting the $\overline{RESET}$ time delay: connect CT pin to a capacitor to GND, or leave CT pin floating. The reset time delay can be set to a minimum value of 80 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed to any value within the range by connecting a capacitor no larger than 10 µF between CT pin and GND. The relationship between external capacitor (C_{CT_EXT}) at CT pin and the $\overline{RESET}$ time delay is given by Equation 1.

$$t_D = -\ln(0.29) \times R_{CT} \times C_{CT\_EXT} + t_D \text{ (no cap)} \quad (1)$$

Equation 1 is simplified to Equation 2 by plugging R_{CT} and $T_{D(no\ cap)}$ given in the *Electrical Characteristics Table* in TLV841 datasheet.

$$t_D = 618937 \times C_{CT\_EXT} + 80\ \mu s \quad (2)$$

Equation 3 solves for external capacitor value (C_{CT_EXT})

$$C_{CT\_EXT} = (t_D - 80\ \mu s) \div 618937 \quad (3)$$

The recommended maximum delay capacitor for the TLV841C is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

The TLV841EVM provides jumper J6 to configure the CT pin and test point TP3 to monitor the CT pin. Place a shunt jumper on pin 1 (left pin) and pin 2 (middle pin) of jumper J6 to connect CT to delay capacitor C2. This connects the CT pin to a 0.01 µF capacitor to set the $\overline{\text{RESET}}$ delay (t_D) to ~6.2 ms. Place a shunt between pin 2 (middle pin) and pin 3 (right pin) of jumper J6 to connect CT to delay capacitor C3. This connects the CT pin to a 0.1 µF capacitor to set the $\overline{\text{RESET}}$ delay (t_D) to ~61.9 ms. By removing the shunt jumper from jumper J6, the $\overline{\text{RESET}}$ time delay defaults to the minimum value of 80 µs or less. If using a different delay capacitor, the capacitor must be ≥ 100 pF to be recognized.

For the TLV841M / TLV841S variant or TLV841C where C_T is floating, Figure 4-3 shows the typical reset delay time. Depending on how much VDD deviates from the specified threshold, the typical reset delay value (~40 µs) may be shorter or longer.

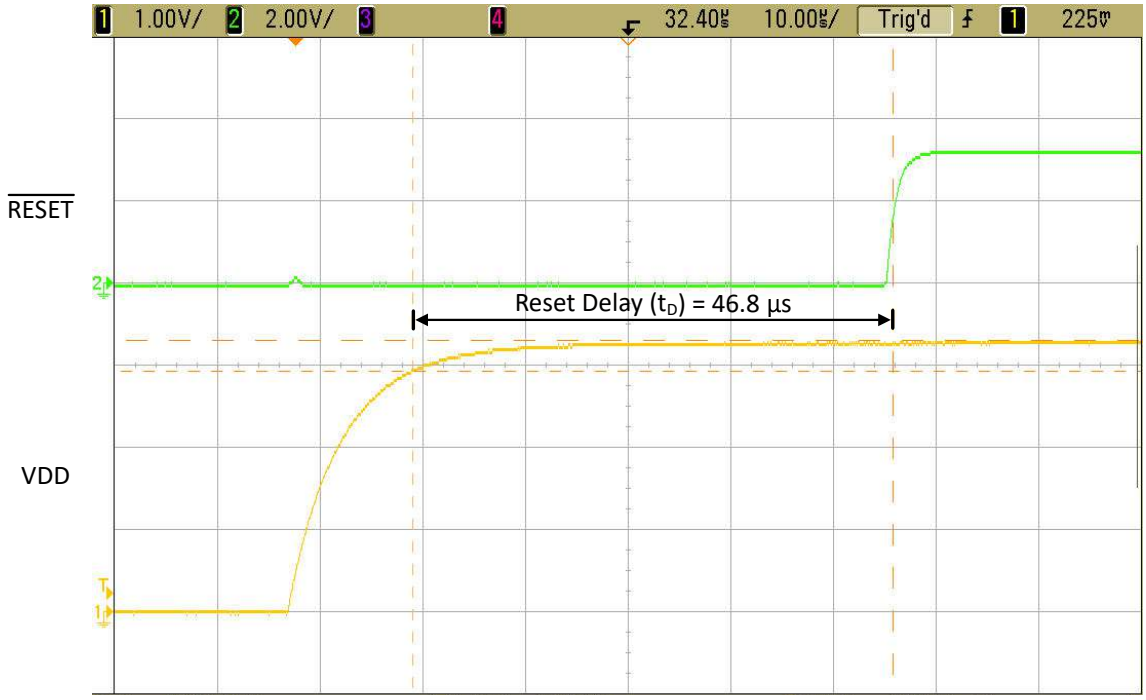

Figure 4-3. TLV841EVM $\overline{\text{RESET}}$ Delay Time (t_D) for TLV841S/M or for TLV841C where C_T Pin Is Floating

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2021) to Revision A (June 2021)	Page
• Updated supply voltage from 6 V to 5.5 V	2
• Updated schematic	5
• Included supply voltage range for TLV841C and TLV841M with open-drain and push-pull outputs	11

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265