To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD8828A

7500 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8828A is a high-speed and high sensitive color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD8828A has 3 rows of 7500 pixels, and it is a 2-output/color type CCD sensor with 2 rows/color of charge transfer register, which transfers the photo signal electrons of 7500 pixels separately in odd and even pixels.

Therefore, it is suitable for 600 dpi/A3 high-speed color digital copiers, color scanners and so on.

FEATURES

- Valid photocell : 7500 pixels × 3
- Photocell pitch : 4.7 μm
- Line spacing : 37.6 μm (8 lines) Red line-Green line, Green line-Blue line
- Color filter : Primary colors (red, green, and blue), pigment filter
  Light resistance is 10^7 lx•hour with standard sunlight and ultraviolet cut filter (L40)
- Resolution : 24 dot/mm A3 (297 × 420 mm) size (shorter side)
- Data rate : 40 MHz MAX. (20 MHz/ch max.)
- Output type : 2 outputs in phase/color
- Power supply : +10 V
- Drive clock level : CMOS output under 5 V operation
- On-chip circuits : Reset feed-through level clamp circuit
  Voltage amplifiers

ORDERING INFORMATION

	Part Number	Package
<R>	μPD8828AD-A	CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

Remark The μPD8828AD-A is a lead-free product.

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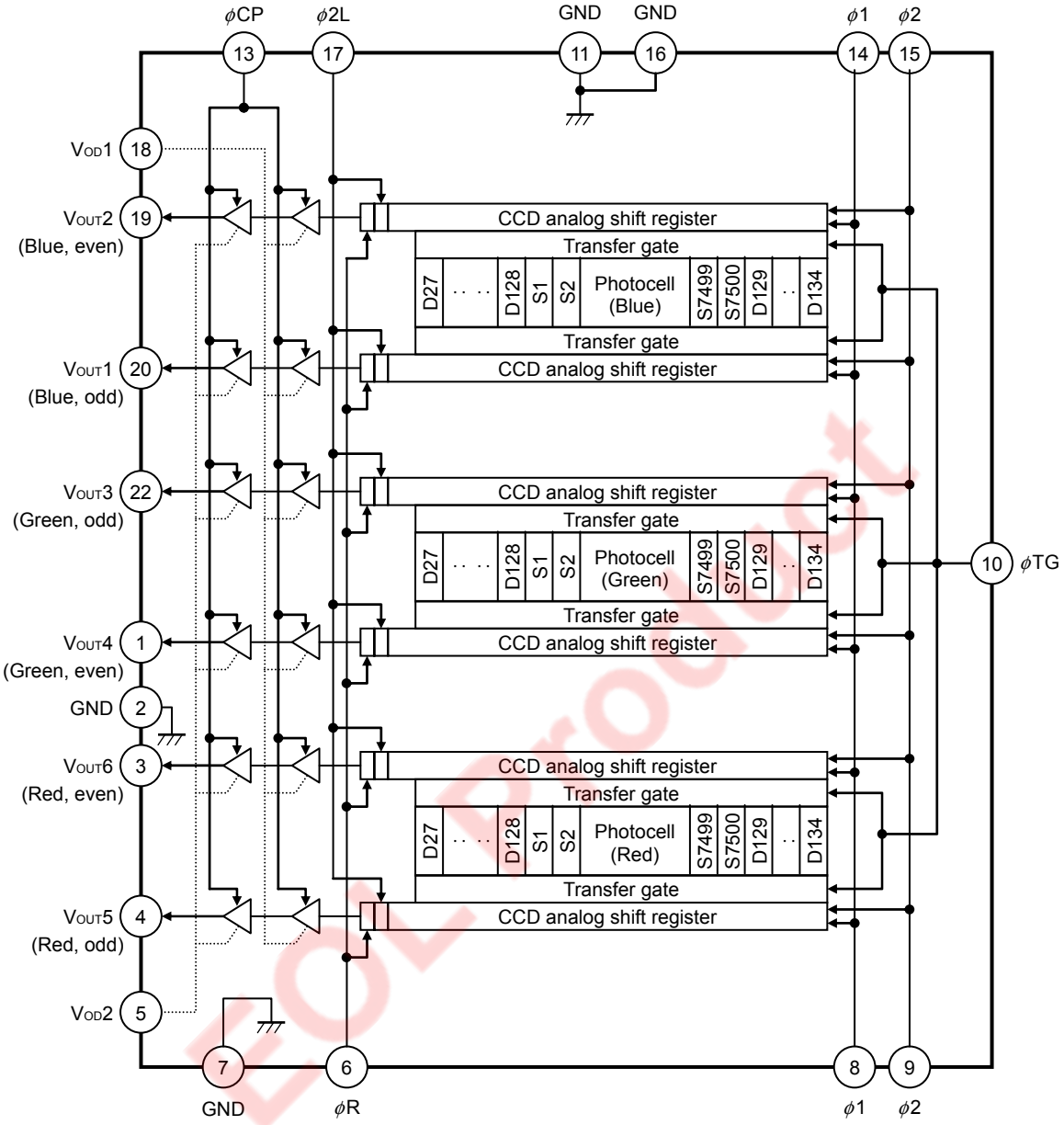
Date Published October 2006 NS CP (K)
Printed in Japan

The mark " <R>" shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

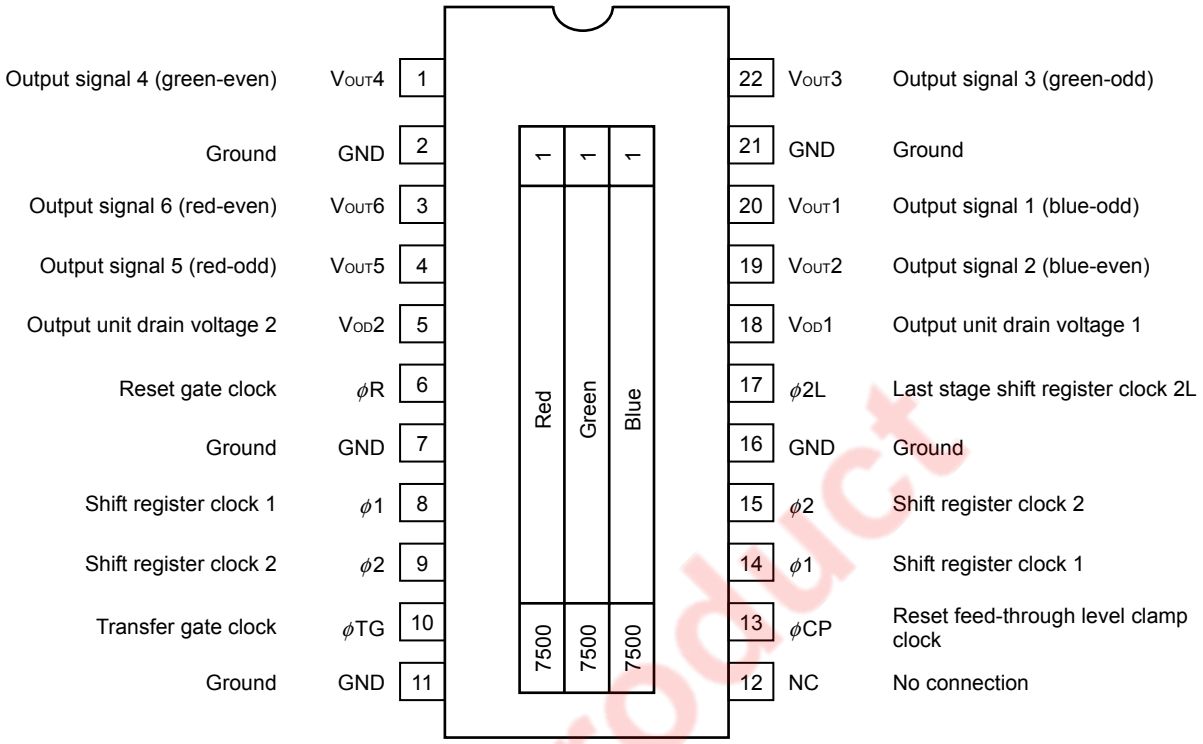
BLOCK DIAGRAM



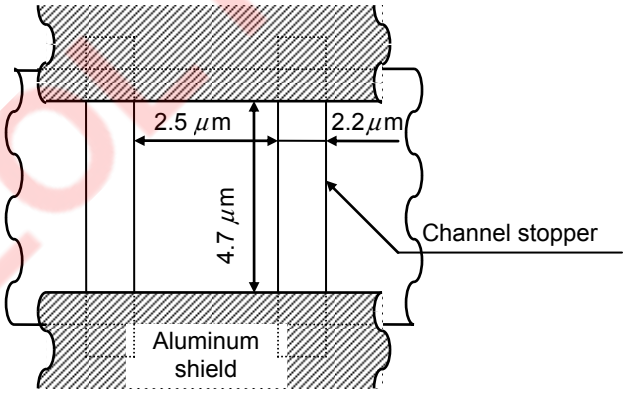
PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

μPD8828AD-A



PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	$V_{OD}1$, $V_{OD}2$	–0.3 to +12.0	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	–0.3 to +8.0	V
Last stage shift register clock voltage	$V_{\phi 2L}$	–0.3 to +8.0	V
Reset gate clock voltage	$V_{\phi R}$	–0.3 to +8.0	V
Reset feed-through level clamp clock voltage	$V_{\phi CP}$	–0.3 to +8.0	V
Transfer gate clock voltage	$V_{\phi TG}$	–0.3 to +8.0	V
Operating ambient temperature Note	T_A	0 to +60	˚C
Storage temperature	T_{stg}	–40 to +100	˚C

Note The operating ambient temperature is defined as an atmosphere temperature in a point 10 mm away on the substrate, and 10 mm away from the short side of package 1 pin. Use at the condition without dewy condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	$V_{OD}1$, $V_{OD}2$	9.5	10.0	10.5	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$	4.75	5.0	6.0	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$	–0.3	0.0	+0.5	V
Last stage shift register clock high level	$V_{\phi 2LH}$	4.75	5.0	6.0	V
Last stage shift register clock low level	$V_{\phi 2LL}$	–0.3	0.0	+0.5	V
Reset gate clock high level	$V_{\phi RH}$	4.75	5.0	5.5	V
Reset gate clock low level	$V_{\phi RL}$	-0.3	0.0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CPH}$	4.75	5.0	6.0	V
Reset feed-through level clamp clock low level	$V_{\phi CPL}$	–0.3	0.0	+0.5	V
Transfer gate clock high level Note	$V_{\phi TGH}$	4.75	$V_{\phi 1H}$	$V_{\phi 1H}$	V
Transfer gate clock low level	$V_{\phi TGL}$	–0.3	0.0	+0.5	V
Shift register clock amplitude	$V_{\phi 1p\text{-}p}$, $V_{\phi 2p\text{-}p}$	4.75	5.0	6.3	V
Last stage shift register clock amplitude	$V_{\phi 2Lp\text{-}p}$	4.75	5.0	6.3	V
Reset gate clock amplitude	$V_{\phi Rp\text{-}p}$	4.75	5.0	6.3	V
Reset feed-through level clamp clock amplitude	$V_{\phi CPp\text{-}p}$	4.5	5.0	6.3	V
Transfer gate clock amplitude	$V_{\phi TGp\text{-}p}$	4.75	5.0	6.3	V
Data rate	$2 \times f_{\phi R}$	0.2	2	40	MHz

Note When Transfer gate clock high level ($V_{\phi TGH}$) is higher than shift register clock high level ($V_{\phi 1H}$), image lag can increase.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = +10 V, $f_{\phi R}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms, input clock = 5 V_{p-p}
light source: 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm)+ HA-50 (heat absorbing filter, t = 3 mm) (except Response 2))

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage		Vsat		1.5	2.0	–	V
Saturation exposure	Red	SER	3200K+C500S+HA50	–	0.17	–	lx•s
	Green	SEG		–	0.2	–	lx•s
	Blue	SEB		–	0.37	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1 V	–	6.0	18.0	%
Average dark signal		ADS	Light shielding	–	1.0	5.0	mV
Dark signal non-uniformity		DSNU	Light shielding	–	2.0	10.0	mV
Power consumption 1		$P_{OD}1$		–	130	150	mW
Power consumption 2		$P_{OD}2$		–	340	400	mW
Output impedance		Z_O		–	0.2	0.4	kΩ
Response 1	Red	R_R	3200K+C500S+HA50	8.47	12.1	15.73	V/lx•s
	Green	R_G		6.93	9.9	12.87	V/lx•s
	Blue	R_B		3.78	5.4	7.02	V/lx•s
Response 2 (corresponding value from Response 1)	Red	R_R	A light source+CM500S	6.30	9.0	11.70	V/lx•s
	Green	R_G		5.81	8.3	10.79	V/lx•s
	Blue	R_B		2.66	3.8	4.94	V/lx•s
Response peak	Red			–	610	–	nm
	Green			–	535	–	nm
	Blue			–	460	–	nm
Image lag		IL	V_{OUT} = 1 V	–	3.0	5.0	%
Offset level		V_{OS}		3.9	4.9	5.9	V
Output fall delay time Note		t_d		13	15	17	ns
Register imbalance		RI	V_{OUT} = 1 V	–	0	8	%
Total transfer efficiency		TTE	V_{OUT} = 1 V, $f_{\phi R}$ = 20 MHz	94	98	–	%
Dynamic range		DR1	V_{sat}/DSNU	–	1000	–	times
		DR2	V_{sat}/σ	–	1333	–	times
Reset feed-through noise		RFTN	Light shielding	–1000	–200	+500	mV
Light shielding random noise		σdark	Bit clamp, t17 > 8 ns	–	1.5	–	mV

Note t_d is defined as period from 10% of ϕ2L of V_{OUT}1 to V_{OUT}6, and td is reference data after V_{OUT}1 to V_{OUT}6 pins with FET proving.

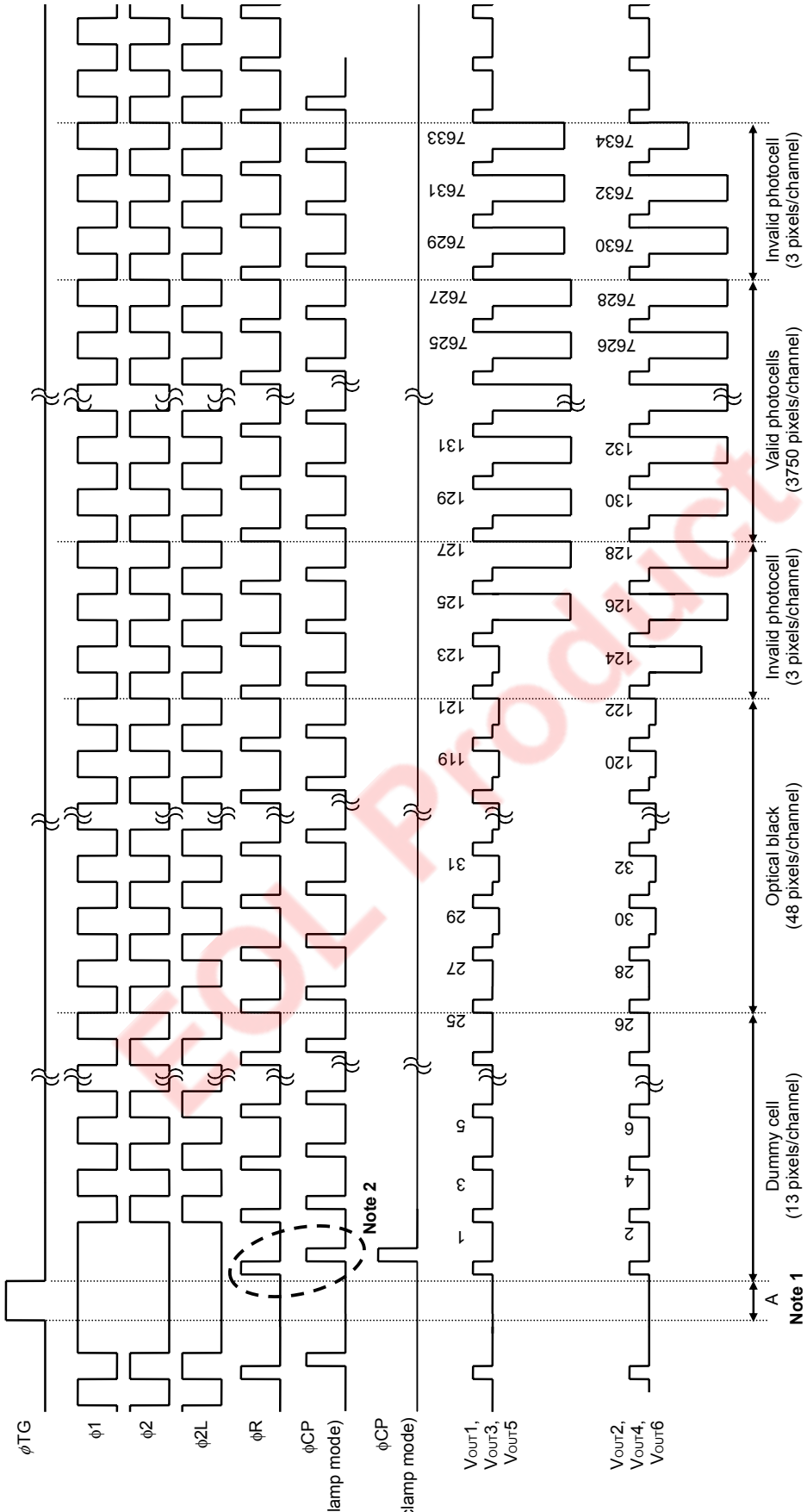
INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = +10 V)

Parameter	Symbol	Pin	Pin No	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance [Note]	$C_{\phi 1}$	ϕ1	8	360	400	440	pF
		ϕ1	14	360	400	440	pF
	ϕ1 total capacitance			720	800	880	pF
	$C_{\phi 2}$	ϕ2	9	360	400	440	pF
		ϕ2	15	360	400	440	pF
	ϕ2 total capacitance			720	800	880	pF
Last stage shift register clock pin capacitance	$C_{\phi 2L}$	ϕ2L	17	14	15	17	pF
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR	6	20	22	24	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CP}$	ϕCP	13	35	39	43	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	10	225	250	275	pF

Note $C_{\phi 1}$, $C_{\phi 2}$ are equivalent capacitance with driving device, including the co-capacitance between ϕ1 and ϕ2.

Remark Pins 8 and 14 (ϕ1), pins 9 and 15 (ϕ2) are each connected inside of the device.

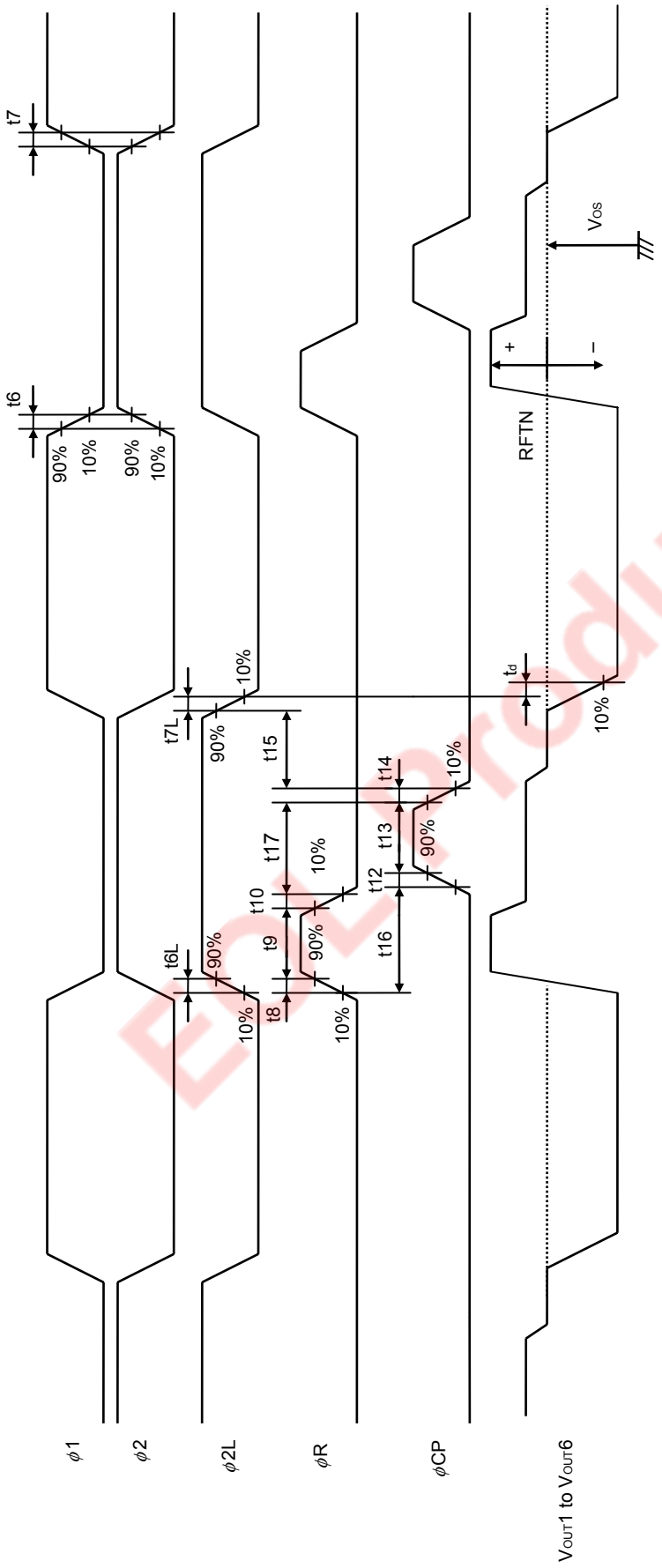
TIMING CHART 1



Notes 1. Set the φR and φCP to low level during this period (A).

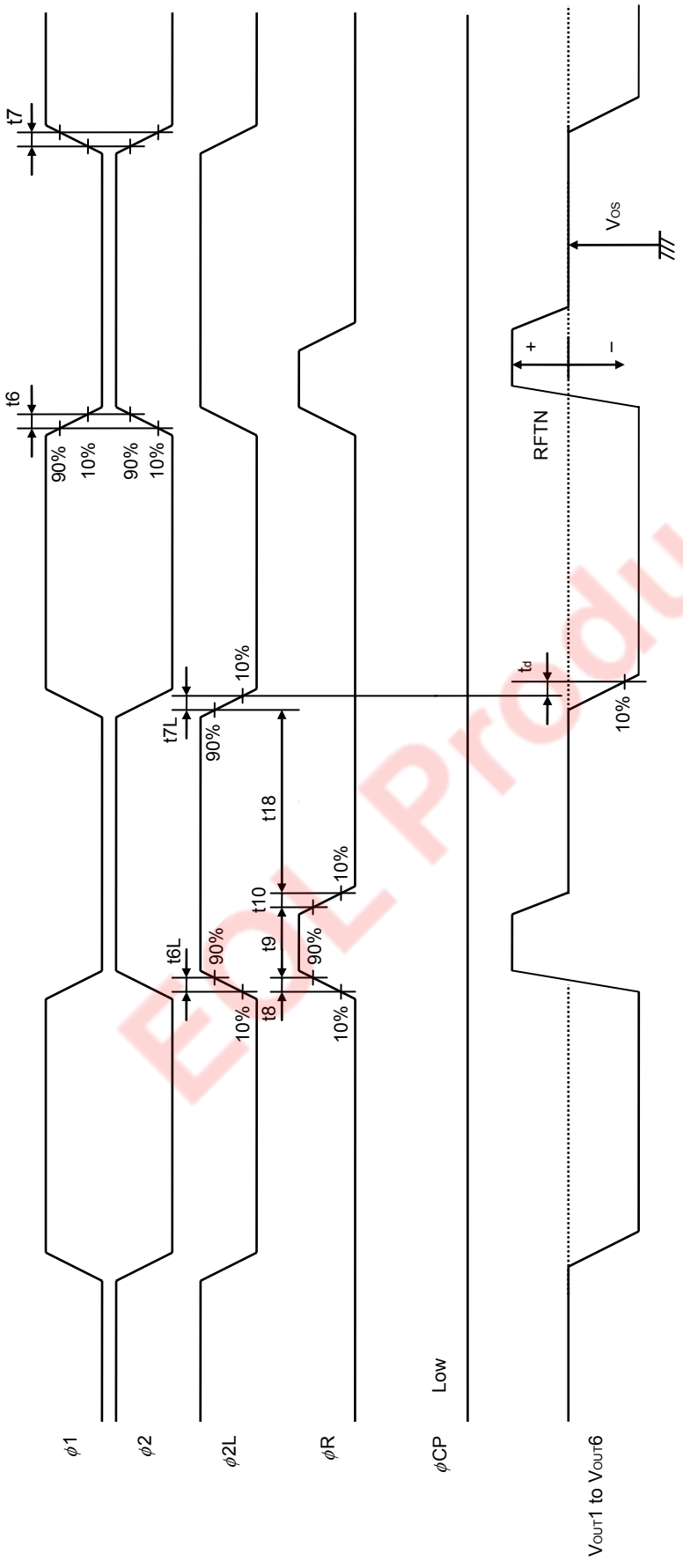
2. The φR and φCP pulses which surrounded with the dashed line are omissible at the bit clamp mode.

TIMING CHART 2 (Bit Clamp Mode)



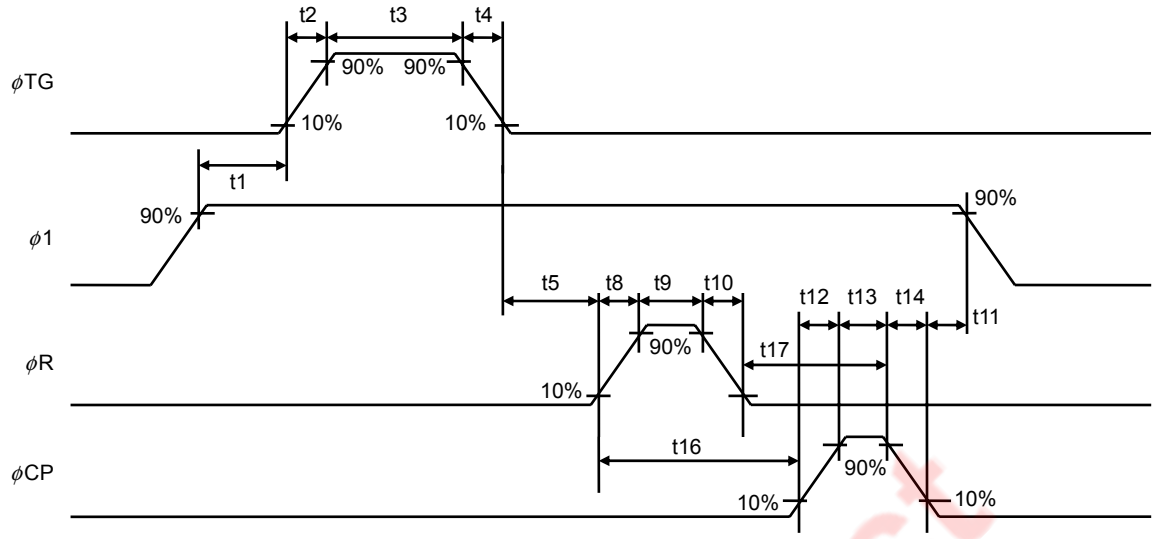
Caution "10%" and "90%" define as the clock voltage with 5 V_{p-p} condition. i.e. "10%" shows 0.5 V, "90%" shows 4.5 V

TIMING CHART 3 (Line Clamp Mode)



Caution "10%" and "90%" define as the clock voltage with 5 V_{p-p} condition. i.e. "10%" shows 0.5 V, "90%" shows 4.5 V

TIMING CHART 4 (Bit Clamp Mode, Line Clamp Mode)

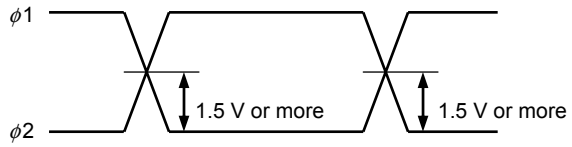


Caution "10%" and "90%" define as the clock voltage with 5 V_{p-p} condition. i.e. "10%" shows 0.5 V, "90%" shows 4.5 V

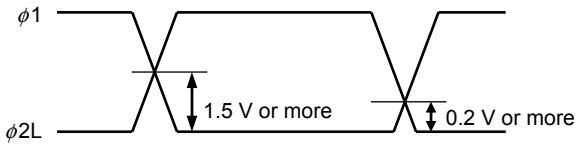
Symbol	MIN.	TYP.	MAX.	Unit
t1, t5	100	200	2000	ns
t2, t4	0	10	–	ns
t3	500	1000	10000	ns
t6, t7	0	10	–	ns
t6L, t7L	0	3	–	ns
t8, t10	0	3	–	ns
t9	10	125	–	ns
t11	0	250	–	ns
t12, t14	0	3	–	ns
t13	10	125	–	ns
t15	0	250	–	ns
t16	0	125	–	ns
t17	8	125	–	ns
t18	5	125	–	ns

Cross Points Characteristics

ϕ1, ϕ2 Cross Points

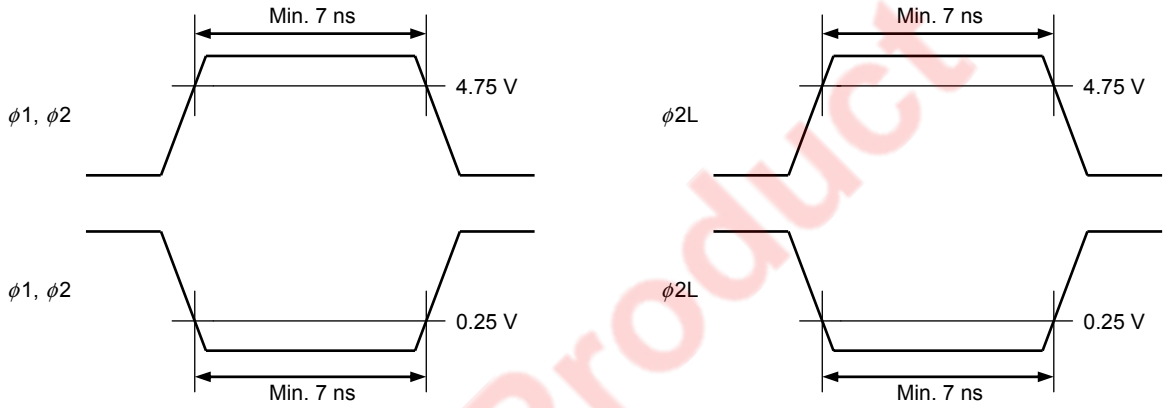


ϕ1, ϕ2L Cross Points



Remark Adjust cross points of (ϕ1, ϕ2) and (ϕ1, ϕ2L) with input resistance of each pin.

Clock High/Low Level Width Characteristics



DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : V_{sat}

Output signal voltage at which the response linearity is lost.

2. Saturation exposure : SE

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : PRNU

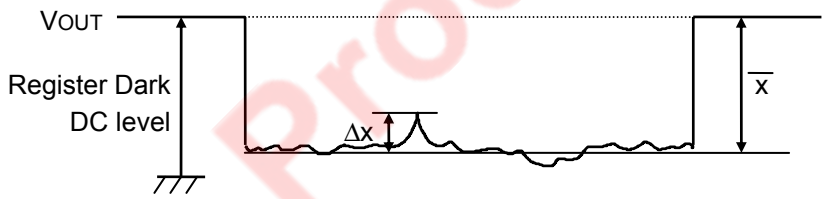
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $| x_j - \overline{x} |$

$$\overline{x} = \frac{\sum_{j=1}^{3750} x_j}{3750}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : ADS

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS\ (mV) = \frac{\sum_{j=1}^{3750} d_j}{3750}$$

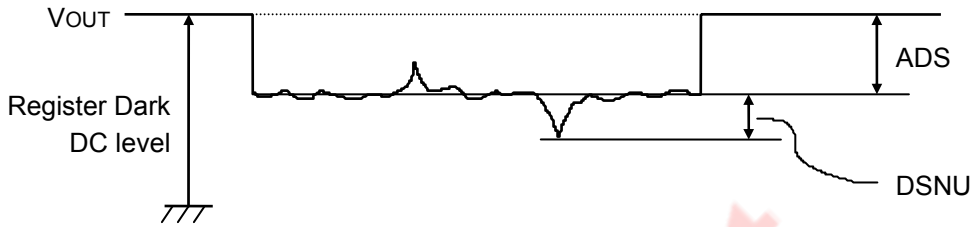
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each six of them.

DSNU (mV) : maximum of $| d_j - ADS |_{j = 1 \text{ to } 3750}$

d_j : Dark signal of valid pixel number j



6. Output impedance : Zo

Impedance of the output pins viewed from outside.

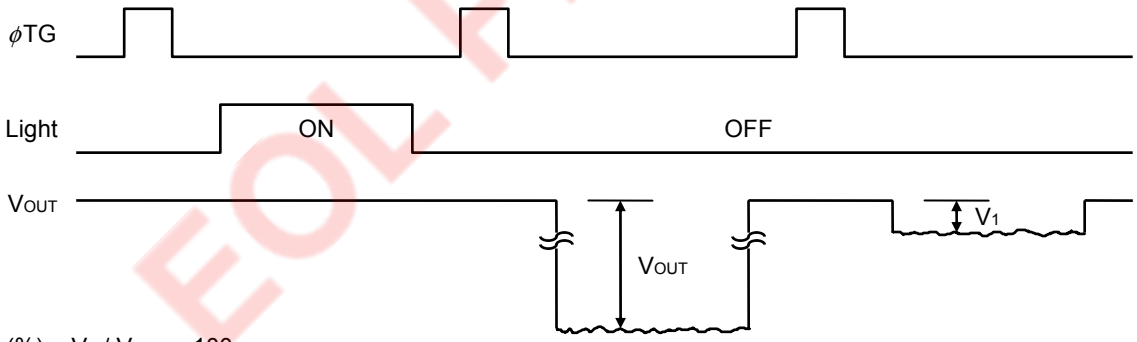
7. Response : R

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : IL

The rate between the last output voltage and the next one after read out the data of a line.



$IL (\%) = V_1 / V_{OUT} \times 100$

9. Register imbalance : RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}}(V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels

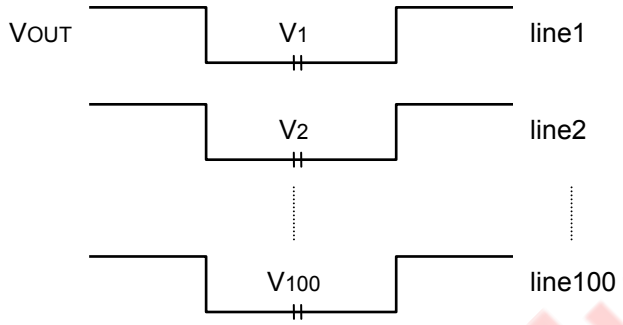
V_j : Output voltage of each pixel

10. Light shielding random noise : σdark

Light shielding random noise σdark is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

$$\sigma\,(\mathrm{mV}) = \sqrt{\frac{\sum_{i=1}^{100}(V_i - \overline{V})^2}{100}}, \qquad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

V_i :A valid pixel output signal among all of the valid pixels for each color.

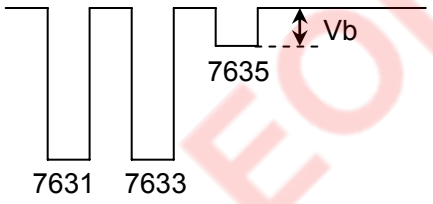


This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling)

11. Total transfer efficiently : TTE

The total transfer rate of CCD analog shift register. This is calculated by the following formula, it is defined by each odd output.

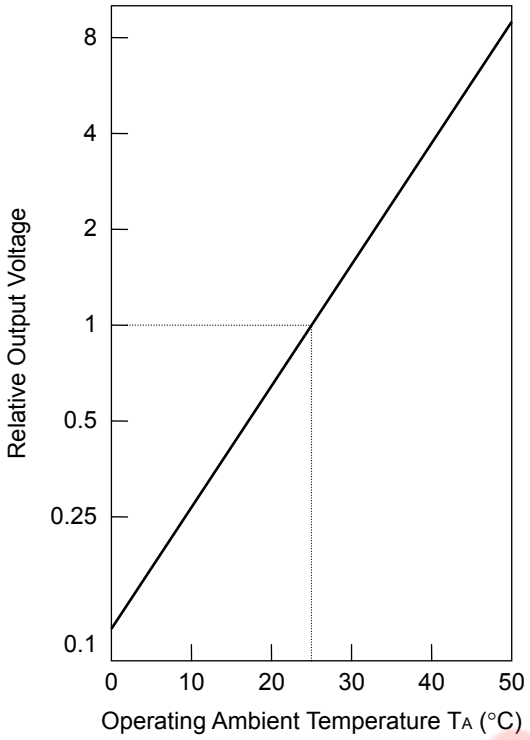
TTE(%) = (1-Vb/average output of all the valid pixels) × 100



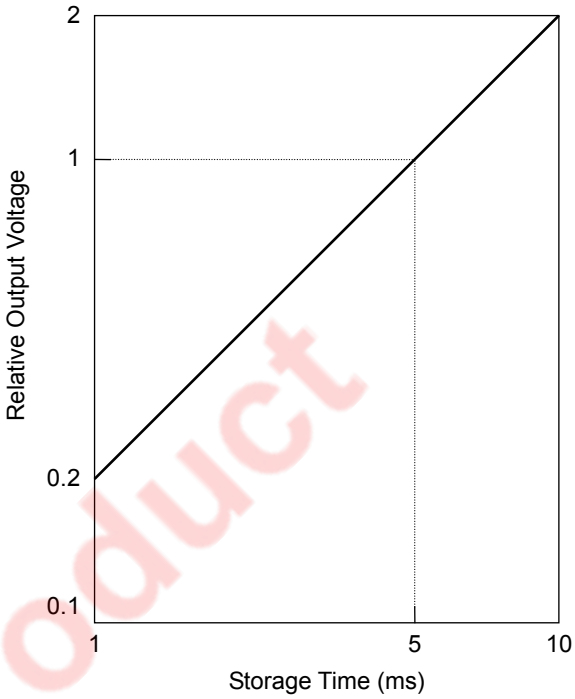
Vb: The spilt pixel output (7635th pixel)

STANDARD CHARACTERISTIC CURVES (Reference Value)

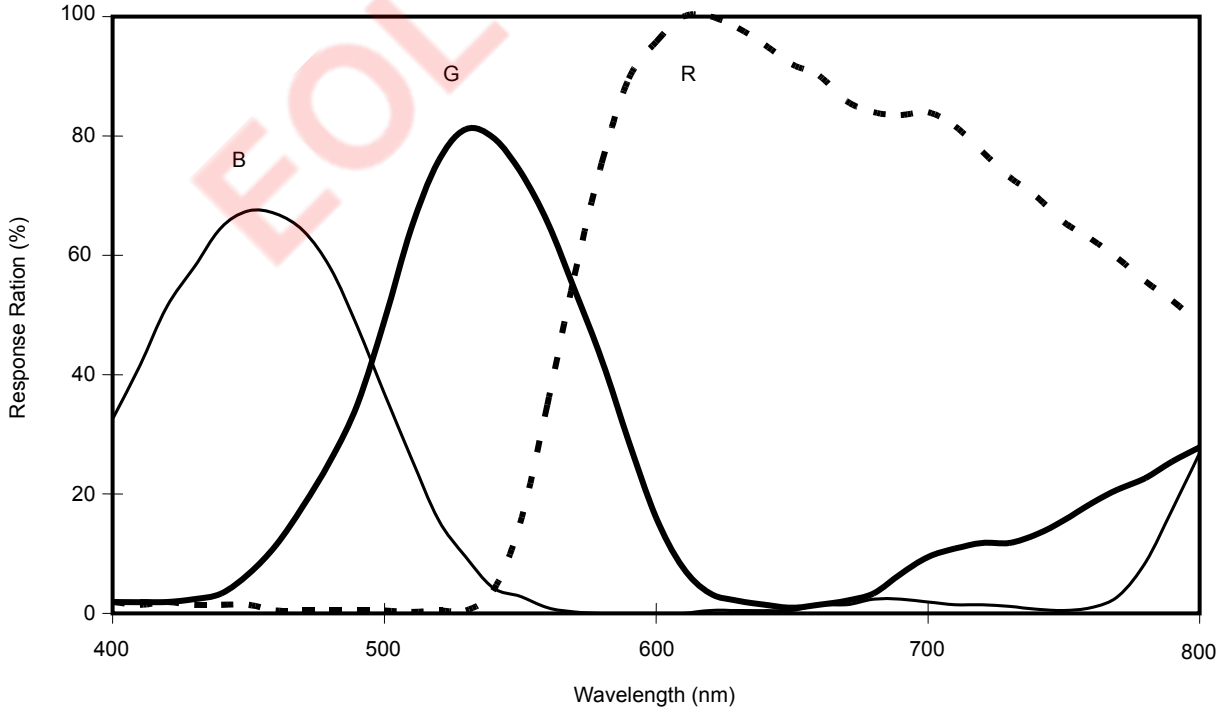
DARK OUTPUT TEMPERATURE CHARACTERISTIC



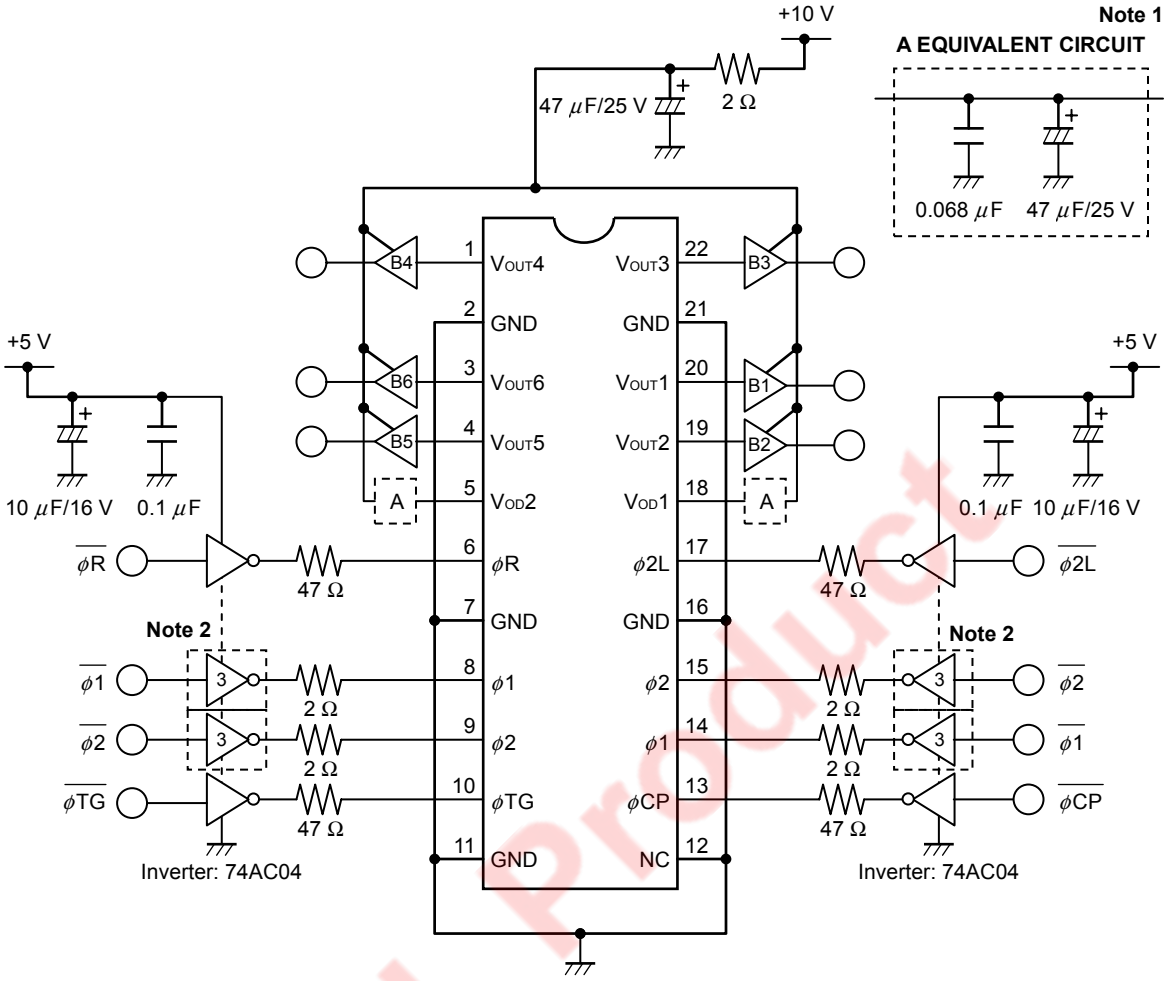
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) (T_A = 25°C)



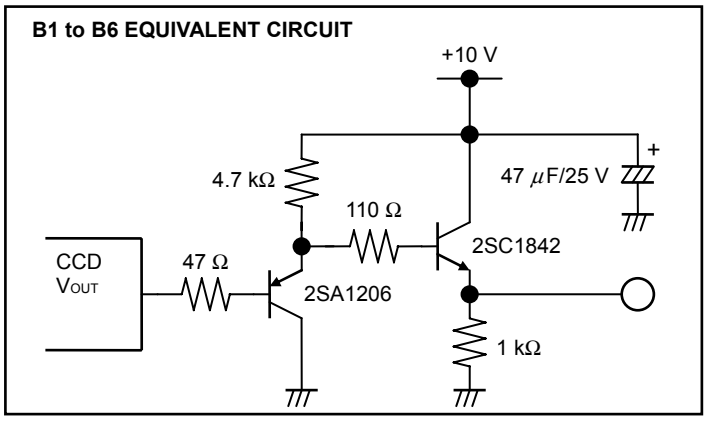
APPLICATION CIRCUIT EXAMPLE



Notes 1. Arrange the circuit A near each power supply terminal ($V_{OD}1$, $V_{OD}2$) to prevent the interference between $V_{OD}1$ and $V_{OD}2$.

2. Connects the 3 inverters for each $\phi 1$ and $\phi 2$ pin.

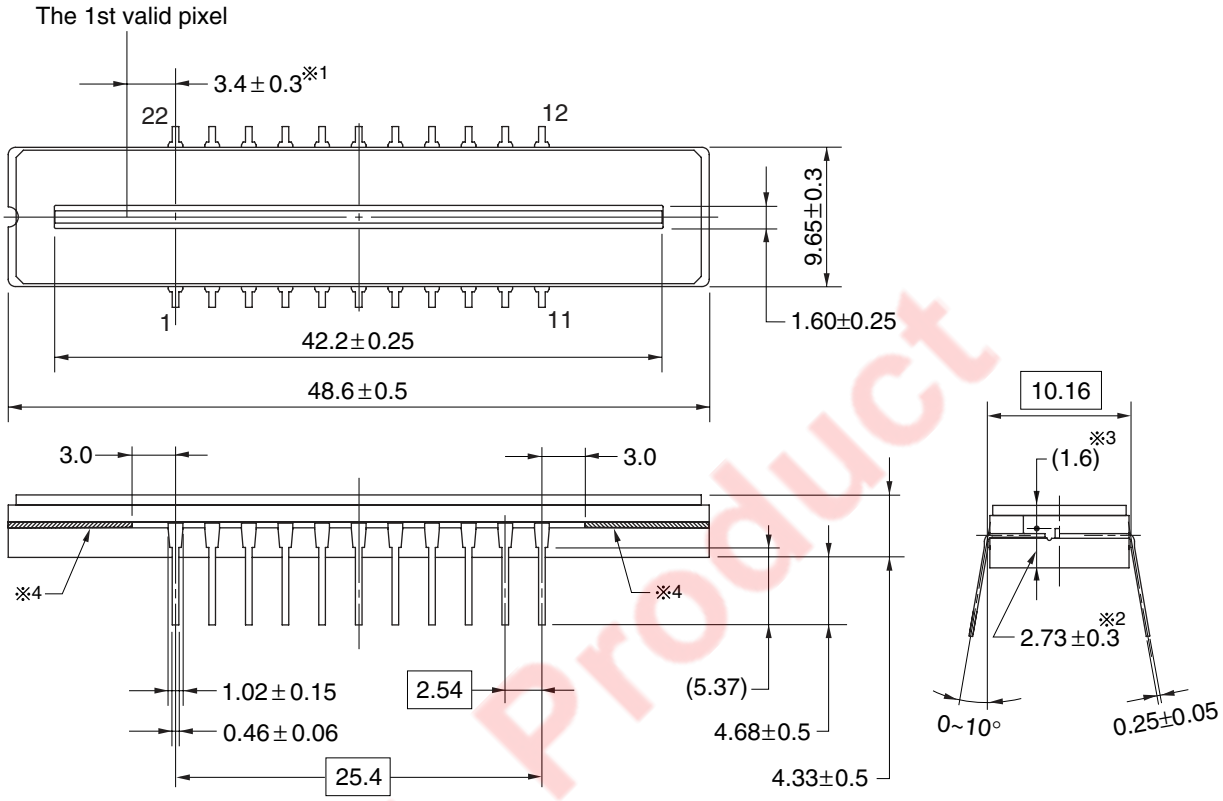
Caution Connect the No connection pins (NC) to GND.



PACKAGE DRAWING

μPD8828AD-A
CCD LINEAR IMAGE SENSOR 22-PIN CERAMIC DIP (CERDIP) (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	47.5×9.25×0.7	1.5

※1 1st valid pixel ↔ Center of pin 1
※2 Photosensitive surface of CCD chip ↔ Bottom of package
※3 Photosensitive surface of CCD chip ↔ Top of glass cap
※4 The shaded portions are overflow prohibited area of the seal glass.

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8828AD-A: CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature: 380°C or below, Heat time: 3 seconds or less (per pin).

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.

2. Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES ON HANDLING THE PACKAGES

① MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with glass cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

② GLASS CAP

Don't either touch glass cap surface by hand or have any object come in contact with glass cap surface. Care should be taken to avoid mechanical or thermal shock because the glass cap is easily to damage. For dirt stuck through electricity ionized air is recommended.

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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