

# BLP9H10S-850AVT

Power LDMOS transistor

Rev. 1 — 25 May 2022

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

850 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 617 MHz to 960 MHz.

**Table 1. Typical performance 942 MHz**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty test circuit.  $V_{DS} = 50\text{ V}$ ;  $I_{Dq} = 700\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.083\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	925 to 960	50	50.8	17.5	51.7	-35.6 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

**Table 2. Typical performance 806 MHz**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty test circuit.  $V_{DS} = 48\text{ V}$ ;  $I_{Dq} = 820\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.25\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	791 to 821	48	50.8	18.6	52.7	-32.6 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

**Table 3. Typical performance 698 MHz**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty test circuit.  $V_{DS} = 48\text{ V}$ ;  $I_{Dq} = 720\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.25\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	616 to 746	48	49.5	18.5	48.5	-36.9 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

**Table 4. Typical performance 859 MHz**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty test circuit.  $V_{DS} = 48\text{ V}$ ;  $I_{Dq} = 740\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.4\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	758 to 960	48	49.6	18.3	45.2	-38.4 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 617 MHz to 960 MHz frequency range

## 2. Pinning information

Table 5. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	gate1		
2	gate2		
3	video decoupling		
4	drain2		
5	drain1		
6	video decoupling		
7	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 6. Ordering information

Type number	Package		
	Name	Description	Version
BLP9H10S-850AVT	-	overmolded plastic earless flanged package; 6 leads	OMP-1230-6F-1

## 4. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	105	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-6	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+11	V

**Table 7. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature	[1]	-	225	°C
T <sub>case</sub>	case temperature	[1]	-40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

**Table 8. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-c)</sub>	thermal resistance from junction to case	V <sub>DS</sub> = 48 V; I <sub>Dq</sub> = 720 mA (main); V <sub>GS(amp)peak</sub> = 0.25 V; T <sub>case</sub> = 80 °C		
		P <sub>L</sub> = 89 W	0.35	K/W
		P <sub>L</sub> = 112 W	0.32	K/W

## 6. Characteristics

**Table 9. DC characteristics**

T<sub>j</sub> = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 2 mA	108	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 200 mA	1.5	2.0	2.5	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 48 V; I <sub>D</sub> = 820 mA	-	2.2	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V	-	-	2.8	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; V <sub>DS</sub> = 10 V	-	33	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	280	nA
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 10 A	-	13.2	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; I <sub>D</sub> = 7.0 A	-	114	155	mΩ
<b>Peak device</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 3 mA	108	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 300 mA	1.5	2.0	2.5	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 48 V; I <sub>D</sub> = 1600 mA	-	2.2	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V	-	-	2.8	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; V <sub>DS</sub> = 10 V	-	48	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	280	nA
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 15 A	-	19.6	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; I <sub>D</sub> = 10.5 A	-	80	107	mΩ

**Table 10. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH;  $f_1 = 793.5$  MHz;  $f_2 = 818.5$  MHz; RF performance at  $V_{DS} = 48$  V;  $I_{Dq} = 820$  mA (main);  $V_{GS(amp)peak} = 0.30$  V;  $T_{case} = 25$  °C; unless otherwise specified in an asymmetrical Doherty test circuit at frequencies from 791 MHz to 821 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 120$ W	16.8	17.8	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 120$ W	-	-14	-9	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 120$ W	46	51	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 120$ W	-	-33	-28	dBc

**Table 11. RF characteristics**

Test signal: pulsed CW;  $\delta = 10$  %;  $t_p = 100$   $\mu$ s;  $f = 793.5$  MHz; RF performance at  $V_{DS} = 48$  V;  $I_{Dq} = 820$  mA (main);  $V_{GS(amp)peak} = 0.30$  V;  $T_{case} = 25$  °C; unless otherwise specified in an asymmetrical Doherty test circuit at frequencies from 791 MHz to 821 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	-	675	800	-	W

## 7. Test information

### 7.1 Ruggedness in Doherty operation

The BLP9H10S-850AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 50$  V;  $I_{Dq} = 820$  mA;  $V_{GS(amp)peak} = 0.25$  V;  $f = 821$  MHz;  $P_L = 310$  W (5 dB OBO); 1-carrier W-CDMA, 100 % clipping.

### 7.2 Impedance information

**Table 12. Typical impedance of main device**

Measured load-pull data of main device;  $I_{Dq} = 1000$  mA (main);  $V_{DS} = 50$  V; pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

f (MHz)	$Z_S$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )	$P_L$ (W)	$\eta_D$ (%)	$G_p$ (dB)
<b>Maximum power load</b>					
617	4.5 + j2.0	3.4 - j1.2	457.8	64.8	17.7
652	4.0 + j1.5	3.3 - j0.9	445.1	64.6	18.6
698	2.8 + j1.3	2.6 - j0.0	426.6	63.4	18.7
720	3.1 + j1.6	3.1 + j0.2	416.6	61.9	18.5
746	3.0 + j1.8	2.8 - j0.7	461.7	62.6	18.1
757	3.0 + j1.9	2.8 - j0.5	469.4	64.2	18.2
769	2.9 + j2.1	3.1 - j0.7	465.9	66.2	18.6
790	2.8 + j2.3	2.6 - j0.3	467.4	65.7	18.5
805	2.4 + j2.3	2.3 - j0.1	455.9	70.0	19.1
820	2.4 + j2.4	2.2 - j1.0	469.6	63.3	18.1
869	2.6 + j3.0	2.4 - j1.3	462.4	64.1	17.9
894	2.7 + j3.3	2.1 - j0.5	457.0	70.6	18.6

**Table 12. Typical impedance of main device ...continued**

Measured load-pull data of main device;  $I_{DQ} = 1000 \text{ mA (main)}$ ;  $V_{DS} = 50 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f (MHz)	Z <sub>S</sub> (Ω)	Z <sub>L</sub> (Ω)	P <sub>L</sub> (W)	η <sub>D</sub> (%)	G <sub>p</sub> (dB)
925	3.0 + j3.7	1.9 – j1.1	468.1	65.3	17.8
942	3.2 + j3.9	2.1 – j1.4	462.7	64.0	17.6
960	3.5 + j4.2	2.0 – j1.0	459.3	66.7	17.8
<b>Maximum drain efficiency load</b>					
617	4.3 + j2.0	6.5 – j1.0	329.6	71.9	19.7
652	3.8 + j1.6	5.7 + j0.2	332.5	71.3	20.4
698	2.7 + j1.4	5.0 – j0.2	325.6	68.3	20.0
720	3.0 + j1.7	5.6 + j1.6	313.1	71.1	20.4
746	2.8 + j2.0	5.2 + j3.1	271.0	75.1	21.2
757	2.8 + j2.1	5.1 + j2.0	313.6	75.9	20.7
769	2.7 + j2.2	4.0 + j2.5	303.0	76.5	21.1
790	2.7 + j2.4	3.8 + j2.1	310.3	76.8	20.9
805	2.3 + j2.4	3.6 + j2.0	263.2	75.2	21.4
820	2.3 + j2.5	2.7 + j1.9	263.3	77.2	21.9
869	2.5 + j3.0	2.3 + j0.8	345.4	77.3	20.0
894	2.6 + j3.3	2.1 + j0.7	339.0	77.3	20.0
925	2.9 + j3.7	1.9 + j0.6	306.5	75.3	20.6
942	3.2 + j4.0	2.0 + j0.5	315.7	75.1	20.3
960	3.5 + j4.2	1.7 + j0.5	288.8	74.8	20.2

**Table 13. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{DQ} = 1400 \text{ mA (peak)}$ ;  $V_{DS} = 50 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

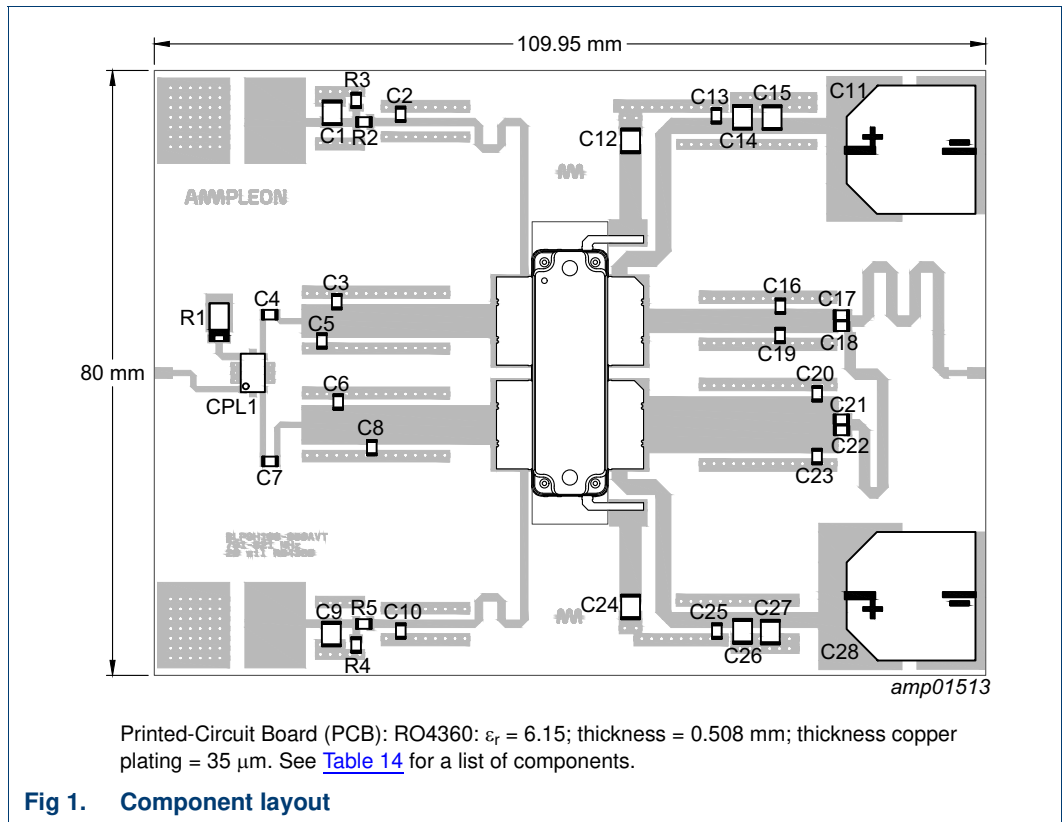
f (MHz)	Z <sub>S</sub> (Ω)	Z <sub>L</sub> (Ω)	P <sub>L</sub> (W)	η <sub>D</sub> (%)	G <sub>p</sub> (dB)
<b>Maximum power load</b>					
617	3.2 – j0.8	2.1 – j1.0	666.4	63.7	18.6
652	2.0 – j0.6	1.7 – j0.9	653.2	61.7	19.4
698	1.8 – j0.9	1.5 – j0.8	669.6	62.5	19.1
720	1.7 – j1.1	1.7 – j0.8	678.5	65.1	19.4
746	1.7 – j1.3	1.4 – j0.8	669.1	62.1	19.0
757	1.7 – j1.4	1.7 – j0.7	666.1	68.4	19.7
769	1.7 – j1.5	1.6 – j0.7	665.0	68.1	19.8
790	1.8 – j1.6	1.5 – j0.8	663.3	68.5	19.7
805	1.9 – j1.7	1.5 – j0.9	629.8	69.2	19.8
820	2.0 – j1.8	1.5 – j1.2	658.9	65.8	19.3
869	2.4 – j2.2	1.5 – j1.2	637.7	68.3	19.5
894	2.7 – j2.3	1.3 – j1.3	642.1	68.0	19.2
925	3.3 – j2.4	1.4 – j1.8	639.0	63.0	18.6

**Table 13. Typical impedance of peak device ...continued**

Measured load-pull data of peak device;  $I_{Dq} = 1400 \text{ mA (peak)}$ ;  $V_{DS} = 50 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f (MHz)	Z <sub>s</sub> (Ω)	Z <sub>L</sub> (Ω)	P <sub>L</sub> (W)	η <sub>D</sub> (%)	G <sub>p</sub> (dB)
942	3.6 – j2.4	1.3 – j1.6	639.6	64.8	18.7
960	4.1 – j2.3	1.1 – j1.7	629.8	62.7	18.3
<b>Maximum drain efficiency load</b>					
617	3.0 + j0.8	4.1 + j0.0	481.0	73.3	20.8
652	1.9 + j0.7	3.2 + j0.2	460.2	71.8	21.8
698	1.8 + j1.0	2.9 + j0.0	511.3	73.3	21.2
720	1.7 + j1.1	2.6 + j0.0	523.6	73.4	21.2
746	1.7 + j1.3	2.8 + j0.1	485.3	73.8	21.3
757	1.7 + j1.4	2.5 + j0.3	477.5	74.6	21.4
769	1.7 + j1.5	2.4 + j0.2	477.2	74.5	21.5
790	1.8 + j1.7	2.3 + j0.2	477.8	75.1	21.4
805	1.9 + j1.7	1.9 + j0.0	452.1	73.9	21.4
820	1.9 + j1.8	2.0 – j0.3	496.0	74.3	21.1
869	2.4 + j2.1	1.6 – j0.3	451.5	74.6	21.2
894	2.7 + j2.3	1.4 – j0.2	409.1	74.5	21.3
925	3.3 + j2.3	1.2 – j0.4	404.1	73.7	21.2
942	3.7 + j2.3	1.4 – j0.6	449.0	73.0	20.8
960	4.1 + j2.0	1.3 – j0.6	426.6	72.1	20.7

7.3 Test circuit



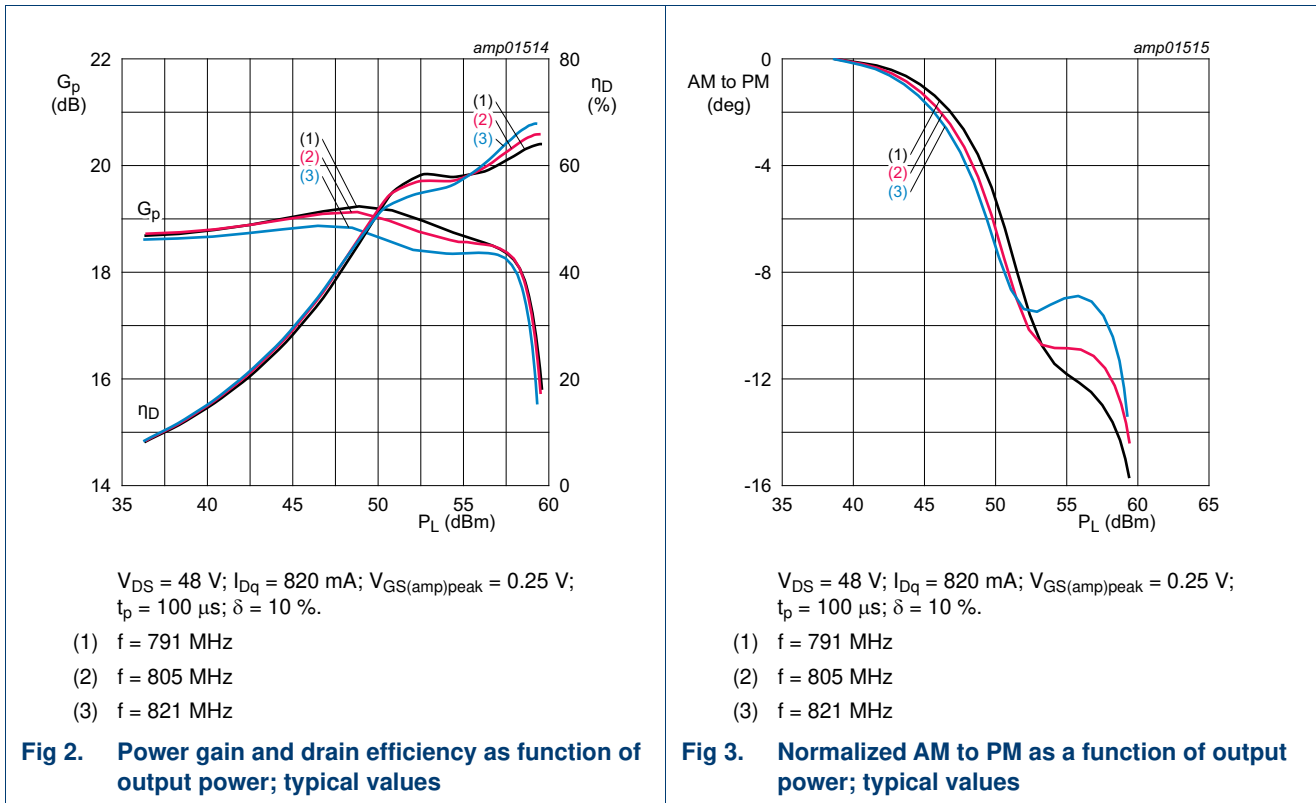
**Table 14. List of components**

See [Figure 1](#) for component layout.

Component	Description	Value	Remarks
C1, C9, C12, C14, C15, C24, C26, C27	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 100 V	Murata: GCM32DC72A475KE02L
C2, C4, C7, C10, C13, C25	multilayer ceramic chip capacitor	68 pF	Murata: HiQ GQM21 0805
C3, C5	multilayer ceramic chip capacitor	1.5 pF	Murata: HiQ GQM21 0805
C6	multilayer ceramic chip capacitor	3 pF	Murata: HiQ GQM21 0805
C8, C16, C19	multilayer ceramic chip capacitor	2.2 pF	Murata: HiQ GQM21 0805
C11, C28	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	radial leaded
C17, C18	multilayer ceramic chip capacitor	4.3 pF	Murata: HiQ GQM21 0805
C20	multilayer ceramic chip capacitor	2.7 pF	Murata: HiQ GQM21 0805
C21, C22	multilayer ceramic chip capacitor	33 pF	Murata: HiQ GQM21 0805
C23	multilayer ceramic chip capacitor	1.6 pF	Murata: HiQ GQM21 0805
R1	resistor	50 $\Omega$ , 16 W	Anaren: C16A50Z4
R2, R5	resistor	4.7 $\Omega$ , 1 %	SMD 0805
R3, R4	resistor	10 k $\Omega$ , 1 %	SMD 0805
CPL1	hybrid coupler	2 dB, 90°	Anaren: X3C07F1-02S

7.4 Graphical data

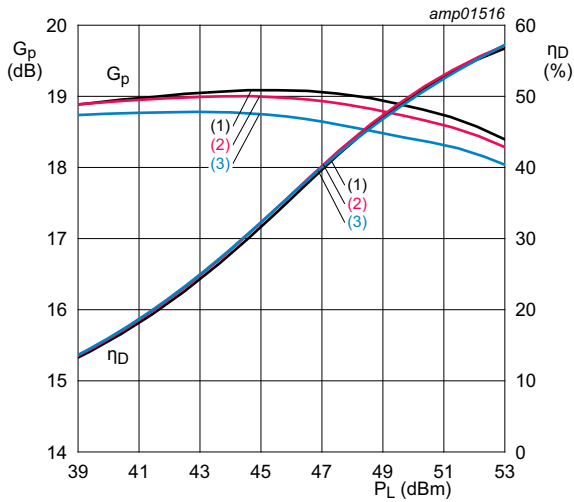
7.4.1 Pulsed CW





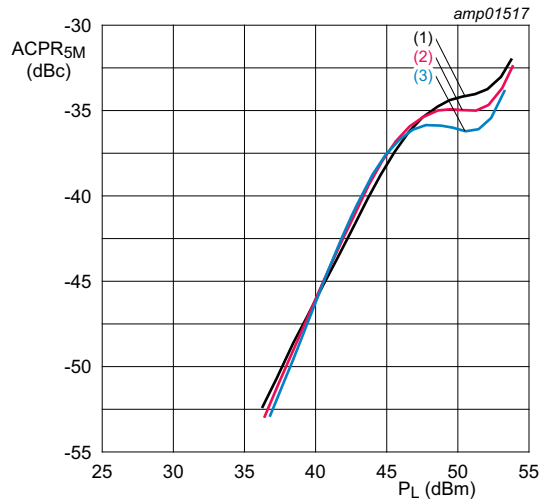
7.4.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping); PAR = 9.9 dB at 0.01 % probability on CCDF per carrier.



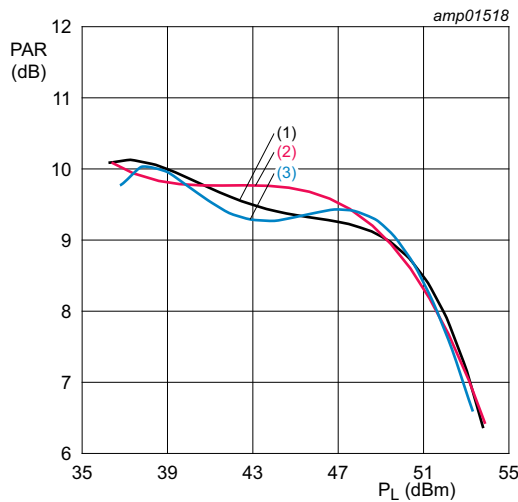
$V_{DS} = 48\text{ V}; I_{Dq} = 820\text{ mA}; V_{GS(amp)peak} = 0.25\text{ V}.$   
 (1)  $f = 791\text{ MHz}$   
 (2)  $f = 805\text{ MHz}$   
 (3)  $f = 821\text{ MHz}$

Fig 4. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 48\text{ V}; I_{Dq} = 820\text{ mA}; V_{GS(amp)peak} = 0.25\text{ V}.$   
 (1)  $f = 791\text{ MHz}$   
 (2)  $f = 805\text{ MHz}$   
 (3)  $f = 821\text{ MHz}$

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

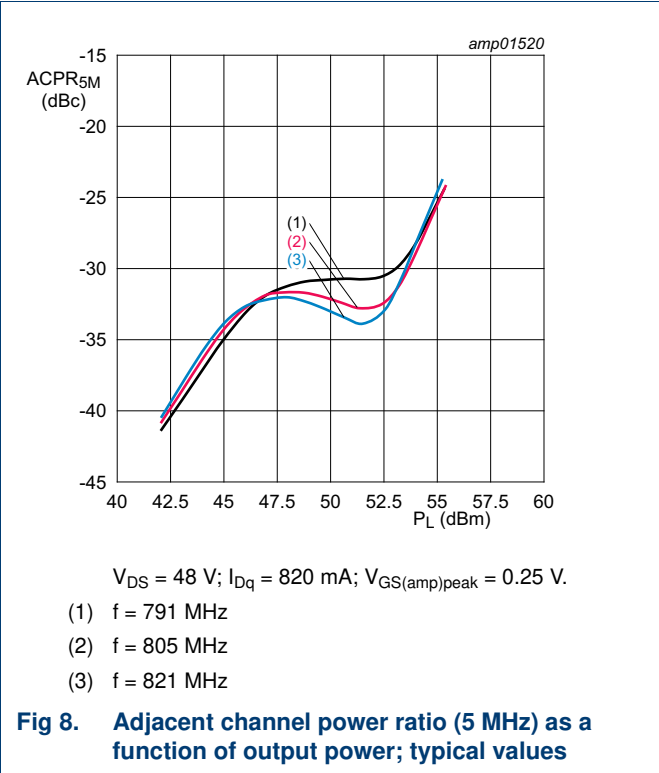
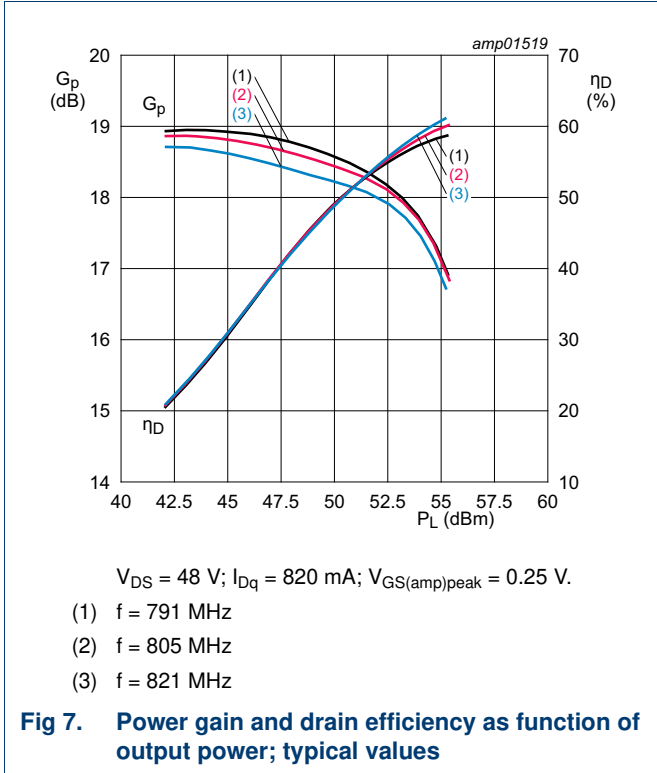


$V_{DS} = 48\text{ V}; I_{Dq} = 820\text{ mA}; V_{GS(amp)peak} = 0.25\text{ V}.$   
 (1)  $f = 791\text{ MHz}$   
 (2)  $f = 805\text{ MHz}$   
 (3)  $f = 821\text{ MHz}$

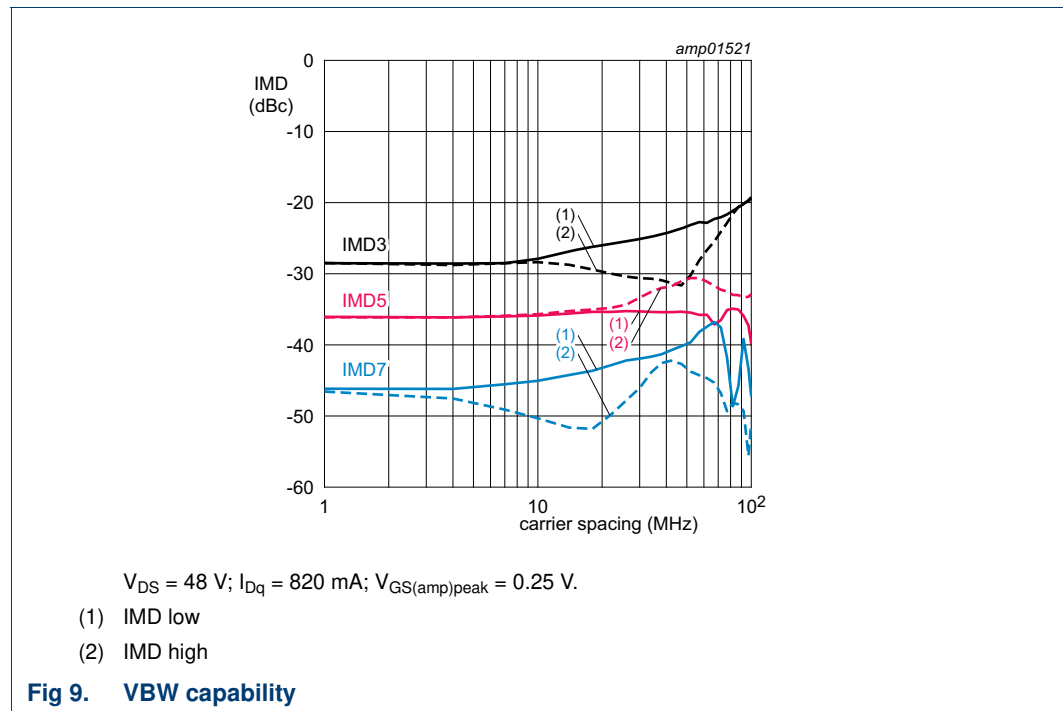
Fig 6. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Carrier W-CDMA

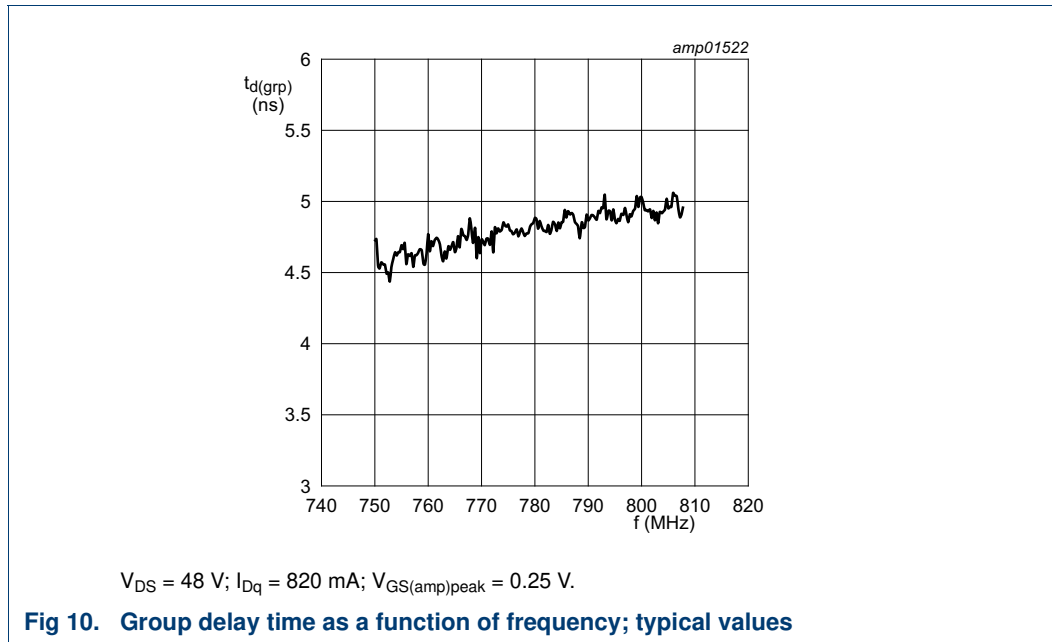
Test signal: 3GPP test model 1; 1 to 64 DPCH (46 % clipping); PAR = 9.9 dB at 0.01 % probability on CCDF per carrier.



7.4.4 2-Tone VBW



7.4.5 Group delay



8. Package outline

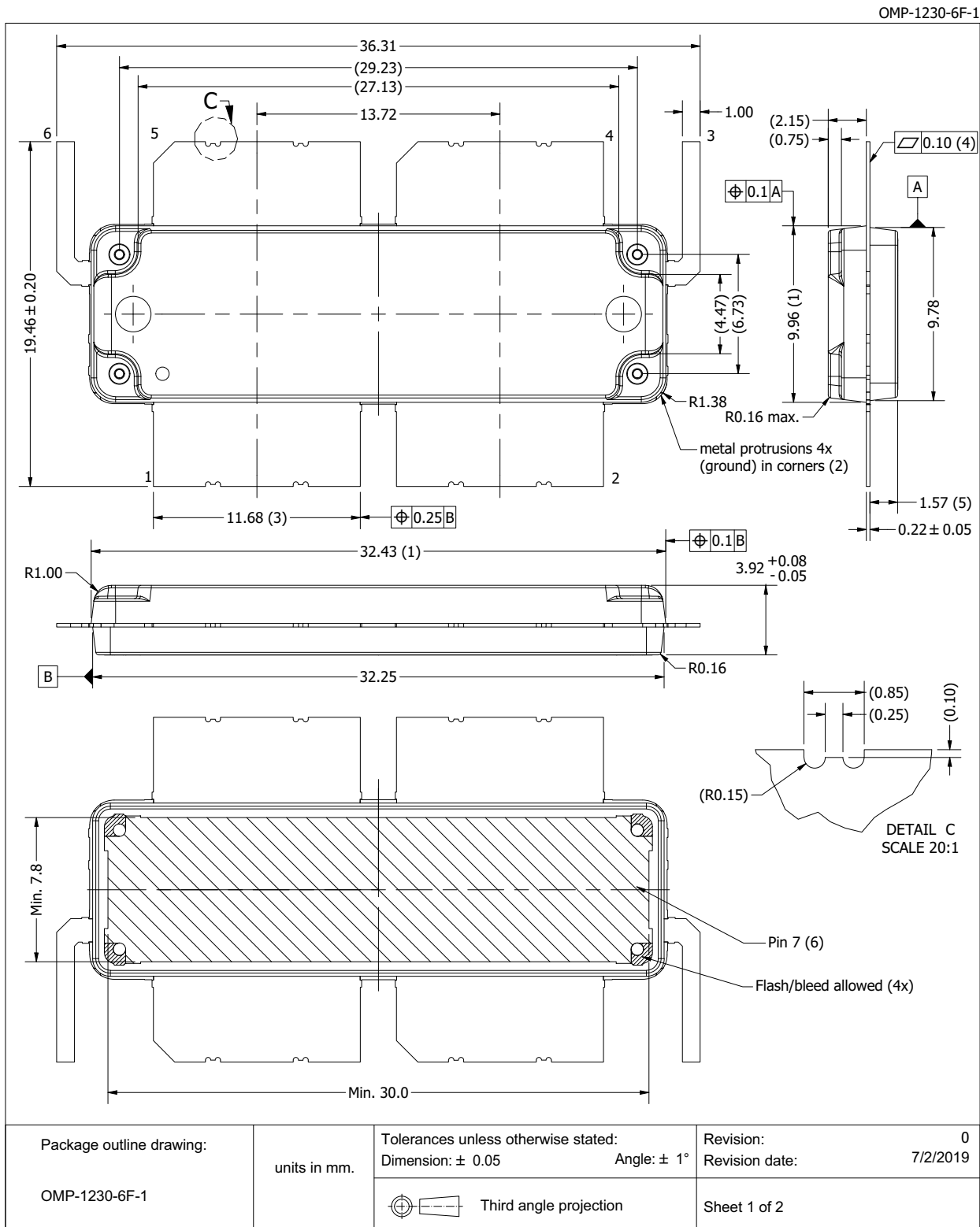


Fig 11. Package outline OMP-1230-6F-1 (sheet 1 of 2)

OMP-1230-6F-1

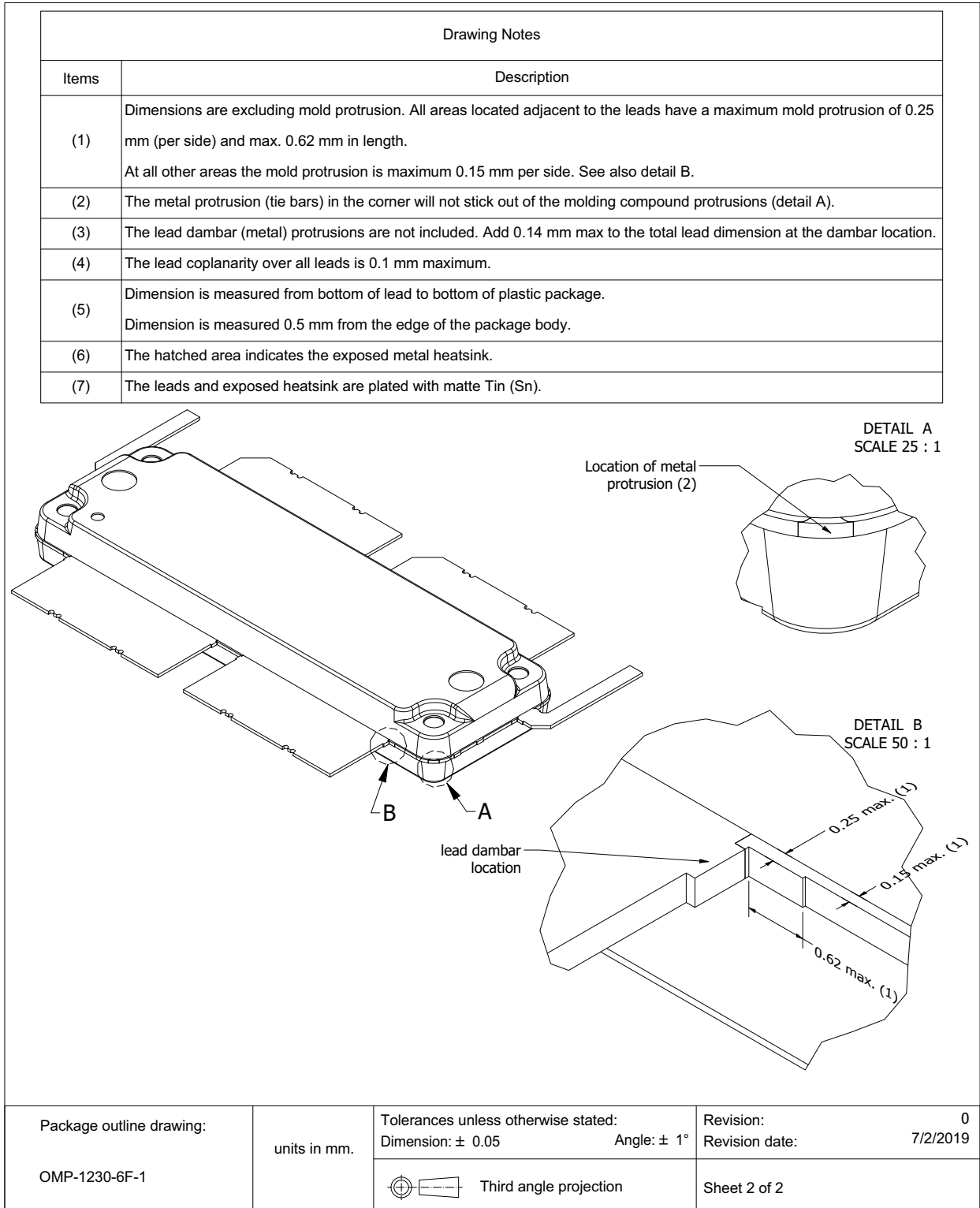


Fig 12. Package outline OMP-1230-6F-1 (sheet 2 of 2)

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 15. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

**Table 16. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 17. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP9H10S-850AVT v.1	20220525	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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