

## NC7SZD384

### TinyLogic™ UHS 1-Bit Low Power Bus Switch with Level Shifting

#### General Description

The NC7SZD384 provides 1-bit of high-speed CMOS TTL-compatible bus switch. The low on resistance of the switch allows inputs to be connected to outputs with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 1-bit switch with a bus enable ( $\overline{BE}$ ) signal. When  $\overline{BE}$  is LOW, the switch is on and Port A is connected to Port B. When  $\overline{BE}$  is HIGH, the switch is open and a high-impedance state exists between the two ports. Reduced voltage drive to the gate of the FET switch permits nominal level shifting of 5V to 3.3V through the switch.

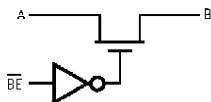
#### Features

- Space saving SOT23 or SC70 5-lead package.
- $5\Omega$  switch connection between two ports.
- Designed to be used in level-shifting applications.
- Minimal propagation delay through the switch.
- Low  $I_{CC}$ .
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

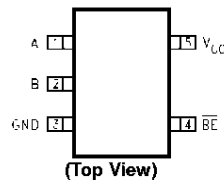
#### Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
NC7SZD384M5	MA05B	8Z4D	5-Lead SOT23, JEDEC MO-178, 1.6mm	250 Units on Tape and Reel
NC7SZD384M5X	MA05B	8Z4D	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7SZD384P5	MAA05A	Z4D	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	250 Units on Tape and Reel
NC7SZD384P5X	MAA05A	Z4D	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel

#### Logic Symbol



#### Connection Diagram



#### Pin Descriptions

Pin Name	Description
$\overline{BE}$	Bus Switch Enable
A	Bus A
B	Bus B

#### Function Table

$\overline{BE}$	$B_O$	Function
L	$A_O$	Connect
H	HIGH-Z State	Disconnect

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Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
Supply Voltage ( $V_{CC}$ )	0.5V to +7.0V	Power Supply Operating ( $V_{CC}$ )	4.5V to 5.5V
DC Switch Voltage (VS)	-0.5V to +7.0V	Input Voltage ( $V_{IN}$ )	0V to 5.5V
DC Input Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +7.0V	Output Voltage ( $V_{OUT}$ )	0V to 5.5V
DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$	-50 mA	Input Rise and Fall Time ( $t_r, t_f$ )	
DC Output ( $I_{OUT}$ ) Sink Current	128 mA	Switch Control Input	0 ns/V to 5 ns
DC $V_{CC}/GND$ Current ( $I_{CC}/GND$ )	$\pm 100$ mA	Switch I/O	0 ns/V to DC
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C	Operating Temperature ( $T_A$ )	-40°C to +85°C
Junction Temperature under bias ( $T_J$ )	+150°C	Thermal Resistance ( $\theta_{JA}$ )	
Junction Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	+260°C	SOT23-5	300°C/Watt
Power Dissipation ( $P_D$ ) @ +85°C		SC70-5	425°C/Watt
SOT23-5	200 mW		
SC70-5	150 mW		

**Note 1:** The 'Absolute Maximum Ratings' are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The 'Recommended Operating Conditions' table will define the conditions for actual device operation.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Min	Typ (Note 3)			Max
$V_{IK}$	Maximum Clamp Diode Voltage	4.5		-1.2	-V	$I_{IN} = -18$ mA	
$V_{IH}$	HIGH Level Input Voltage	4.5-5.5	2.0		V		
$V_{IL}$	LOW Level Input Voltage	4.5-5.5		0.8	V		
$V_{OH}$	HIGH Level Output Voltage						
$I_I$	Input Leakage Current	0-5.5		$\pm 1.0$	$\mu\text{A}$	$0 \leq V_{IN} \leq 5.5V$	
$I_{OFF}$	*OFF* Leakage Current	5.5		$\pm 10.0$	$\mu\text{A}$	$0 \leq A, B, \leq V_{CC}$	
$R_{ON}$	Switch On Resistance (Note 4)	4.5		5	7	$\Omega$	$V_{IN} = 0V, I_I = 64$ mA
				5	7	$\Omega$	$V_{IN} = 0V, I_I = 30$ mA
				35	50	$\Omega$	$V_{IN} = 2.4V, I_I = 15$ mA
$I_{CC}$	Quiescent Supply Current					$V_{IN} = V_{CC}$ or GND, $I_O = 0$	
	Switch On	5.5	0.8	1.5	mA	/BE = GND	
	Switch Off	5.5		10	$\mu\text{A}$	/BE = VCC	
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input (Note 5)	5.5	0.8	2.5	mA	/BE = 3.4V, $I_O = 0$ , Control Input only.	

**Note 3:** All typical values are at  $V_{CC} = 5.0V, T_A = 25^\circ\text{C}$

**Note 4:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

**Note 5:** Per TTL driven input ( $V_{IN} = 3.4V$  control input only). A and B pins do not contribute to  $I_{CC}$ .

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF, R <sub>U</sub> =R <sub>D</sub> =500Ω		Units	Conditions	Fig. No.
			Min	Typ (Note 6)			
t <sub>PHL</sub> t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 7)	4.5-5.5		0.25	ns	V <sub>I</sub> = Open	Figure 1 Figure 2
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	4.5-5.5	1.5	7.5	ns	V <sub>I</sub> = 7V for t <sub>PZL</sub> V <sub>I</sub> = OPEN for t <sub>PZH</sub>	Figure 1 Figure 2
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	4.5-5.5	1.0	6.0	ns	V <sub>I</sub> = 7V for t <sub>PLZ</sub> V <sub>I</sub> = OPEN for t <sub>PHZ</sub>	Figure 1 Figure 2

**Note 6:** All typical values are V<sub>CC</sub> = 5.0V T<sub>A</sub> = 25°C

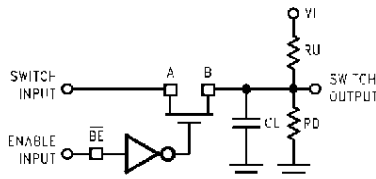
**Note 7:** This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance when driven by an ideal voltage source (zero output impedance)

## Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C <sub>IN</sub>	Control Pin Input Capacitance	2	5	pF	V <sub>CC</sub> = 5.0V
C <sub>I/O</sub>	Input/Output Capacitance	4.5	10	pF	V <sub>CC</sub> = 5.0V

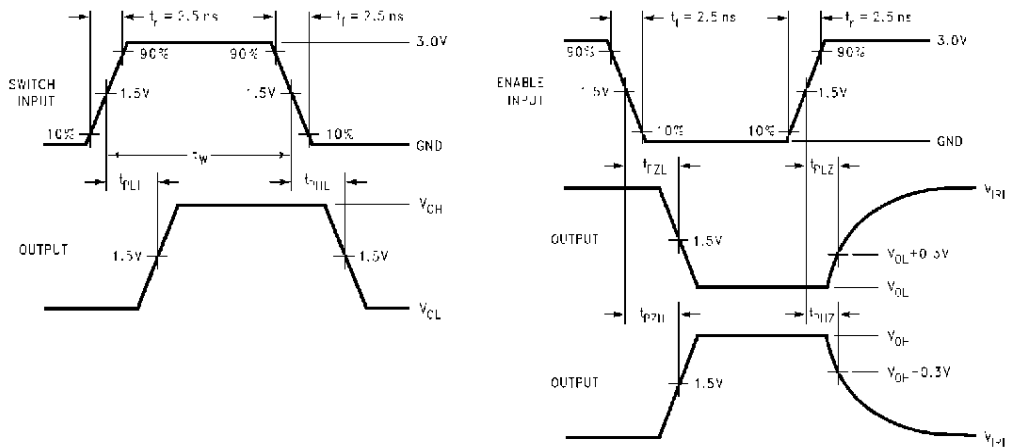
**Note 8:** T<sub>A</sub> = 25°C f = 1MHz

## AC Loading and Waveforms



**FIGURE 1. AC Test Circuit**

**Note:** Input driven by 50Ω source terminated in 50Ω  
C<sub>L</sub> includes load and stray capacitance  
Input PRR = 1.0 MHz t<sub>w</sub> = 500 ns



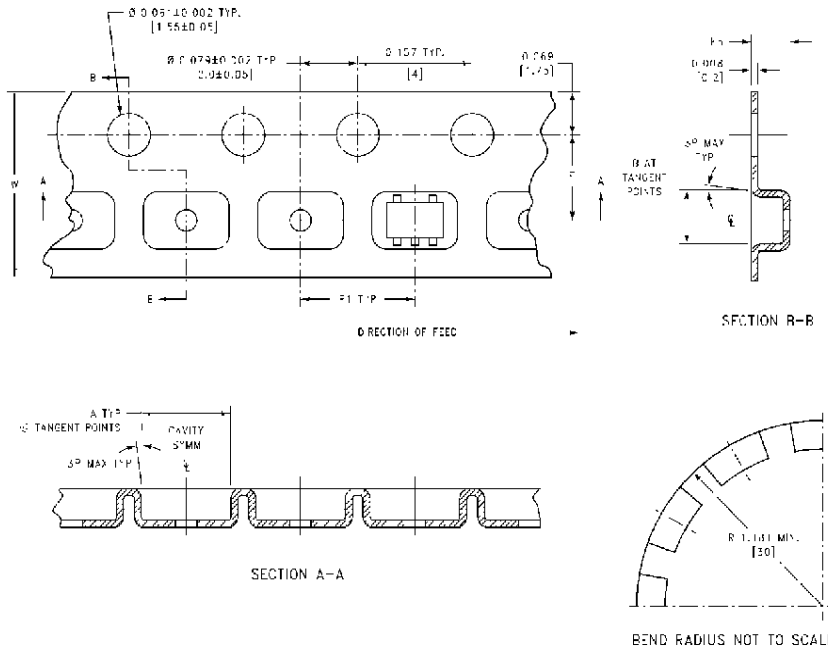
**FIGURE 2. AC Waveforms**

### Tape and Reel Specification

TAPE FORMAT

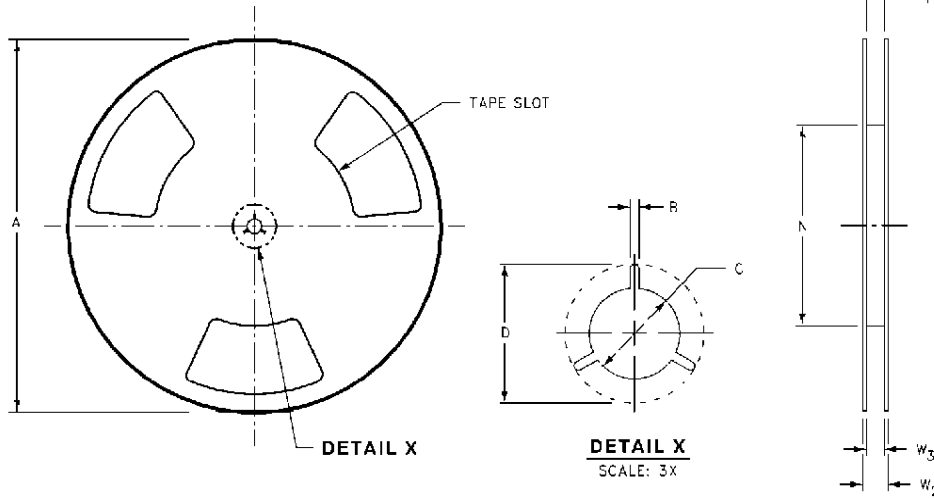
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5, P5	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



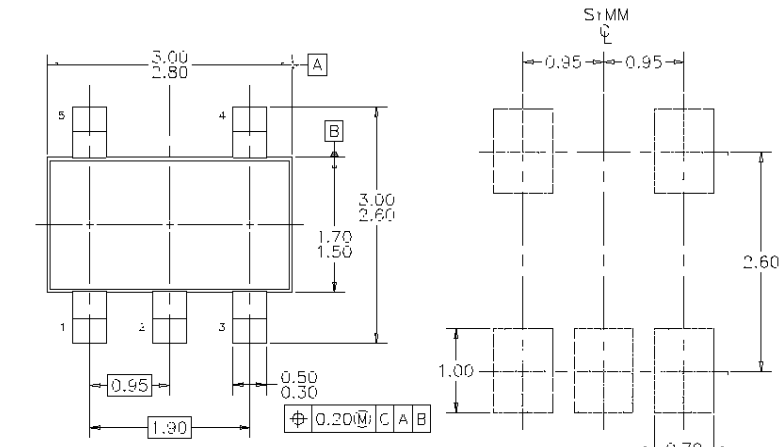
Package	Tape Size	DIM A	DIM B	DIM F	DIM K <sub>0</sub>	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

REEL DIMENSIONS inches (millimeters)

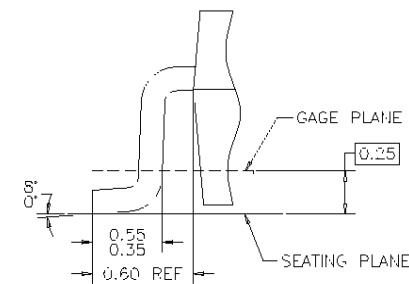
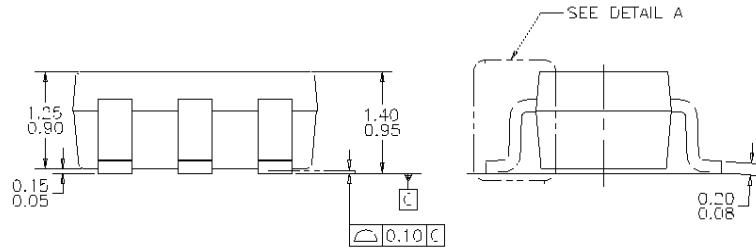


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

**Physical Dimensions** inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION

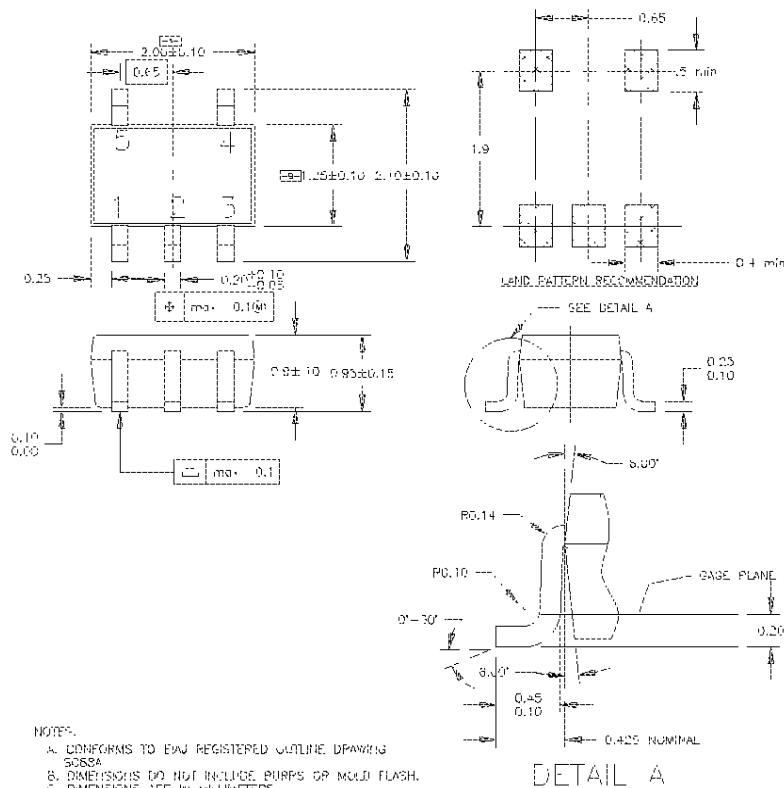


NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA, DATED JANUARY 1999.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.

**5-Lead SOT23, JEDEC MO-178, 1.6mm  
Package Number MA05B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**5-Lead SC70, EIAJ SC-88a, 1.25mm Wide  
Package Number MAA05A**

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