



Improved Standard Products®

**SD-SST210/214**  
**N-CHANNEL LATERAL**  
**DMOS SWITCH**

PART NUMBER	V <sub>(BR)DS</sub> Min (V)	V <sub>(GS)th</sub> Max (V)	r <sub>DS(on)</sub> Max (Ω)	C <sub>rss</sub> Max (pF)	t <sub>ON</sub> Max (ns)
SD210DE	30	1.5	45 @ V <sub>GS</sub> =10V	0.5	2
SD214DE	20	1.5	45 @ V <sub>GS</sub> =10V	0.5	2
SST210	30	1.5	50 @ V <sub>GS</sub> =10V	0.5	2
SST214	20	1.5	50 @ V <sub>GS</sub> =10V	0.5	2

**PRODUCT SUMMARY**

**Features**

- Ultra-High Speed Switching—t<sub>ON</sub>: 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed r<sub>DS</sub> @5V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

**Benefits**

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

**Applications**

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

**Description**

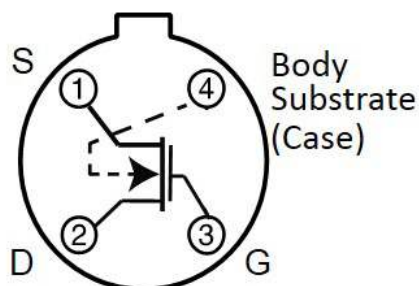
The SD210DE/214 and SST210/214 are enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The SD214DE and SST214 are normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These MOSFETs do not

have a gate protection Zener diode which results in lower gate leakage and ± voltage capability from gate to substrate. A polysilicon gate is featured for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, Zener protected—SD211DE/SST211 Series.

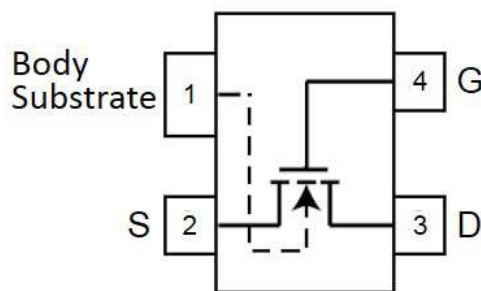
**Top Views**

**SD210DE, SD214DE**



TO-206AF  
(TO-72)

**SST210, SST214**



TO-253  
(SOT-143)

## Absolute Maximum Ratings (T<sub>A</sub> = 25°C unless otherwise noted)

Gate-Drain, Gate-Source Voltage	..... ± 40V	Source-Substrate Voltage	(SD210DE/SST210) ..... 15V
Gate-Substrate Voltage	..... ± 30V		(SD210DE/SST210) ..... 25V
Drain-Source Voltage	(SD210DE/SST210) ..... 30V	Drain Current	..... .50mA
	(SD214DE/SST214) ..... 20V	Lead Temperature (1/16" from case for 10 seconds)	..... 300°C
Source-Drain Voltage	(SD210DE/SST210) ..... 10V	Storage Temperature	..... -65 to 150°C
	(SD214DE/SST214) ..... 20V	Operating Junction Temperature	..... -55 to 125°C
Drain-Substrate Voltage	(SD210DE/SST210) ..... 30V	Power Dissipation*	..... .300mW
	(SD214DE/SST214) ..... 25V		

Note:

\* Derate 3mW/°C above 25°C

## Specifications<sup>a</sup>

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS				UNIT	
				210 Series		214 Series			
				Min	Max	Min	Max		
<b>Static</b>									
Drain - Source Breakdown Voltage	V <sub>(BR)DS</sub>	V <sub>GS</sub> = V <sub>BS</sub> = 0V, I <sub>D</sub> = 10 μA	35	30				V	
		V <sub>GS</sub> = V <sub>BS</sub> = -5V, I <sub>D</sub> = 10 nA	30	10		20			
Source - Drain Breakdown Voltage	V <sub>(BR)SD</sub>	V <sub>GD</sub> = V <sub>BD</sub> = -5V, I <sub>S</sub> = 10 nA	22	10		20			
Drain - Substrate Breakdown Voltage	V <sub>(BR)DBO</sub>	V <sub>GB</sub> = 0V, I <sub>D</sub> = 10 nA Source Open	35	15		25			
Source - Substrate Breakdown Voltage	V <sub>(BR)SBO</sub>	V <sub>GB</sub> = 0V, I <sub>S</sub> = 10 μA Drain Open	35	15		25			
Drain - Source Leakage	I <sub>DS(off)</sub>	V <sub>GS</sub> = V <sub>BS</sub> = -5V	V <sub>DS</sub> = 10V	0.4		10		nA	
			V <sub>DS</sub> = 20V	0.9			10		
Source - Drain Leakage	I <sub>SD(off)</sub>	V <sub>GD</sub> = V <sub>BD</sub> = -5V	V <sub>SD</sub> = 10V	0.5		10			
			V <sub>SD</sub> = 20V				10		
Gate Leakage	I <sub>GBS</sub>	V <sub>DB</sub> = V <sub>SB</sub> = 0V, V <sub>GB</sub> = ±40V	±0.001		±100		±100	pA	
Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1 μA, V <sub>SB</sub> = 0V	0.8	0.5	1.5	0.1	1.5	V	
Drain - Source On-Resistance	r <sub>DS(on)</sub>	V <sub>SB</sub> = 0V I <sub>D</sub> = 1mA	V <sub>GS</sub> = 5V (SD Series)	58		70		70	Ω
			V <sub>GS</sub> = 5V (SST Series)	60		75		75	
			V <sub>GS</sub> = 10V (SD Series)	38		45		45	
			V <sub>GS</sub> = 10V (SST Series)	40		50		50	
			V <sub>GS</sub> = 15V	30					
			V <sub>GS</sub> = 20V	26					
			V <sub>GS</sub> = 25V	24					

# Specifications<sup>a</sup>

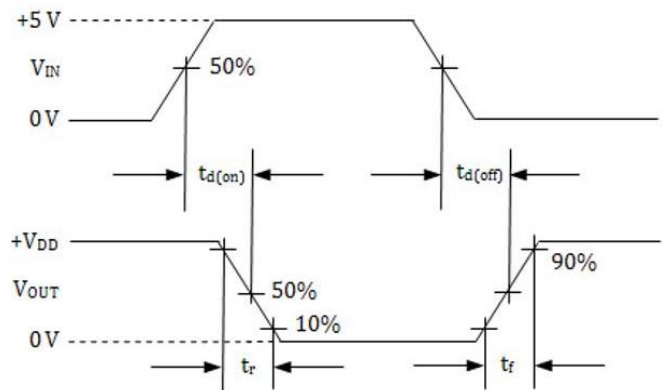
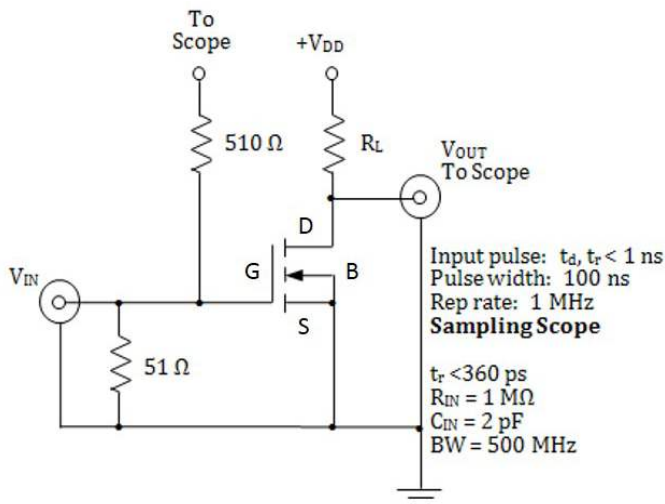
PARAMETER	SYMBOL <sup>b</sup>	TEST CONDITIONS <sup>b</sup>	TYP <sup>c</sup>	LIMITS				UNIT	
				210 Series		214 Series			
				Min	Max	Min	Max		
<b>Dynamic</b>									
Forward Transconductance	$g_{fs}$	$V_{DS} = 10V, V_{SB} = 0V, I_D = 20mA, f = 1kHz$	SD Series	11	10		10		mS
			SST Series	10.5	9		9		
			All	0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10V, f = 1MHz, V_{GS} = V_{BS} = -15V$	SD Series	2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5	
Reverse Transfer Capacitance	$C_{rss}$			SST Series	4.2				
			SD Series	0.2		0.5		0.5	
<b>Switching</b>									
Turn-On Time	$t_{D(on)}$	SD Series Only $V_{SB} = 0V, V_{IN} 0 \text{ to } 5V, R_G = 25\Omega, V_{DD} = 5V, R_L = 680\Omega$	0.5		1		1	ns	
	$t_r$		0.6		1		1		
Turn-Off Time	$t_{D(off)}$		2						
	$t_f$		6						

## NOTES:

- $T_A = 25^\circ C$  unless otherwise notes.
- B is the body (substrate) and  $V_{(BR)}$  is breakdown voltage.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

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## Switching Time Test Circuit



Linear Integrated Systems develops and produces the highest performance semiconductors of their kind in the industry. Linear Systems, founded in 1987, uses patented and proprietary processes and designs to create its high performance discrete semiconductors. Expertise brought to the company is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company founder John H. Hall.