HARRIS HM-6514

1024 x 4 CMOS RAM

Features

- Low Power Standby ..... 125μW Max.
- Low Power Operation ..... 35mW/MHz Max.
- Data Retention ..... @ 2.0V Min.
- TTL Compatible Input/Output
- Common Data In/Out
- Three-State Outputs
- Standard JEDEC Pinout
- Fast Access Time ..... 120/200ns Max.
- Wide Operating Temperature Ranges:
  - ▸ HM-6514-9 ..... -40°C to +85°C
  - ▸ HM-6514-8 ..... -55°C to +125°C
- 18 Pin Package for High Density
- On-Chip Address Register
- Gated Inputs—No Pull Up or Pull Down Resistors Required

Description

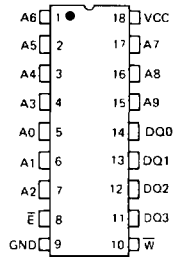
The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays. Gated inputs allow lower operating current and also eliminates the need for pull-up or pull-down resistors.

The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

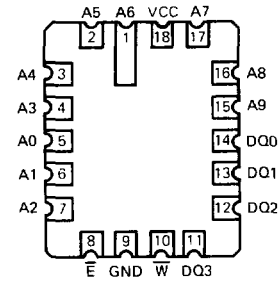
Pinouts

TOP VIEW



LCC

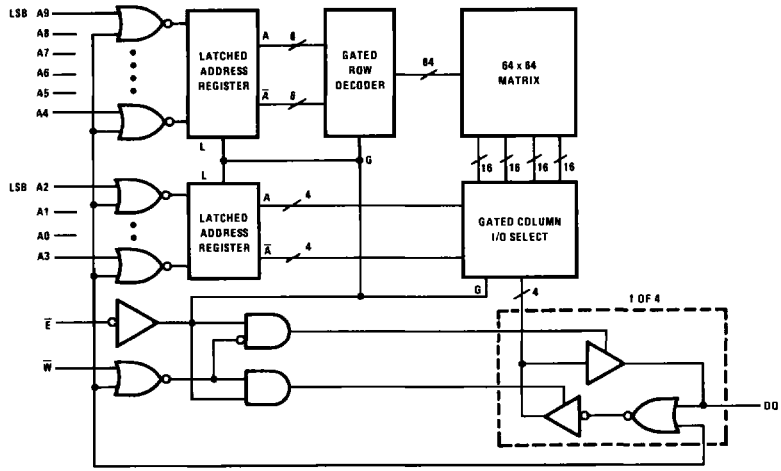
TOP VIEW



PIN NAMES

A — Address Input $\overline{W}$ — Write Enable
$\overline{E}$ — Chip Enable DQ — Data In/Out

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 6910 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6514S-8 ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514S-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	25	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514S-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	120	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	120	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	50	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	120	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	50	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	40	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	120	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	120	-	ns	(Notes 1, 4)
(11) TELWH	Write Enable Pulse Hold Time	120	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	50	-	ns	(Notes 1, 4)
(13) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLDV	Write Data Delay Time	70	-	ns	(Notes 1, 4)
(15) TWLEL	Early Output High-Z Time	0	-	ns	(Notes 1, 4)
(16) TEHWH	Late Output High-Z Time	0	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	170	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 6910 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6514S-9 ..... -40°C to +85°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514S-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	25	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI ≈ GND
ICCDR	Data Retention Supply Current	-	15	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI ≈ VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. *VCC = 4.5V and 5.5V.*

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514S-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	120	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	120	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	50	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	120	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	50	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	40	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	120	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	120	-	ns	(Notes 1, 4)
(11) TELWH	Write Enable Pulse Hold Time	120	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	50	-	ns	(Notes 1, 4)
(13) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLDV	Write Data Delay Time	70	-	ns	(Notes 1, 4)
(15) TWLEL	Early Output High-Z Time	0	-	ns	(Notes 1, 4)
(16) TEHWH	Late Output High-Z Time	0	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	170	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 6910 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6514B-8 ..... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	25	µA	IO = 0, VCC = 2.0V, $\overline{E}$ ≈ VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f ≈ 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC ≈ 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	200	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	220	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	200	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	90	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	200	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	200	-	ns	(Notes 1, 4)
(11) TELWH	Write Enable Pulse Hold Time	200	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	120	-	ns	(Notes 1, 4)
(13) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLDV	Write Data Delay Time	80	-	ns	(Notes 1, 4)
(15) TWLEL	Early Output High-Z Time	0	-	ns	(Notes 1, 4)
(16) TEHWH	Late Output High-Z Time	0	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	290	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 6910 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6514B-9 ..... -40°C to +85°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514B-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	25	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	15	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514B-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	200	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	220	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	80	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	200	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	90	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	200	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	200	-	ns	(Notes 1, 4)
(11) TELWH	Write Enable Pulse Hold Time	200	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	120	-	ns	(Notes 1, 4)
(13) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLDV	Write Data Delay Time	80	-	ns	(Notes 1, 4)
(15) TWLEL	Early Output High-Z Time	0	-	ns	(Notes 1, 4)
(16) TEHWH	Late Output High-Z Time	0	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	290	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 6910 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6514-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6514-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	25	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	300	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	320	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	100	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	300	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	120	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	300	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	300	-	ns	(Notes 1, 4)
(11) TELWH	Write Enable Pulse Hold Time	300	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	200	-	ns	(Notes 1,4)
(13) TWHDZ	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLDV	Write Data Delay Time	100	-	ns	(Notes 1, 4)
(15) TWLEL	Early Output High-Z Time	0	-	ns	(Notes 1, 4)
(16) TEHWH	Late Output High-Z Time	0	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	420	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 12°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} ..... 66°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count ..... 6910 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6514-9 ..... -40°C to +85°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	25	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCOP	Operating Supply Current (Note 3)	-	7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
ICCDR	Data Retention Supply Current	-	15	µA	IO = 0, VCC = 2.0V, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 2.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

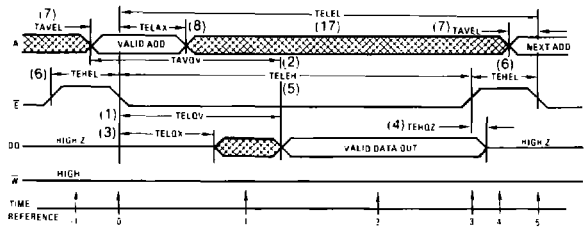
NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6514-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	300	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	320	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	100	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	300	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	120	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TWLWH	Write Enable Pulse Width	300	-	ns	(Notes 1, 4)
(10) TWLEH	Write Enable Pulse Setup Time	300	-	ns	(Notes 1, 4)
(11) TELWH	Write Enable Pulse Hold Time	300	-	ns	(Notes 1, 4)
(12) TDVWH	Data Setup Time	200	-	ns	(Notes 1, 4)
(13) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(14) TWLDV	Write Data Delay Time	100	-	ns	(Notes 1, 4)
(15) TWLEL	Early Output High-Z Time	0	-	ns	(Notes 1, 4)
(16) TEHWH	Late Output High-Z Time	0	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	420	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Read Cycle

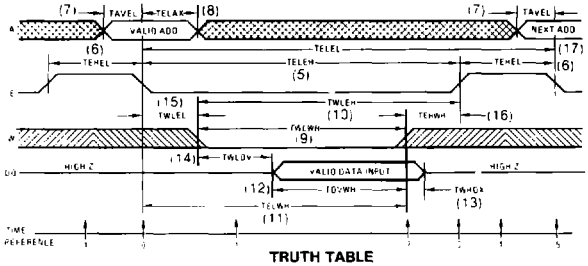


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as - 1)
5	↓	H	V	Z	Cycle Ends, Next Cyle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs and ready the RAM for the next memory cycle (T = 4).

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	X	Z	Write Period Begins
2	L	↓	X	V	Data In is Written
3	↑	H	X	Z	Write Completed
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs and all inputs will three-state after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

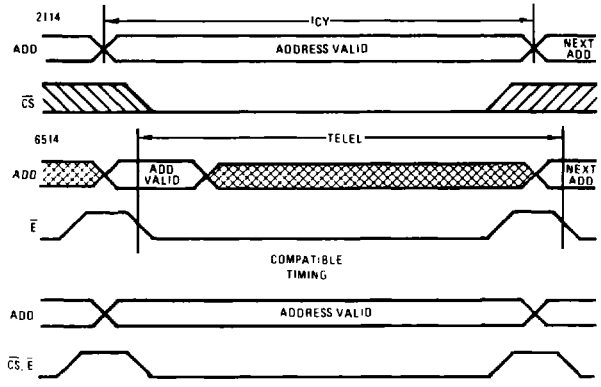
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rising

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met, but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDX become TDVEH and TEHDX. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ and $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDX

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

2114 Capability



2114 - Requires the Address to Remain Valid Throughout the Cycle.

6514 - Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle